# MODEL GT 9000S
# SYNTHESIZED MICROWAVE SWEEPER

Giga-tronics

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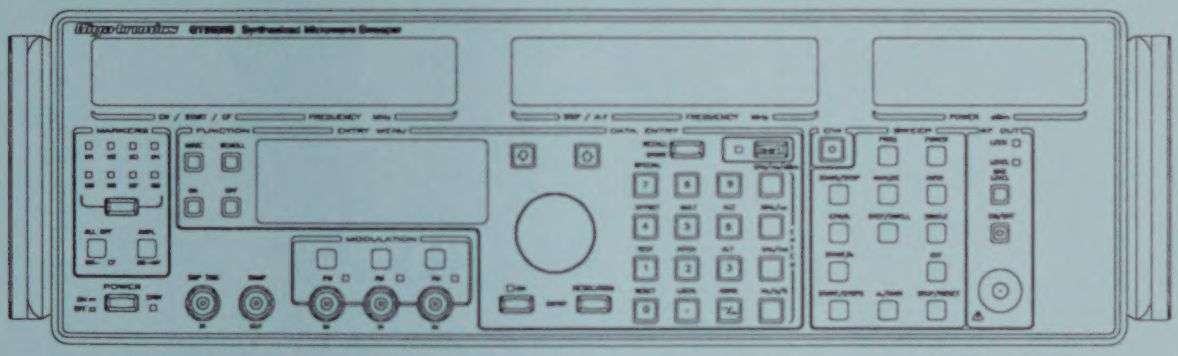
# OPERATION & MAINTENANCE MANUAL

## Model GT 9000S
## Synthesized Microwave Sweeper



*Volume 2 of 2*

*(Includes Sections 7 through 10)*

**Print Date: June, 1994**

**Manual Part Number: 120AM00350**

For instrument part numbers and configurations, see page iii.

The instrument has a 6-digit serial number, shown on a sticker on the rear panel. This manual applies to all serial numbers listed in Manual Changes (Section 10 in the second volume).

Printed in U.S.A.

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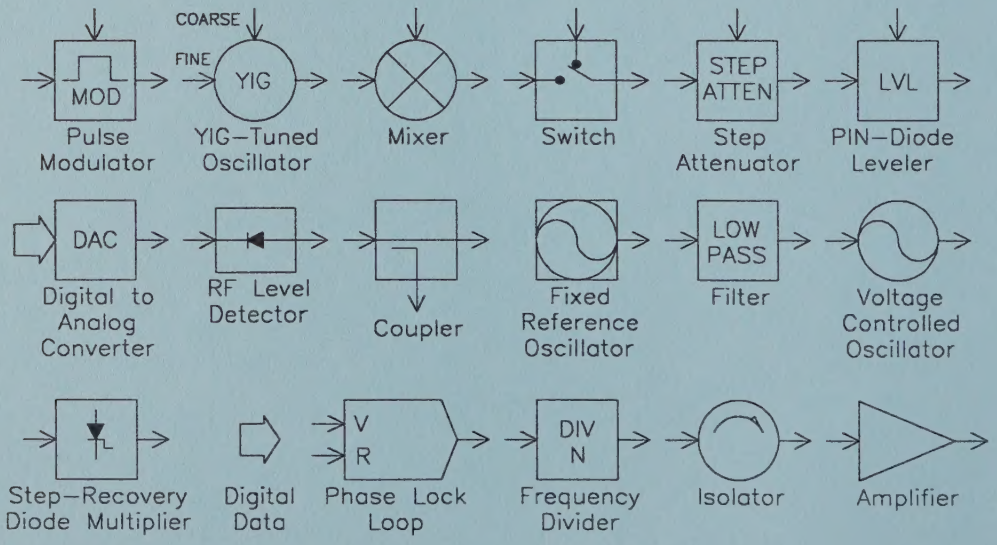
## *SYMBOLS*

Block diagram symbols frequently used in the manual are illustrated below.



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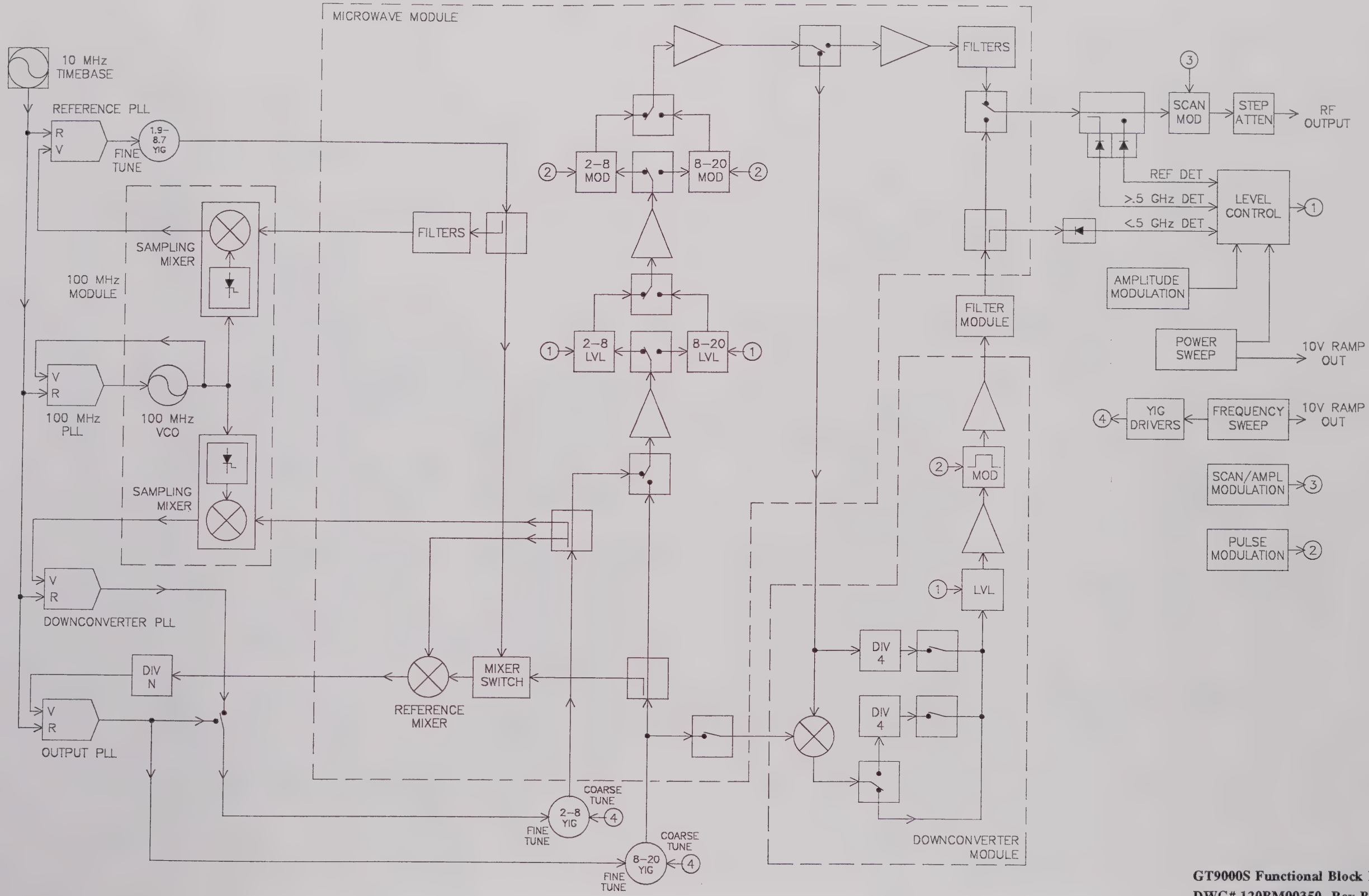
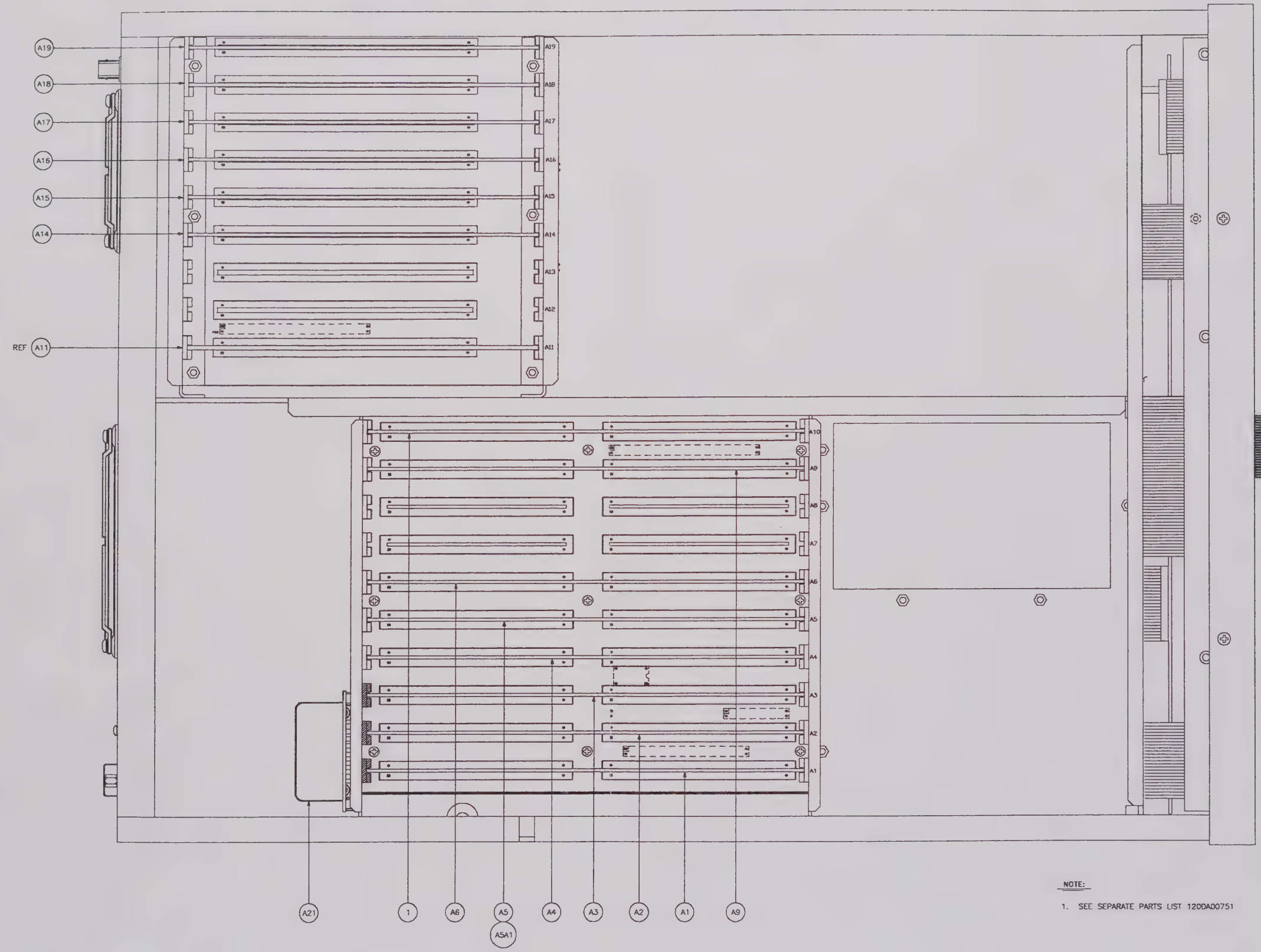


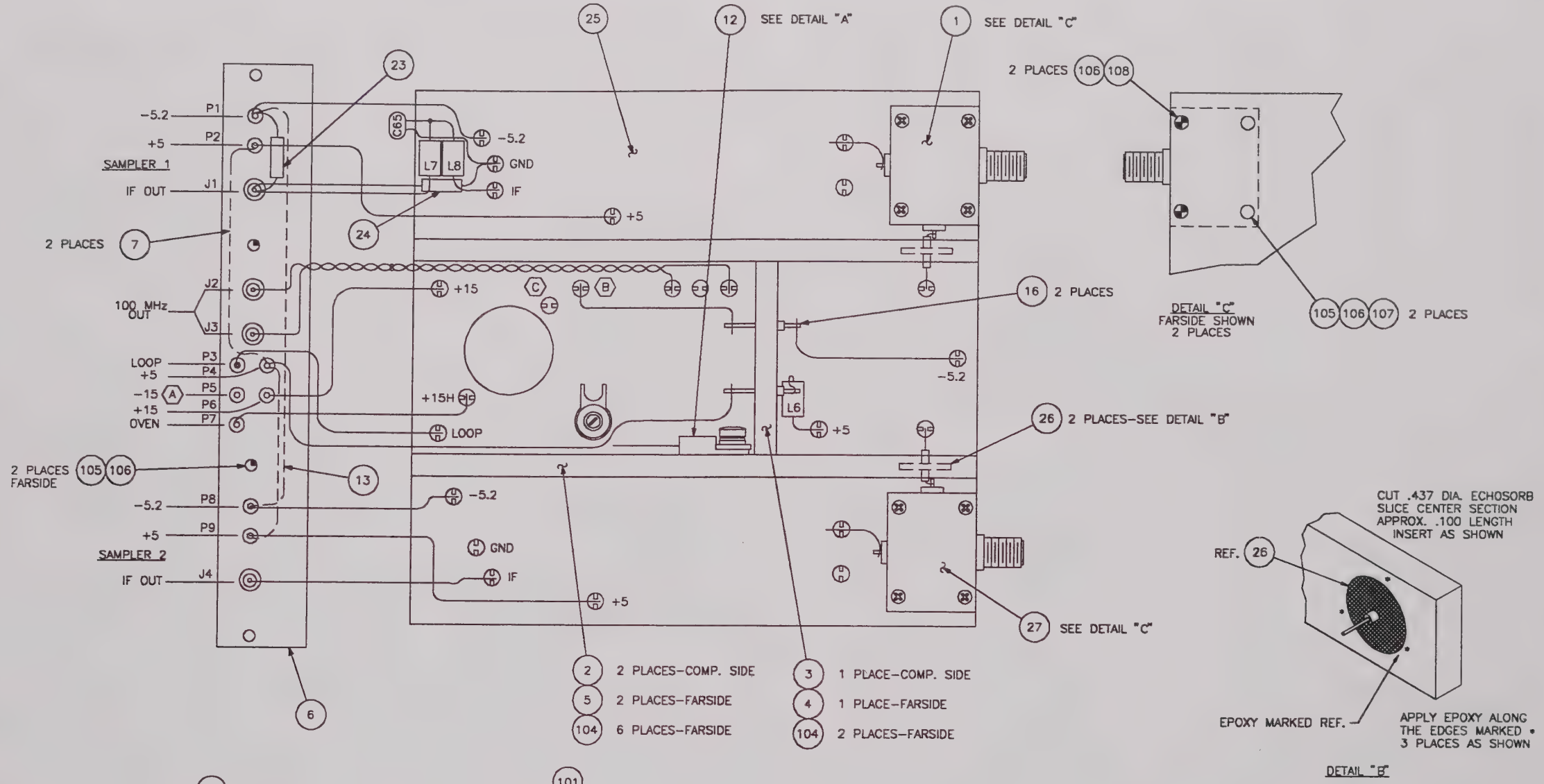

**GT9000S Functional Block Diagram**
**DWG# 120BM00350 Rev B**

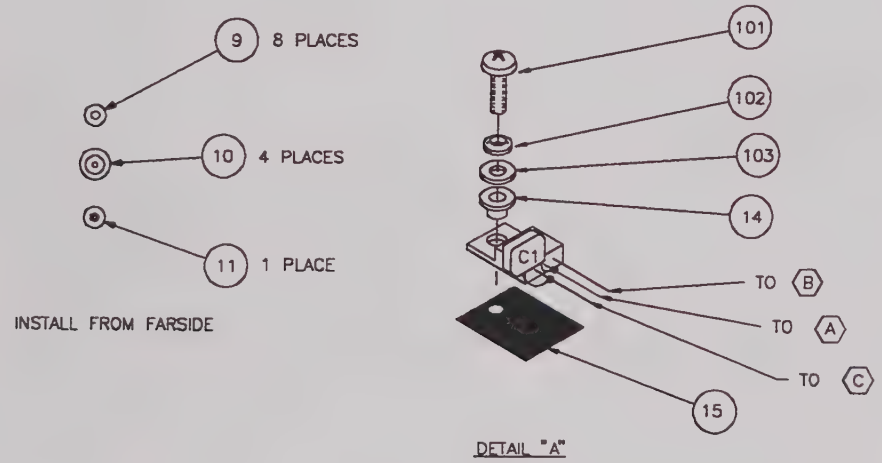



NOTE:

1. SEE SEPARATE PARTS LIST 120DA00751

**GT9000S PCB Assy Set**
**ASSY# 120DA00751 Rev C**
**Sheet 1 of 1**
**7-2**

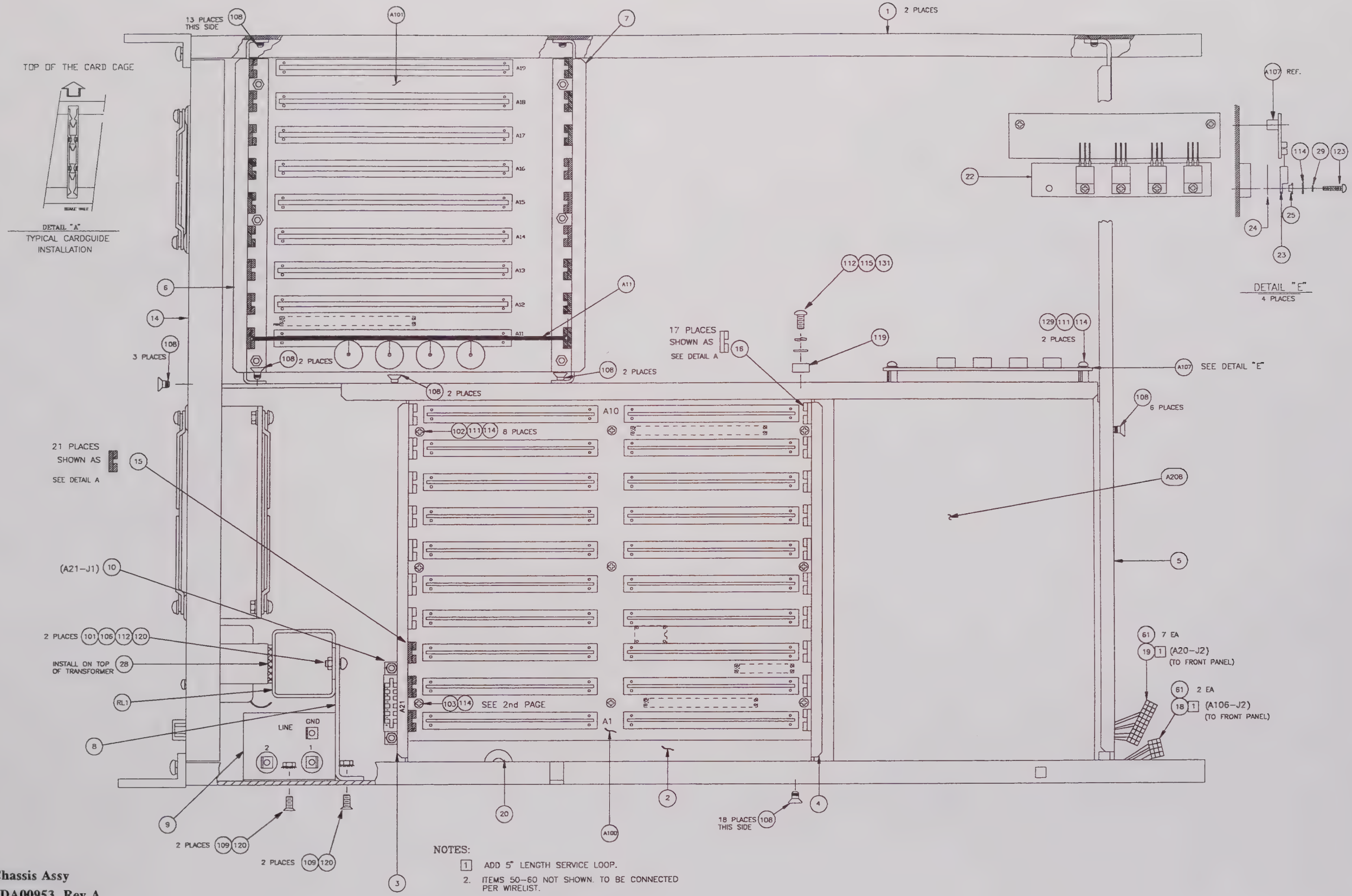



NOTES:

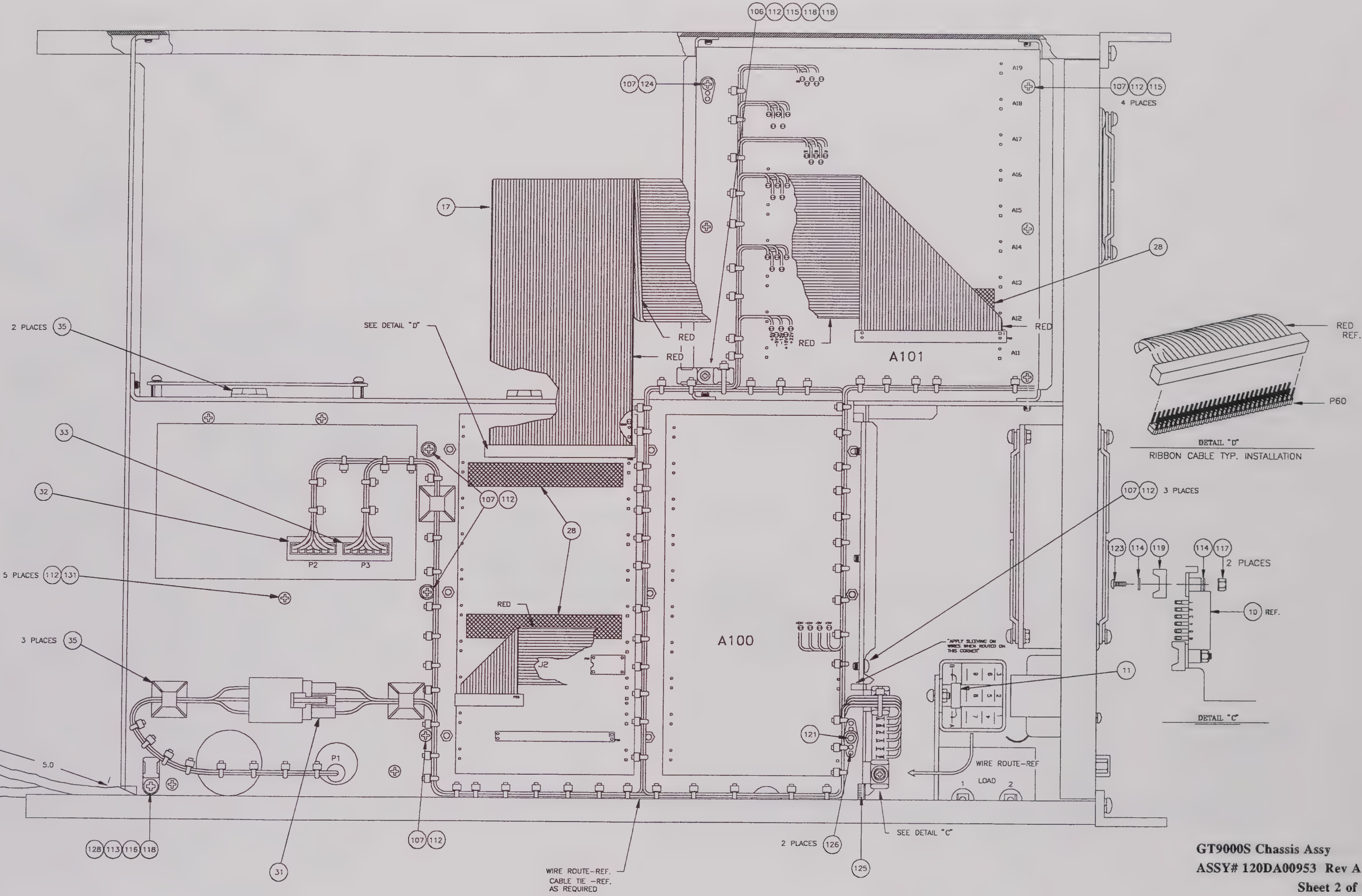
1. SEE SEPARATE PARTS LIST 120CA11500
2. ITEM 8 NOT SHOWN.

*See also:*
*100 MHz PC board, A201*

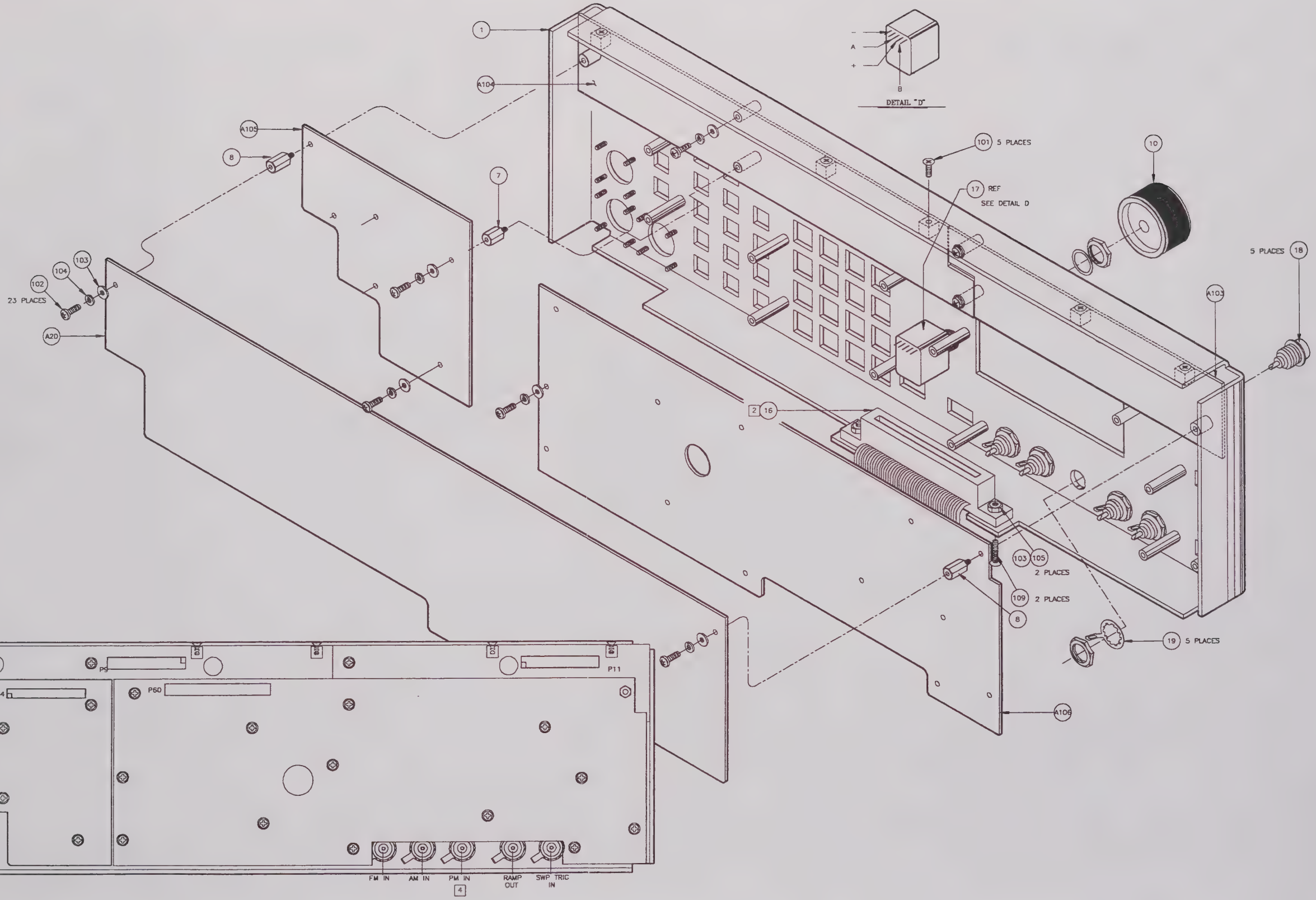



NOTES:

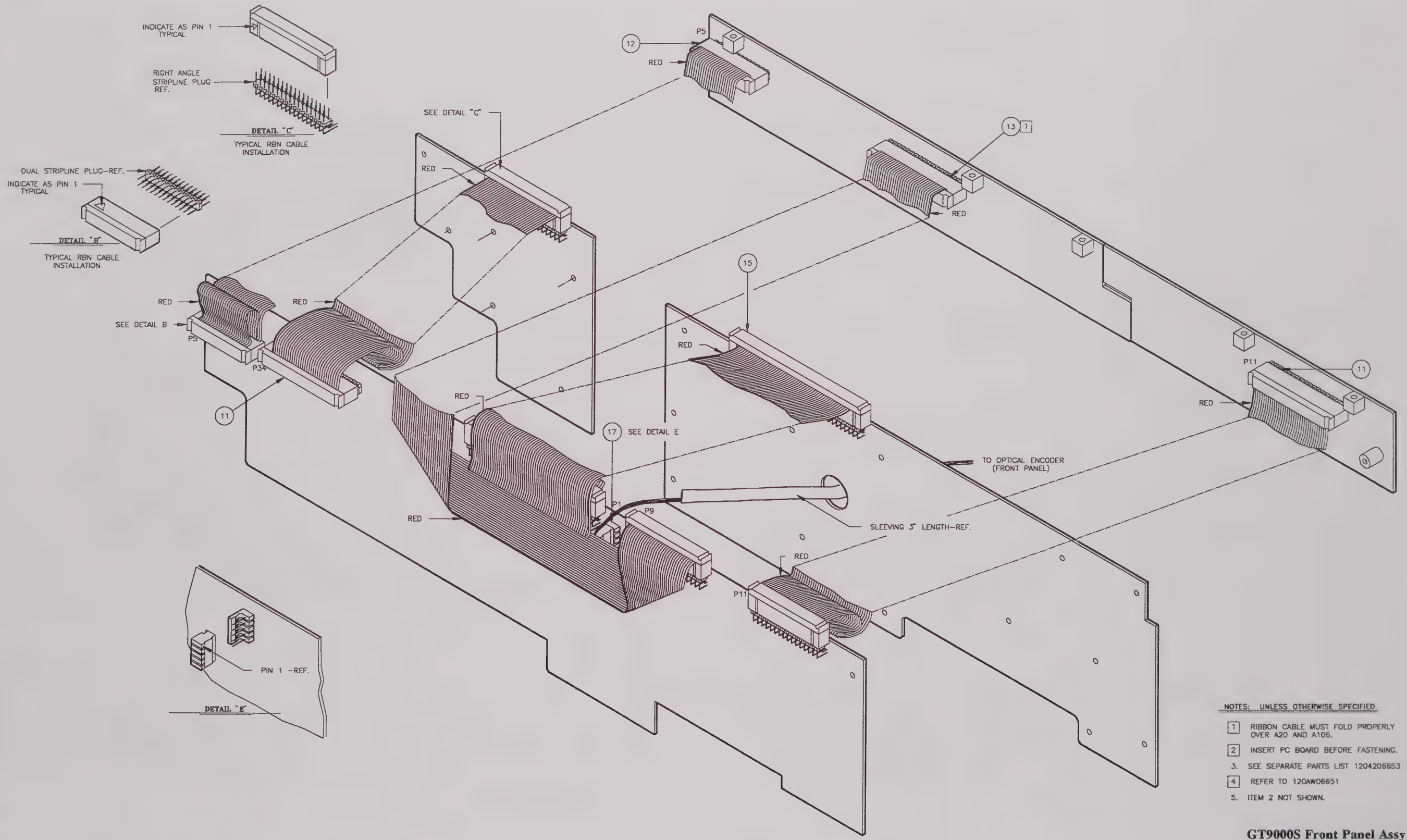
1. ADD 5" LENGTH SERVICE LOOP.
2. ITEMS 50–60 NOT SHOWN. TO BE CONNECTED PER WIRELIST.
3. ALL LEADS OF FILTER SHOULD BE COVERED BY ITEM 36. NO METAL SHOULD BE EXPOSED.




**GT9000S Chassis Assy**
**ASSY# 120DA00953 Rev A**
**Sheet 2 of 2**
**7-5**



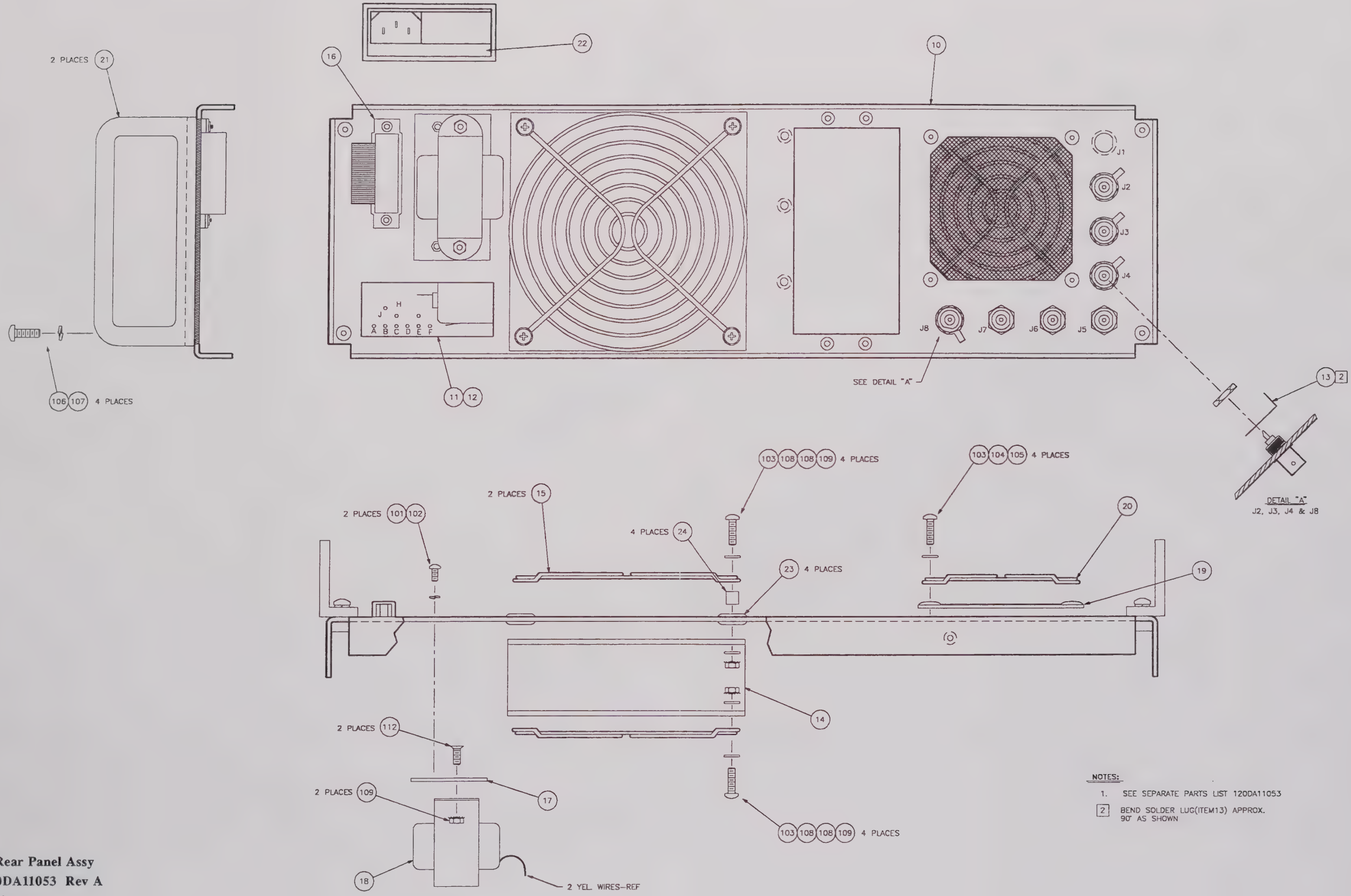

**GT9000S Front Panel Assy**
**ASSY# 1204206653 Rev A**
**Sheet 1 of 2**
**7-6**




NOTES: UNLESS OTHERWISE SPECIFIED

1. RIBBON CABLE MUST FOLD PROPERLY OVER A20 AND A106.
2. INSERT PC BOARD BEFORE FASTENING.
3. SEE SEPARATE PARTS LIST 1204206653
4. REFER TO 120AW06651
5. ITEM 2 NOT SHOWN.

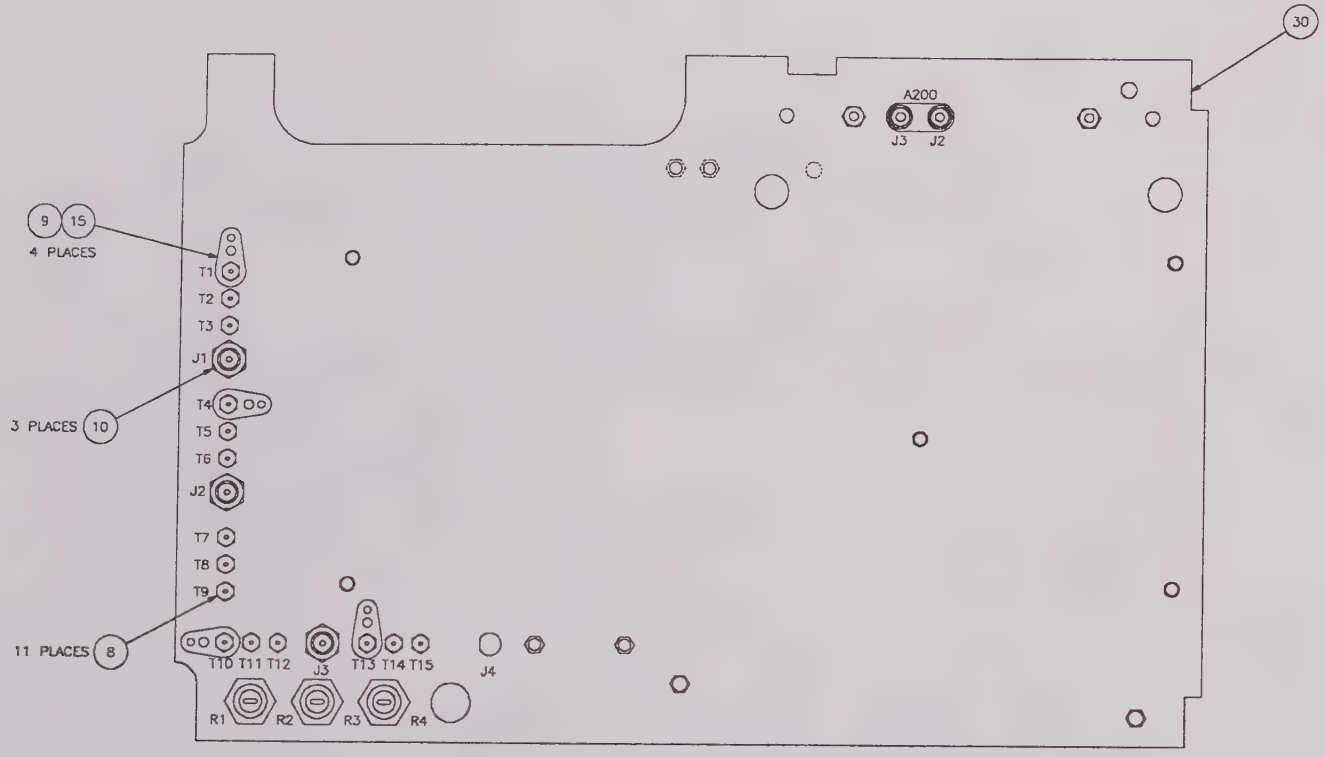
**GT9000S Front Panel Assy**
**ASSY# 1204206653 Rev A**
**Sheet 2 of 2**
**7-7**

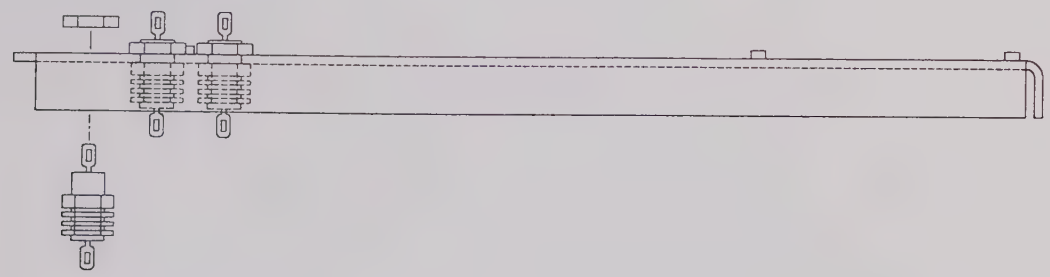


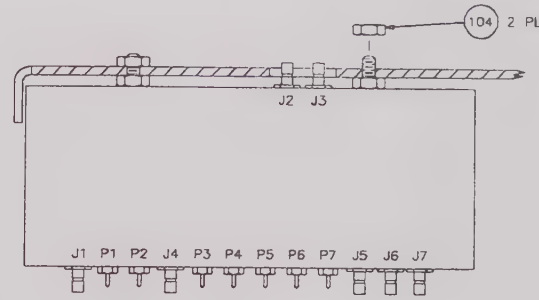

NOTES:

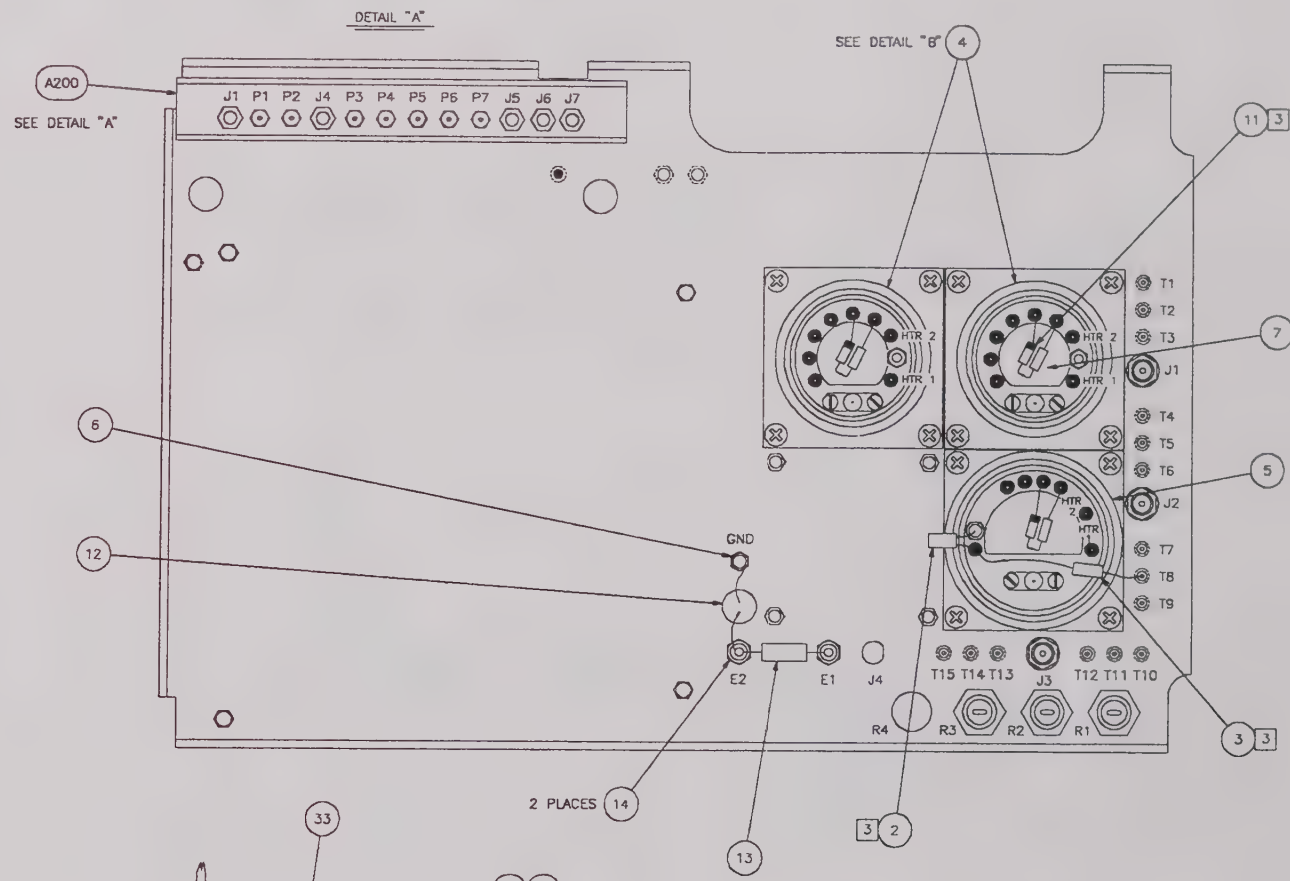
1. SEE SEPARATE PARTS LIST 120DA11053
2. BEND SOLDER LUG(ITEM13) APPROX. 90° AS SHOWN

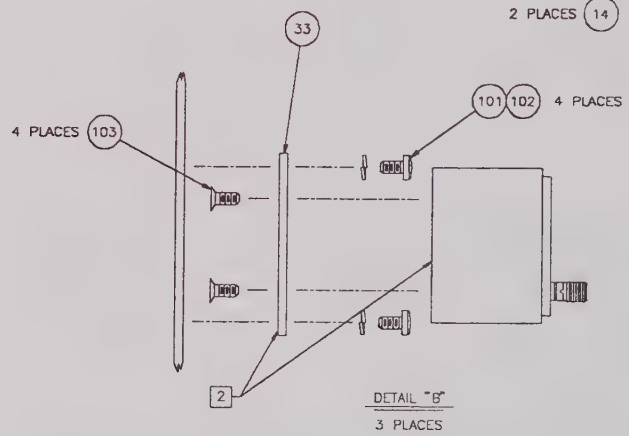
**GT9000S Rear Panel Assy**
**ASSY# 120DA11053 Rev A**
**Sheet 1 of 1**





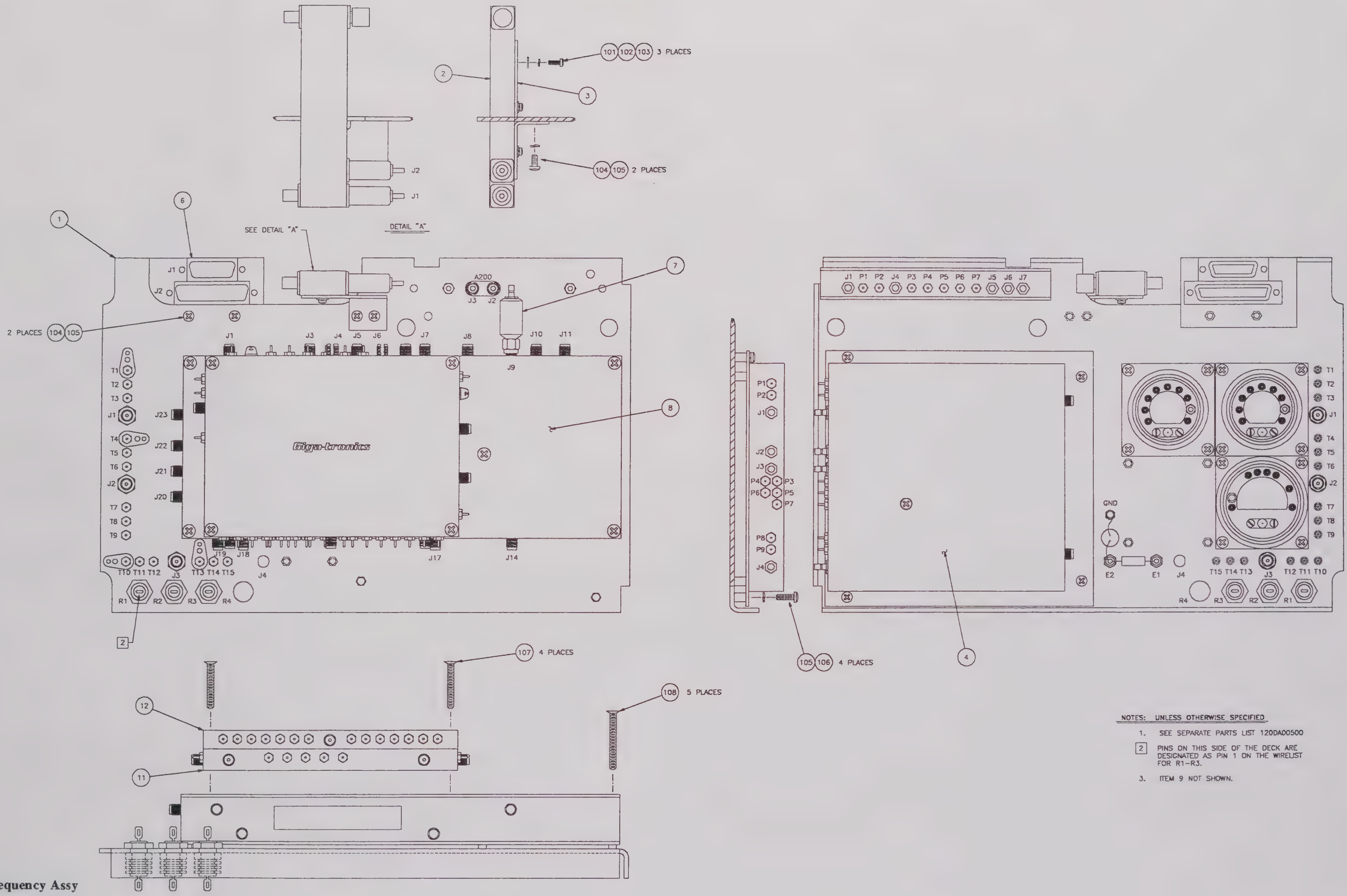




NOTES: UNLESS OTHERWISE SPECIFIED

1. SEE SEPARATE PARTS LIST 420DA46900
2. APPLY THERMAL COMPOUND TO OSC. & MOUNTING SURFACES—3 PLACES
3. APPLY HEATSHRINK TUBING OVER COMPONENTS

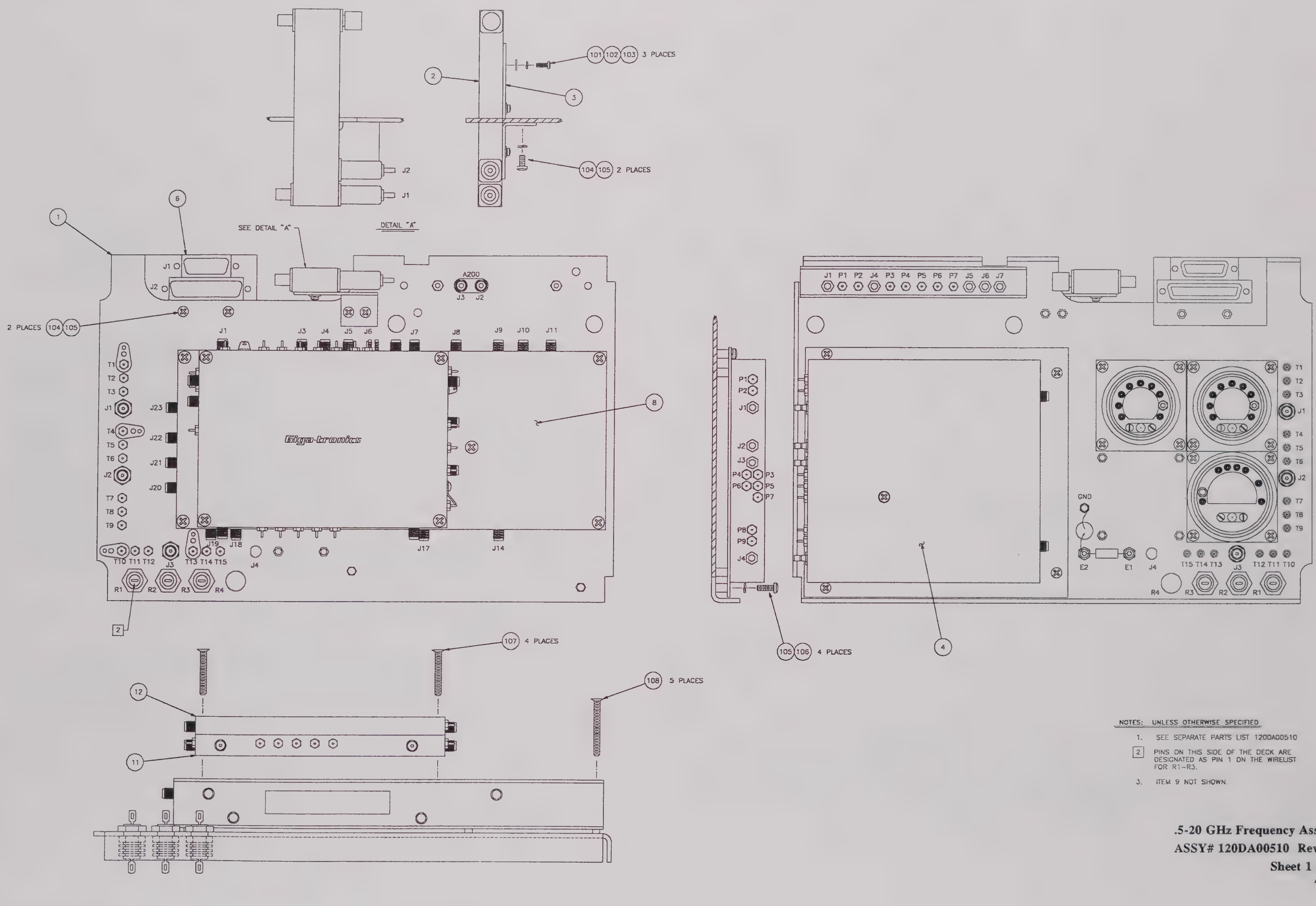
**Microwave Deck**
**ASSY# 420DA46900 Rev B**
**Sheet 1 of 1**
**7-9**




NOTES: UNLESS OTHERWISE SPECIFIED

1. SEE SEPARATE PARTS LIST 120DA00500
2. PINS ON THIS SIDE OF THE DECK ARE DESIGNATED AS PIN 1 ON THE WIRELIST FOR R1–R3.
3. ITEM 9 NOT SHOWN.

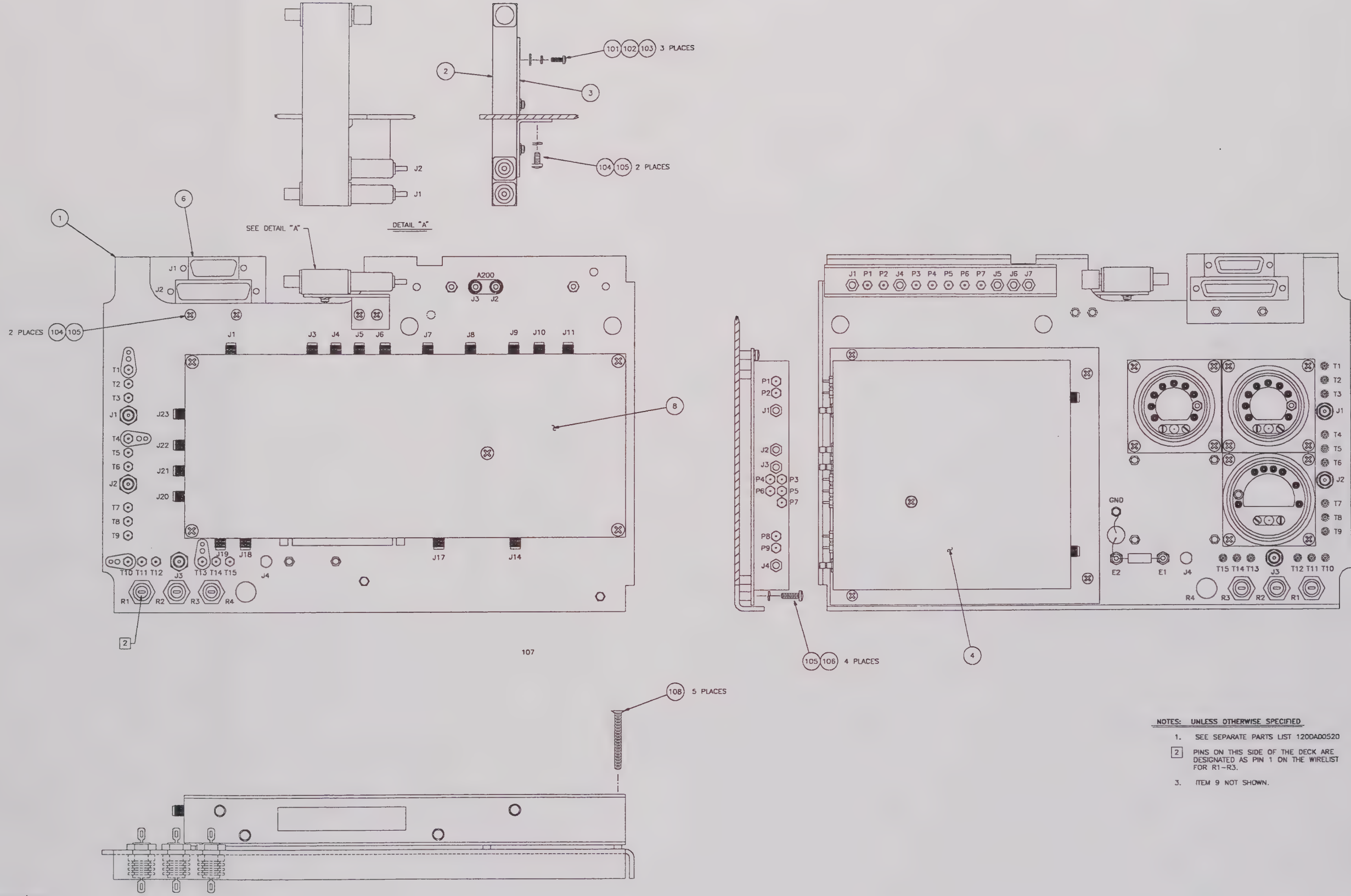
**.01-20 GHz Frequency Assy**
**ASSY# 120DA00500 Rev A**
**Sheet 1 of 1**
**7-10**




NOTES: UNLESS OTHERWISE SPECIFIED

1. SEE SEPARATE PARTS LIST 120DA00510
2. PINS ON THIS SIDE OF THE DECK ARE DESIGNATED AS PIN 1 ON THE WIRELIST FOR R1–R3.
3. ITEM 9 NOT SHOWN.

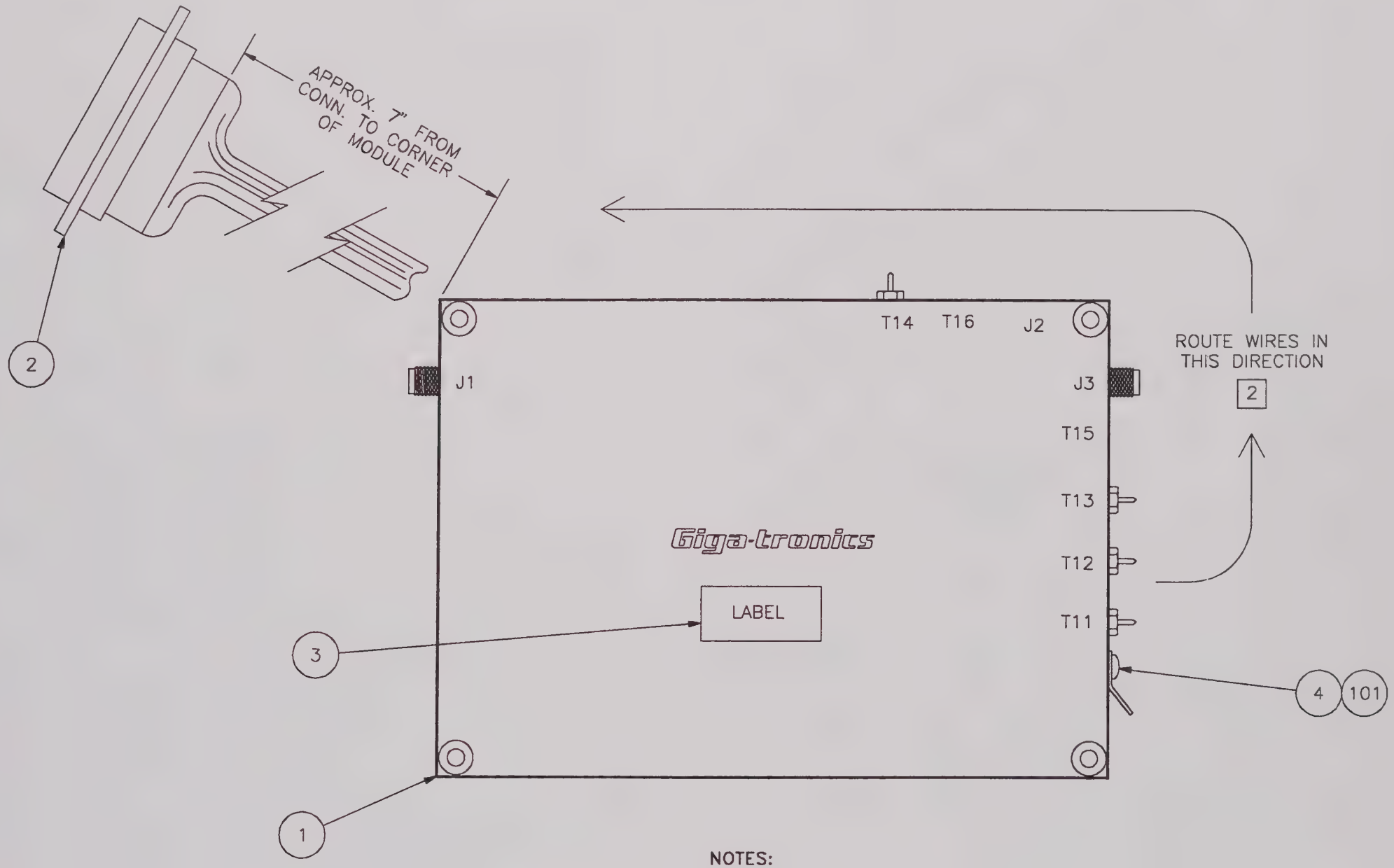
**.5-20 GHz Frequency Assy**
**ASSY# 120DA00510 Rev A**
**Sheet 1 of 1**
**7-11**




NOTES: UNLESS OTHERWISE SPECIFIED

1. SEE SEPARATE PARTS LIST 120DA00520
2. PINS ON THIS SIDE OF THE DECK ARE DESIGNATED AS PIN 1 ON THE WIRELIST FOR R1–R3.
3. ITEM 9 NOT SHOWN.

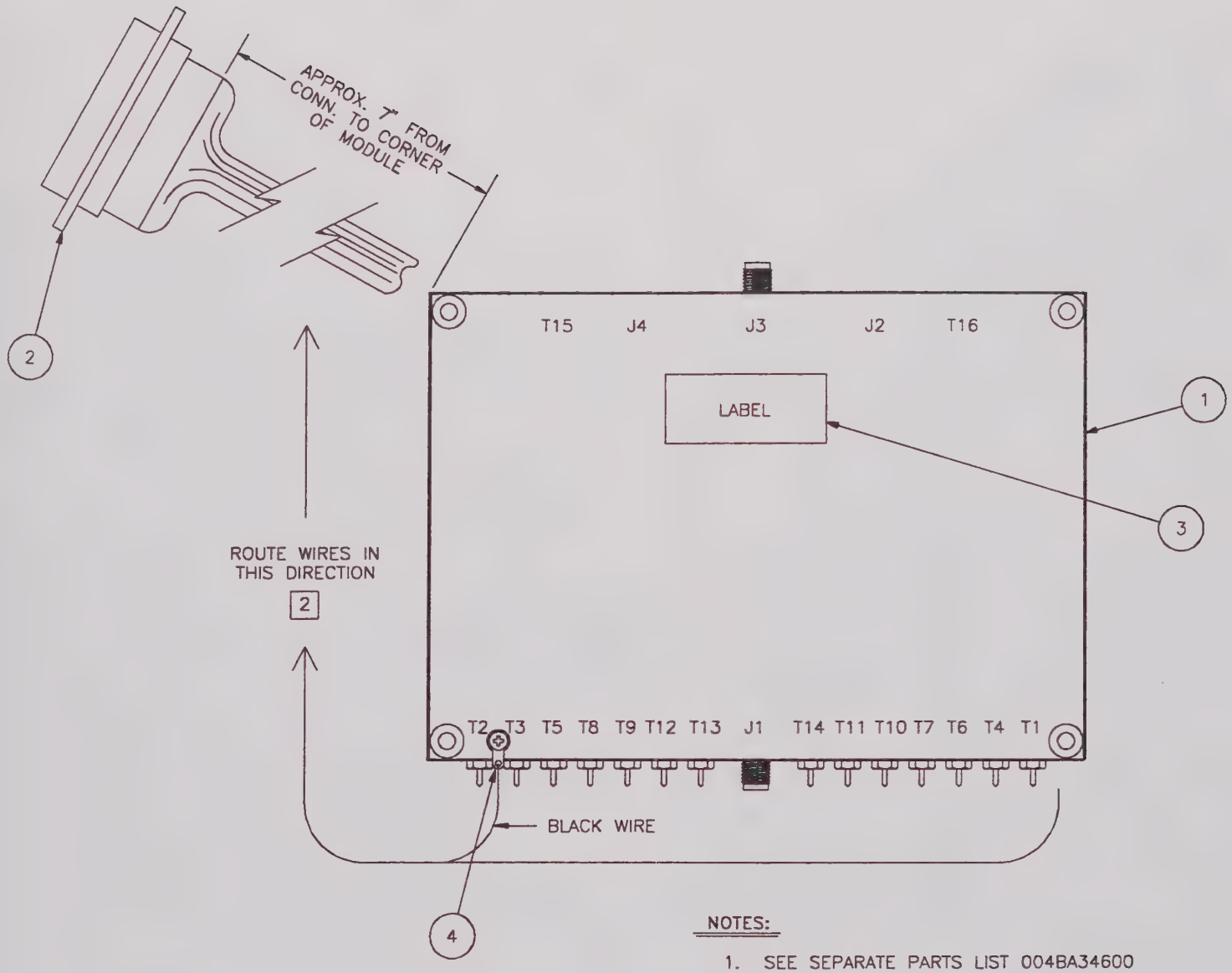
**2-20 GHz Frequency Assy**
**ASSY# 120DA00520 Rev A**
**Sheet 1 of 1**
**7-12**




NOTES:

1. SEE SEPARATE PARTS LIST 004BA34800

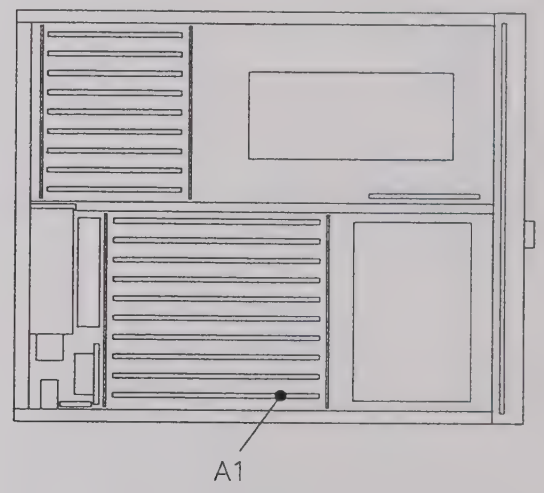
[2] INSTALL CABLE TIES AS REQUIRED.



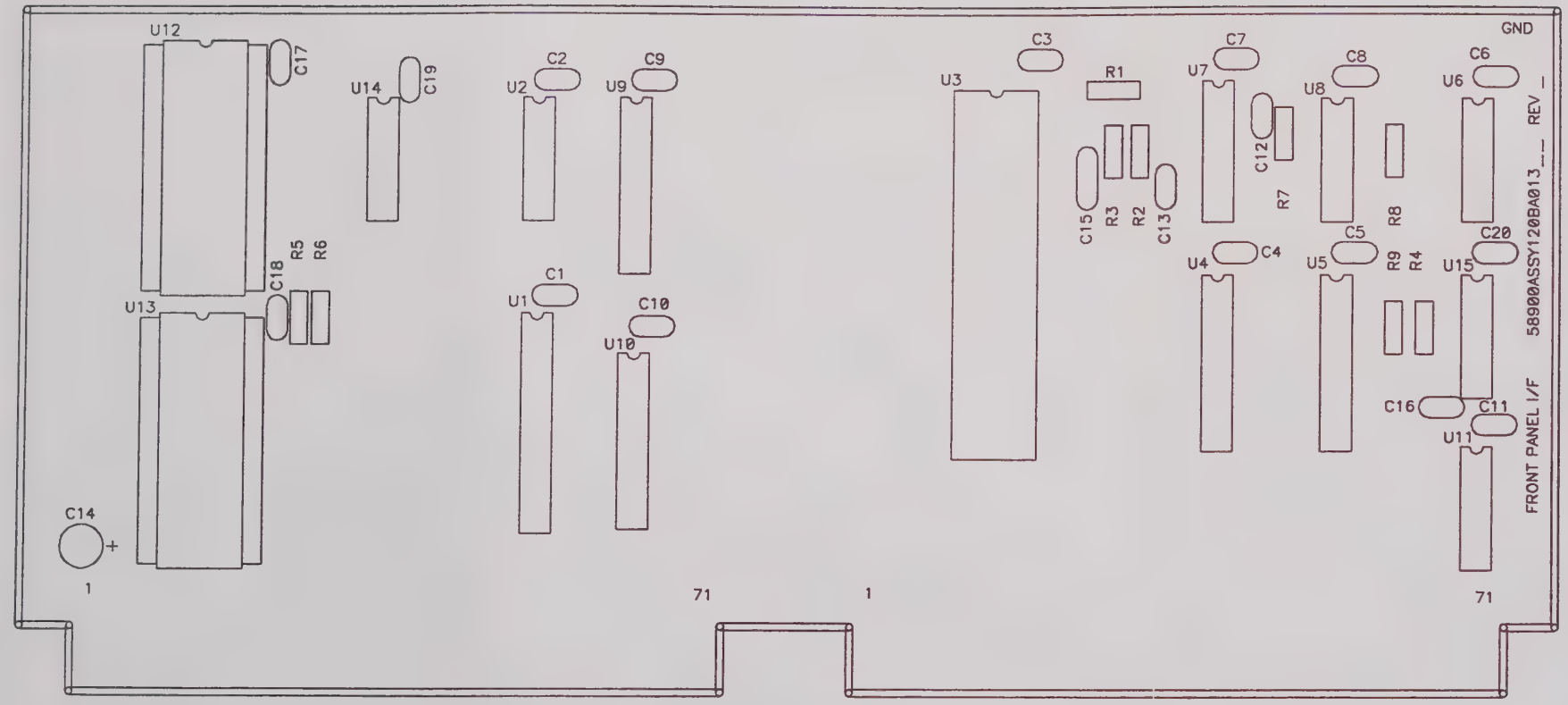

NOTES:

1. SEE SEPARATE PARTS LIST 004BA34600

[2] INSTALL CABLE TIES AS REQUIRED.




**Front Panel Interface (A1)**
**ASSY# 120BA01300 Rev C**
**Sheet 1 of 4**
**7-A1-1**




**FRONT PANEL INTERFACE -- PC ASSY A1**

As the name implies, the Front Panel Interface PCA provides for all interface between the front panel and computer. This includes front panel data entry (in the form of keystrokes or knob movement) as well as front panel data display.

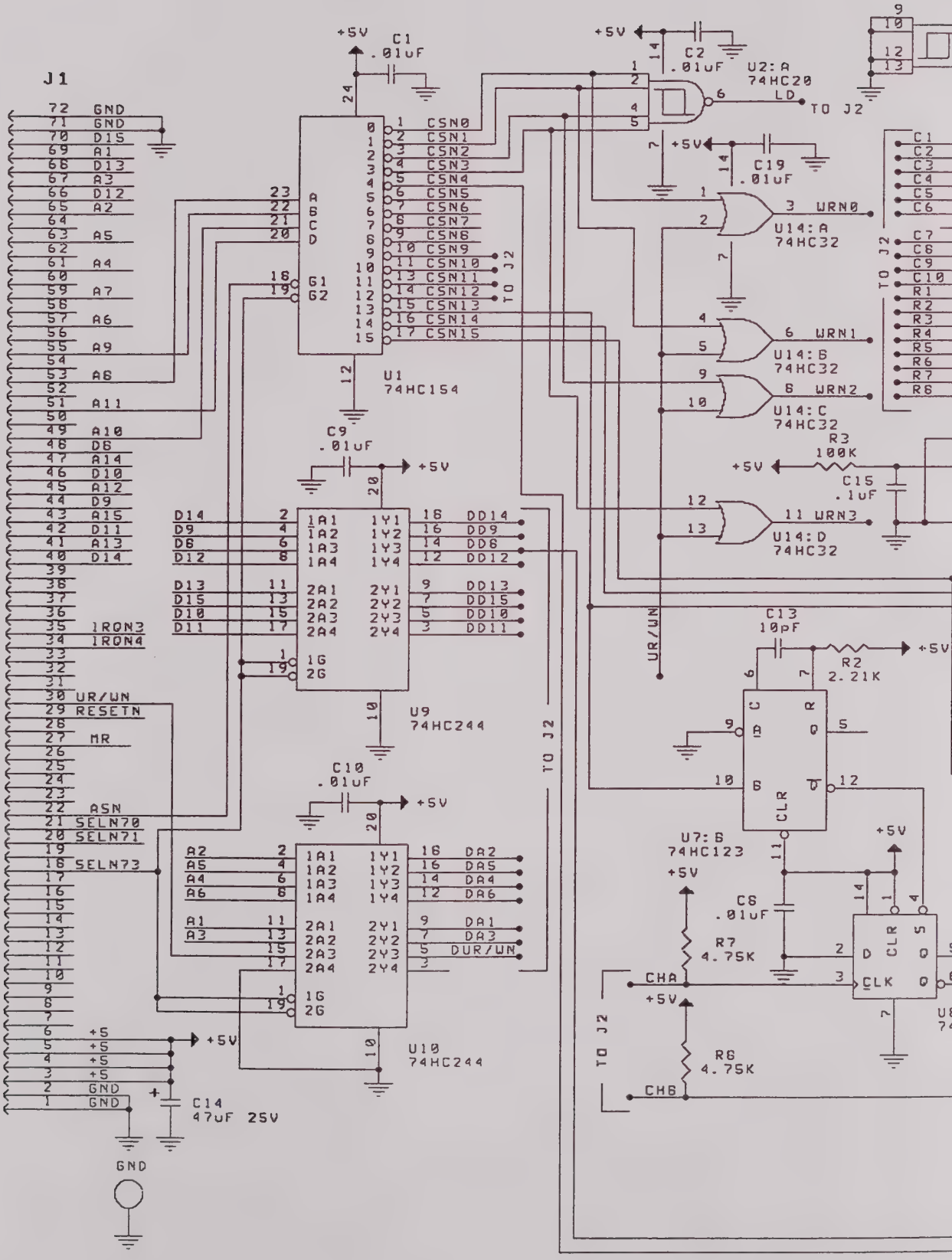
U1, a 4 to 16 decoder, decodes the chip selects for the different front panel displays and interfaces. U14 A thru D provide the individual chip selects for the front panel 'Entry Menu' displays, which are gated by the UR/UN line. U2 A provides a load signal for loading data to these displays.

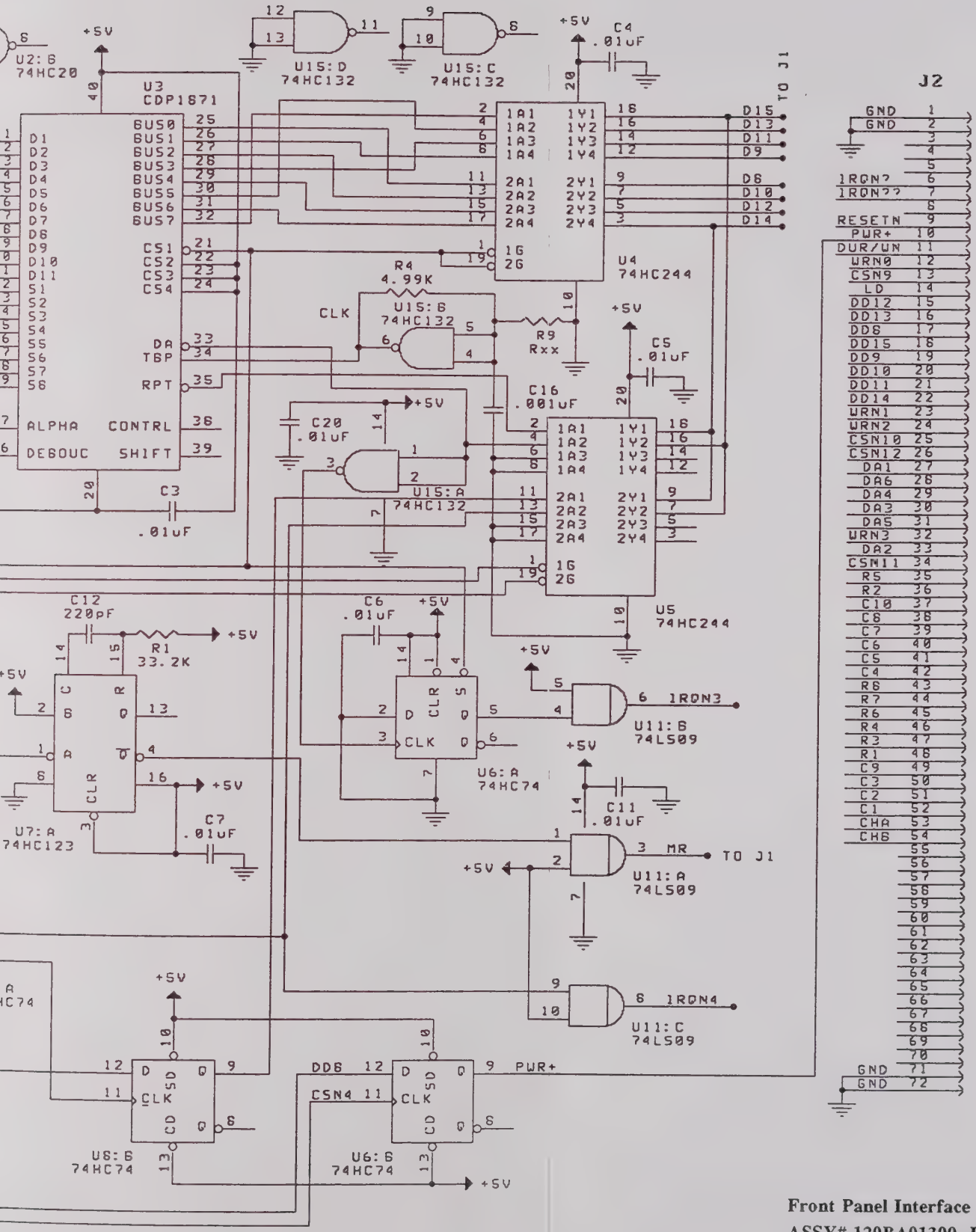
The U3 Keyboard decoder, where D1-11 represent columns and S1-8 are rows, identifies keys pressed and outputs information to the computer bus via U5 buffer. U15 B provides a clock circuit for scanning the keyboard. Whenever keyboard is active, U15 A detects the data available line and causes an interrupt to be generated by U6 A, U11 B. When the computer responds with a chip select from U1 indicating that the keyboard can be read, the interrupt is cleared via U6 A. U7 A and U11 A activate the memory ready line which slows the CPU as required for read cycles to take place.

Any time the front panel knob is turned, the optical decoder generates pulses which are seen at U8 A and B; the flip flops of U8 are set up such that the output at U8-9 indicates which way the knob was turned. U8-5 flips, generating an interrupt via U11 C. When the computer selects the knob to be read a chip select is received at U7-B, from U1, which clears the interrupt.

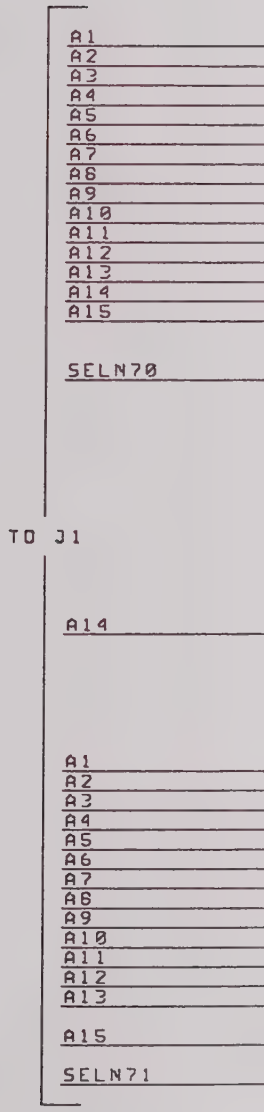
U4, U5, U9, and U18 provide buffers for computer bus interface.

On the next page of the diagram, U12 is the 'CONFIGURATION' ROM, which stores the information about the unit such as its frequency range and what options it has. It is also programmed to hold various characterization data. U13 is a non-volatile RAM chip which is used to store the current unit settings when the power is turned off. It is also used to store multiple unit setups in memory locations 0 thru 9.


J1
72 GND
71 GND
70 D15
69 A1
68 D13
67 A3
66 D12
65 A2
64
63 A5
62
61 A4
60
59 A7
58
57 A6
56
55 A9
54
53 A8
52
51 A11
50
49 A10
48 D8
47 A14
46 D10
45 A12
44 D9
43 A15
42 D11
41 A13
40 D14
39
38
37
36
35 IRQN3
34 IRQN4
33
32
31
30 UR/WN
29 RESETN
28
27 MR
26
25
24
23
22 ASN
21 SELN70
20 SELN71
19
18 SELN73
17
16
15
14
13
12
11
10
9
8
7
6 +5
5 +5
4 +5
3 +5
2 GND
1 GND
+5V
C1
.01uF
C14
47uF 25V
GND
U1
74HC154
CSN0
CSN1
CSN2
CSN3
CSN4
CSN5
CSN6
CSN7
CSN8
CSN9
CSN10
CSN11
CSN12
CSN13
CSN14
CSN15
TO J2
C9
.01uF
U9
74HC244
D14
D9
D8
D12
D13
D15
D10
D11
DD14
DD9
DD8
DD12
DD13
DD15
DD10
DD11
C10
.01uF
U10
74HC244
A2
A5
A4
A6
A1
A3
DA2
DA5
DA4
DA6
DA1
DA3
DUR/WN
C2
.01uF
U2:A
74HC20
LD
TO J2
C19
.01uF
U14:A
74HC32
WRN0
U14:B
74HC32
WRN1
U14:C
74HC32
WRN2
R3
100K
C15
.1uF
U14:D
74HC32
WRN3
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
R1
R2
R3
R4
R5
R6
R7
R8
C13
10pF
R2
2.21K
U7:B
74HC123
C8
.01uF
R7
4.75K
CHA
R8
4.75K
CHB
UR/WN

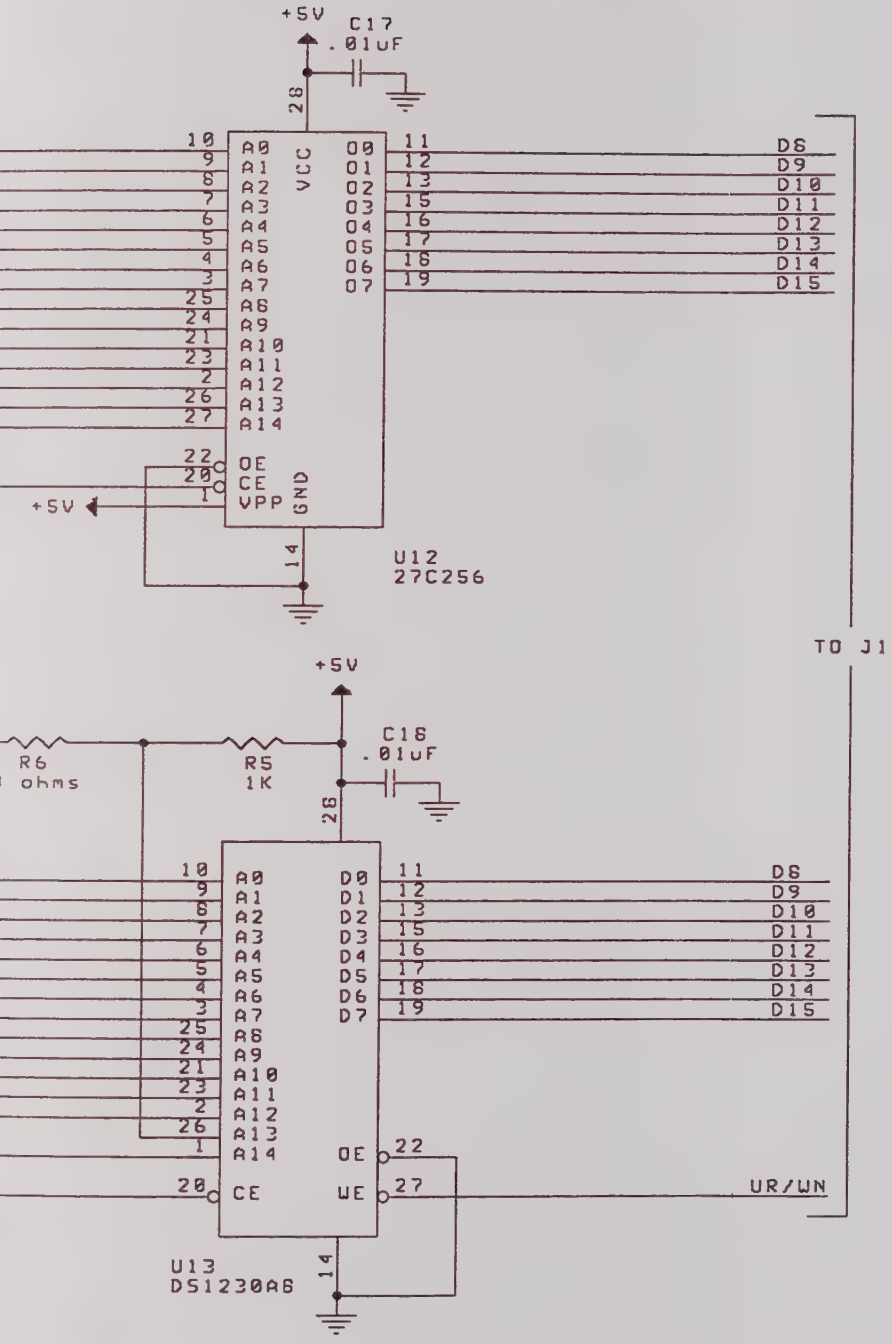



**Front Panel Interface (A1)**
**ASSY# 120BA01300 Rev C**
**Sheet 3 of 4**
**7-A1-3**

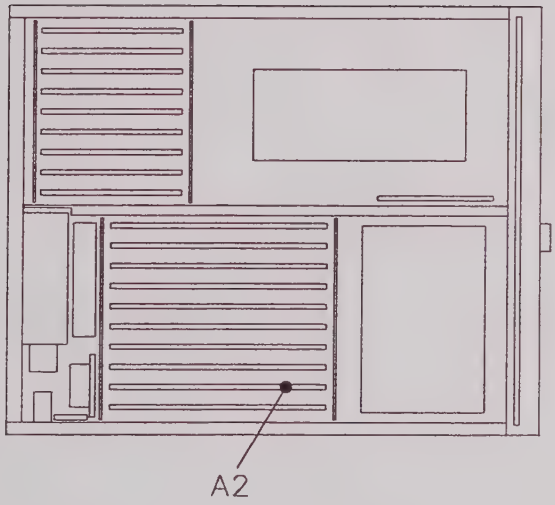



**NOTES: UNLESS OTHERWISE SPECIFIED**

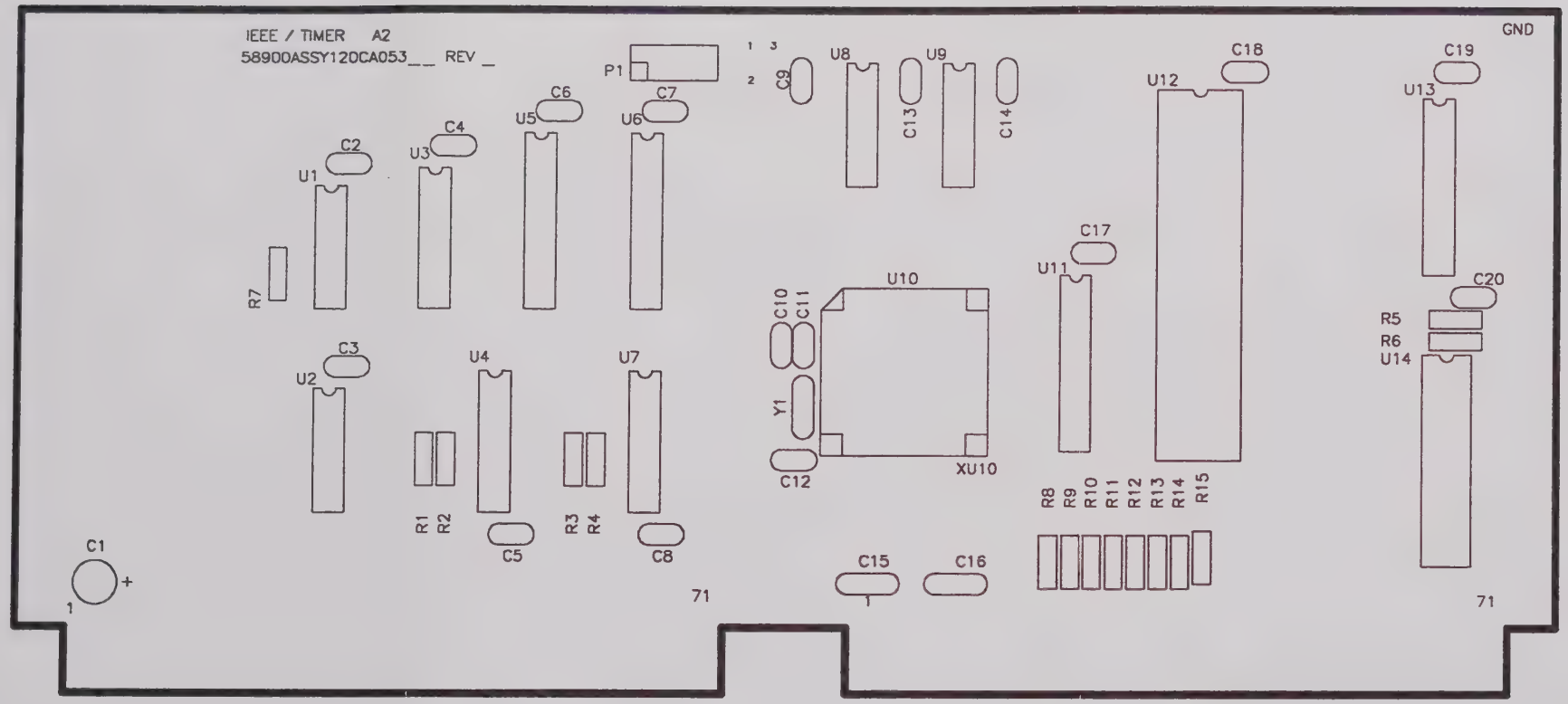
1.) CAPACITOR VALUES ARE IN uF
2.) RESISTOR VALUES ARE IN OHMS
3.) RESISTORS ARE 1/4W, 1%




**Front Panel Interface (A1)**
**ASSY# 120BA01300 Rev C**
**Sheet 4 of 4**
**7-A1-4**




**IEEE/Timer (A2)**
**ASSY# 120BA05300 Rev B**
**Sheet 1 of 4**
**7-A2-1**




**IEEE / TIMER -- PC ASSY A2**

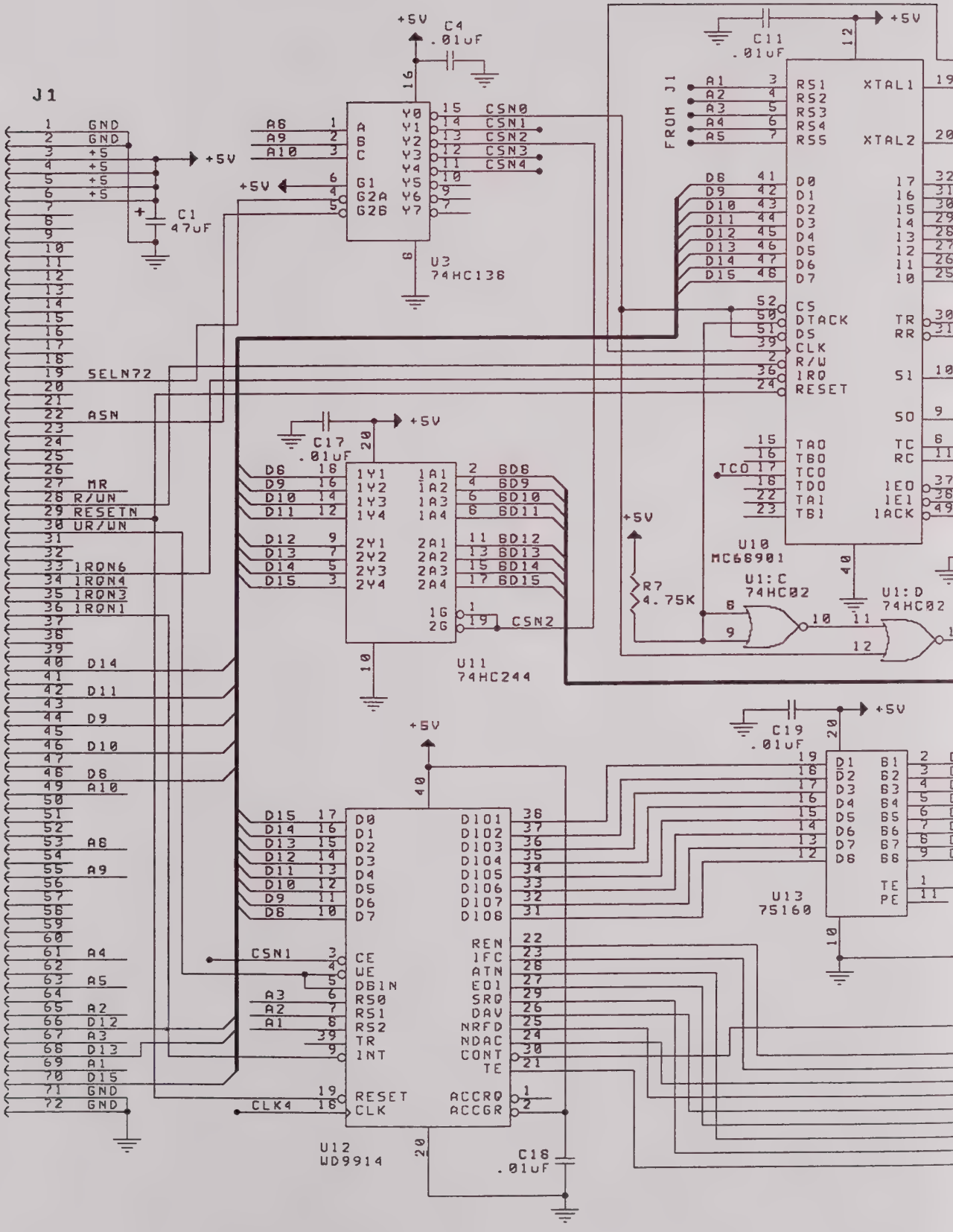
U10 is the interrupt timer for the CPU. It is clocked by the oscillator consisting of Y1, C10, and C12.

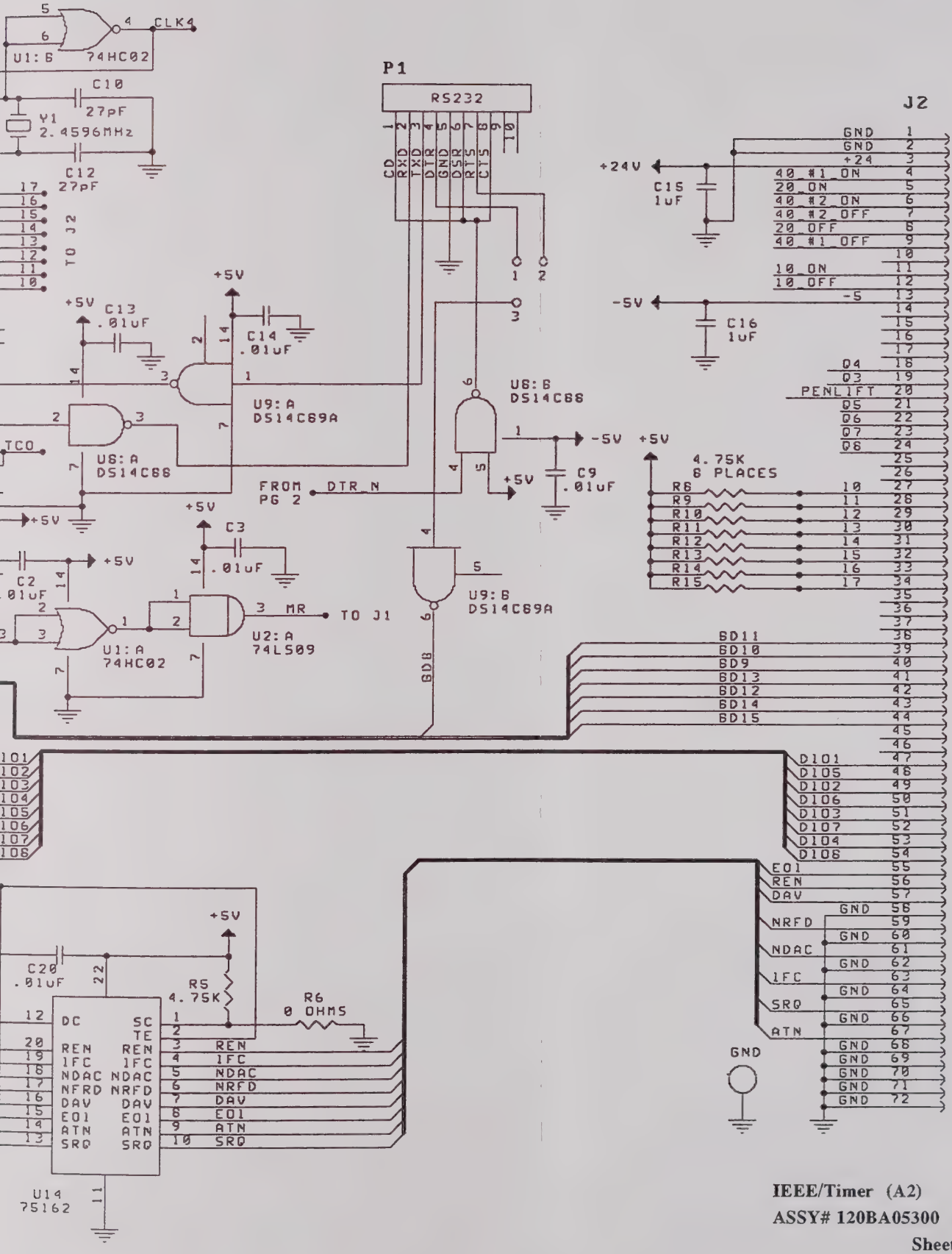
U8 and U9 provide for the addition of an RS-232 interface feature which is not yet implemented.

U12, U13, and U14 operate the instrument's remote control interface, which conforms to the IEEE-488 standard.

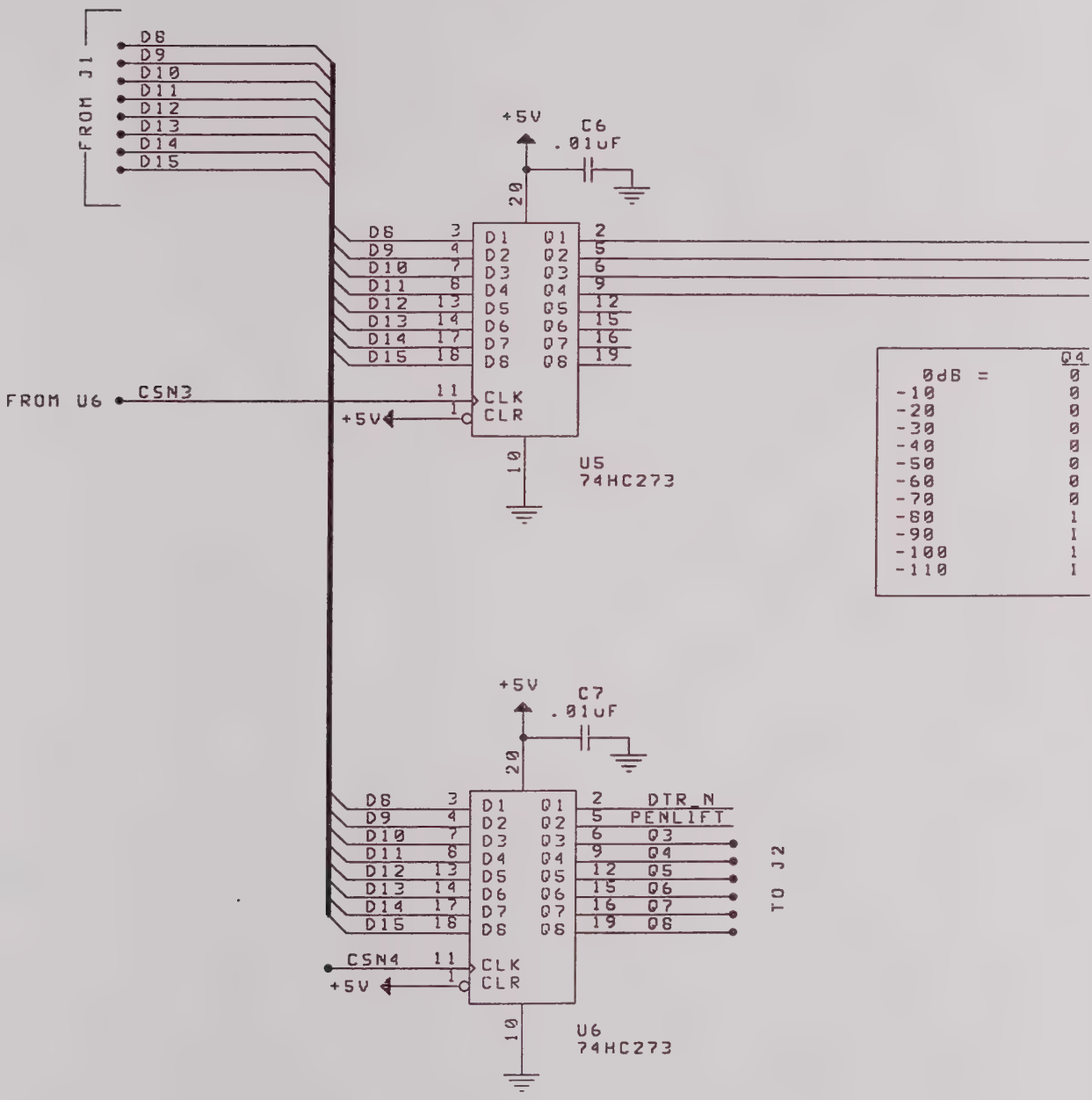
U3 decodes chip selects for the circuits on this board. U11 acts as a buffer for certain computer bus lines.

On sheet 4, the outputs of flip-flop U5 are used to latch attenuator data; U7 and U4 provide the proper logic levels for driving the attenuator. The outputs of flip flop U6 are used to latch miscellaneous computer control lines.


J1
1 GND
2 GND
3 +5
4 +5
5 +5
6 +5
19 SELN72
22 ASN
27 MR
28 R/WN
29 RESETN
30 WR/WN
33 IRQN6
34 IRQN4
35 IRQN3
36 IRQN1
40 D14
42 D11
44 D9
46 D10
48 D8
49 A10
53 A8
55 A9
61 A4
63 A5
65 A2
66 D12
67 A3
68 D13
69 A1
70 D15
71 GND
72 GND
+5V
C1
47uF
C4
.01uF
U3
74HC138
A8
A9
A10
G1
G2A
G2B
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
CSN0
CSN1
CSN2
CSN3
CSN4
C11
.01uF
FROM J1
A1
A2
A3
A4
A5
RS1
RS2
RS3
RS4
RS5
XTAL1
XTAL2
D8
D9
D10
D11
D12
D13
D14
D15
D0
D1
D2
D3
D4
D5
D6
D7
CS
DTACK
DS
CLK
R/W
IRQ
RESET
TR
RR
SI
SO
TC
RC
TAO
TBO
TCO
TDO
TA1
TB1
IEO
IE1
IACK
U10
MC68901
C17
.01uF
U11
74HC244
1Y1
1Y2
1Y3
1Y4
2Y1
2Y2
2Y3
2Y4
1A1
1A2
1A3
1A4
2A1
2A2
2A3
2A4
1G
2G
BD8
BD9
BD10
BD11
BD12
BD13
BD14
BD15
R7
4.75K
U1:C
74HC02
U1:D
74HC02
C19
.01uF
U13
75160
D1
D2
D3
D4
D5
D6
D7
D8
B1
B2
B3
B4
B5
B6
B7
B8
TE
PE
U12
WD9914
D0
D1
D2
D3
D4
D5
D6
D7
D101
D102
D103
D104
D105
D106
D107
D108
CE
WE
DBIN
RS0
RS1
RS2
TR
INT
REN
IFC
ATN
EOI
SRQ
DAV
NRFD
NDAC
CONT
TE
RESET
CLK
ACCRQ
ACCGR
CLK4
C18
.01uF

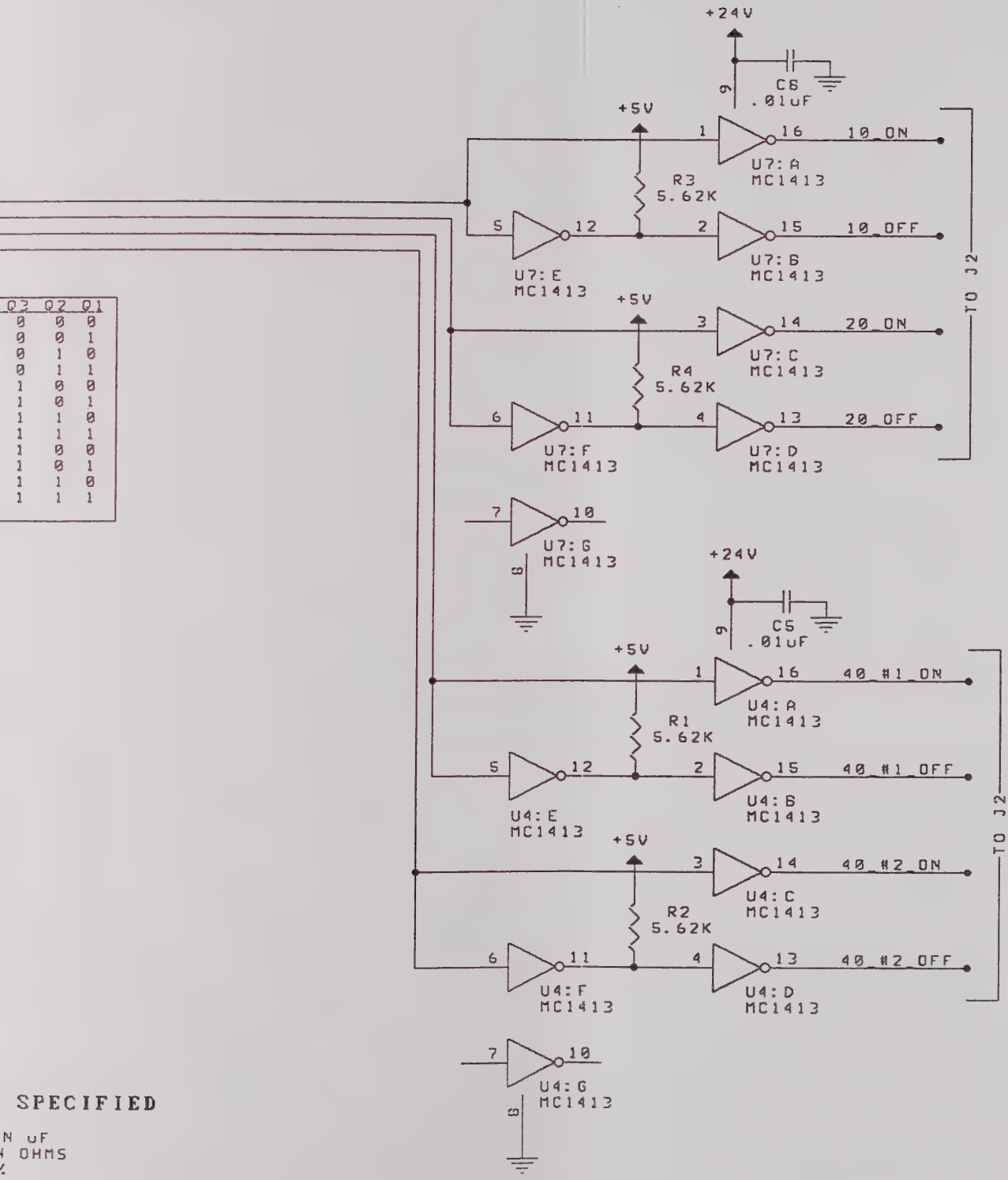



**IEEE/Timer (A2)**
**ASSY# 120BA05300 Rev B**
**Sheet 3 of 4**
**7-A2-3**




**NOTES: UNLESS OTHERWISE**

1. CAPACITOR VALUES ARE
2. RESISTOR VALUES ARE
3. RESISTORS ARE 1/4W, 1

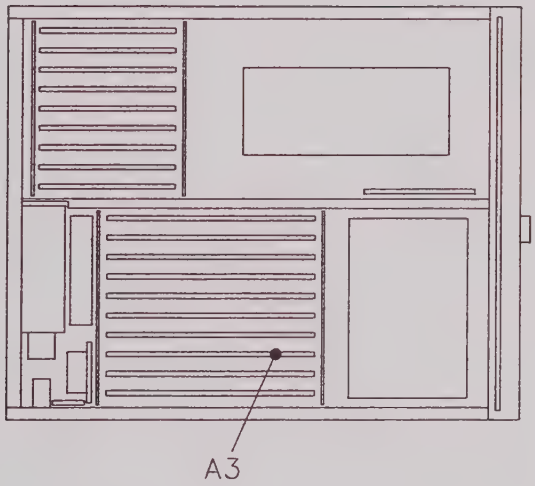



| Q3 | Q2 | Q1 |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |
| 1 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |
| 1 | 1 | 1 |

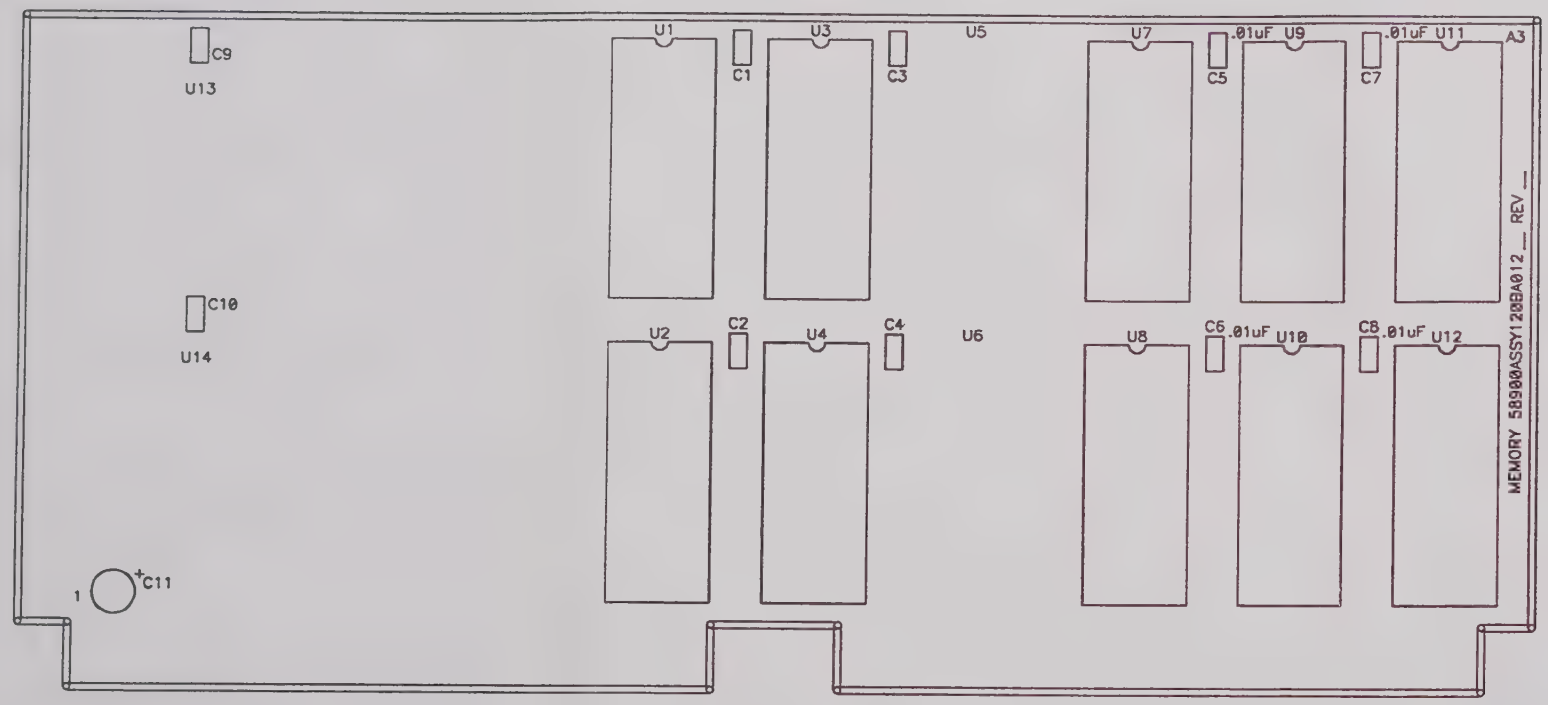
SPECIFIED

N uF
OHMS
%

**IEEE/Timer (A2)**
**ASSY# 120BA05300 Rev B**
**Sheet 4 of 4**
**7-A2-4**




**Memory (A3)**
**ASSY# 120BA01200 Rev C**
**Sheet 1 of 3**
**7-A3-1**

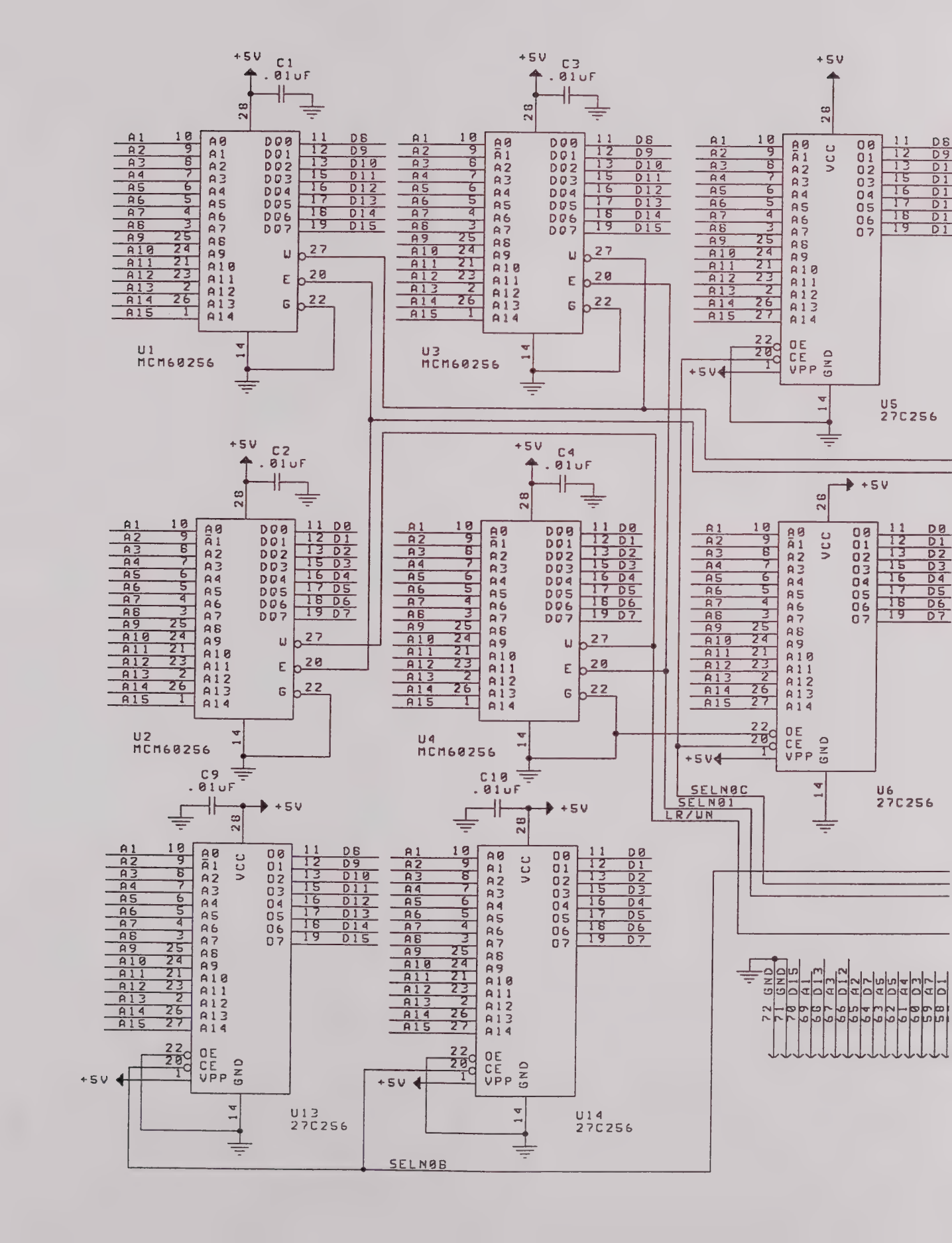


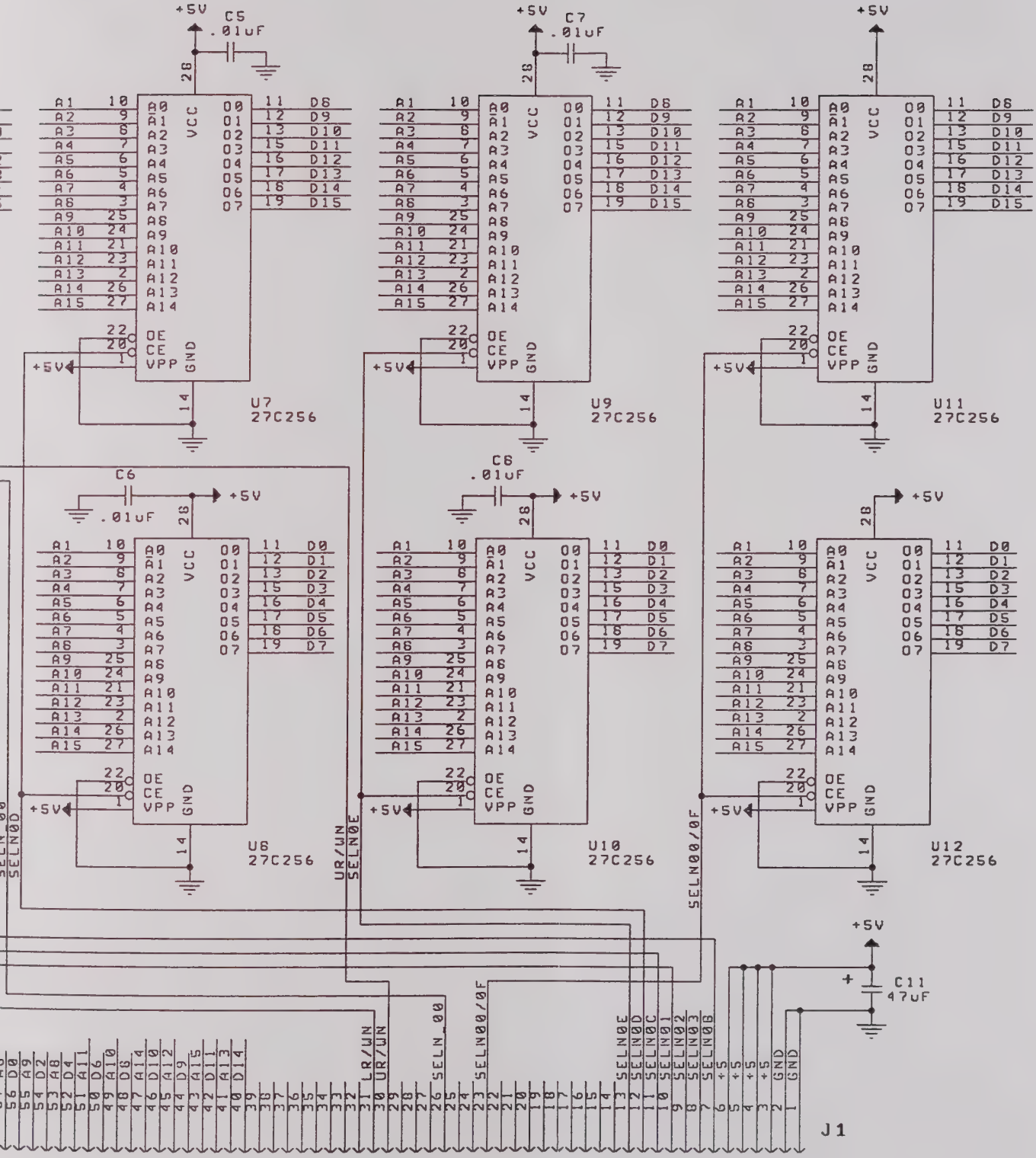

**MEMORY -- PC ASSY A3**

U1 thru U4 are RAMS, used by the CPU for temporary data storage.

U5 thru U14 are ROMs, used to store the instrument's operational software.

The RAMS and ROMs are 32K X 8 and are used in pairs (one for even addresses and the other used for odd), in order to simulate 32K X 16's as required by the 16 bit data bus.


+5V
C1
.01uF
U1
MCM60256
C3
.01uF
U3
MCM60256
U5
27C256
C2
.01uF
U2
MCM60256
C4
.01uF
U4
MCM60256
U6
27C256
C9
.01uF
C10
.01uF
U13
27C256
U14
27C256
SELN0C
SELN01
LR/WN
SELN0B
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
D00
D01
D02
D03
D04
D05
D06
D07
W
E
G
VCC
GND
OE
CE
VPP

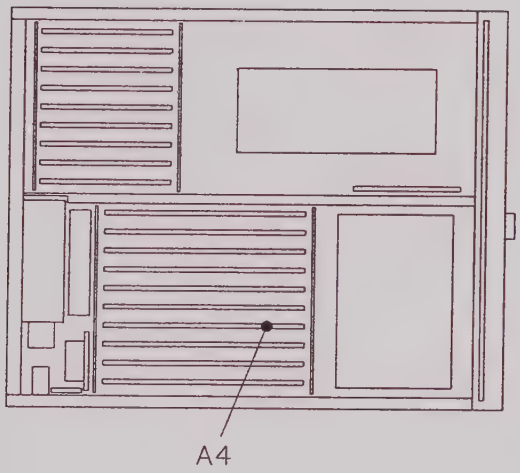



**Memory (A3)**

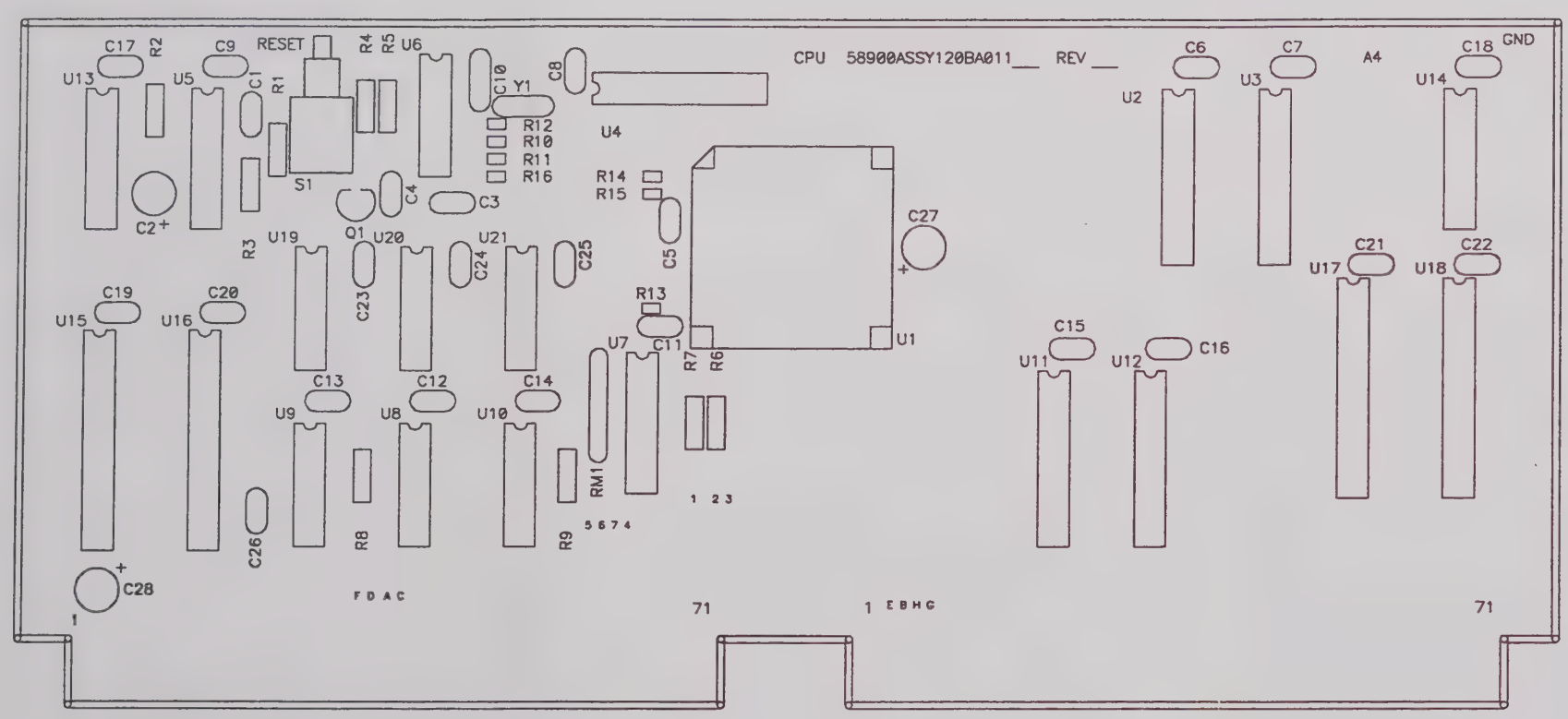
**ASSY# 120BA01200 Rev C**

**Sheet 3 of 3**

**7-A3-3**




**CPU (A4)**
**ASSY# 120BA01100 Rev C**
**Sheet 1 of 4**
**7-A4-1**




**CPU -- PC ASSY A4**

Y1, C3, C4, Q1 and U6 A provide the clock for U1, the 68000 microprocessor chip.

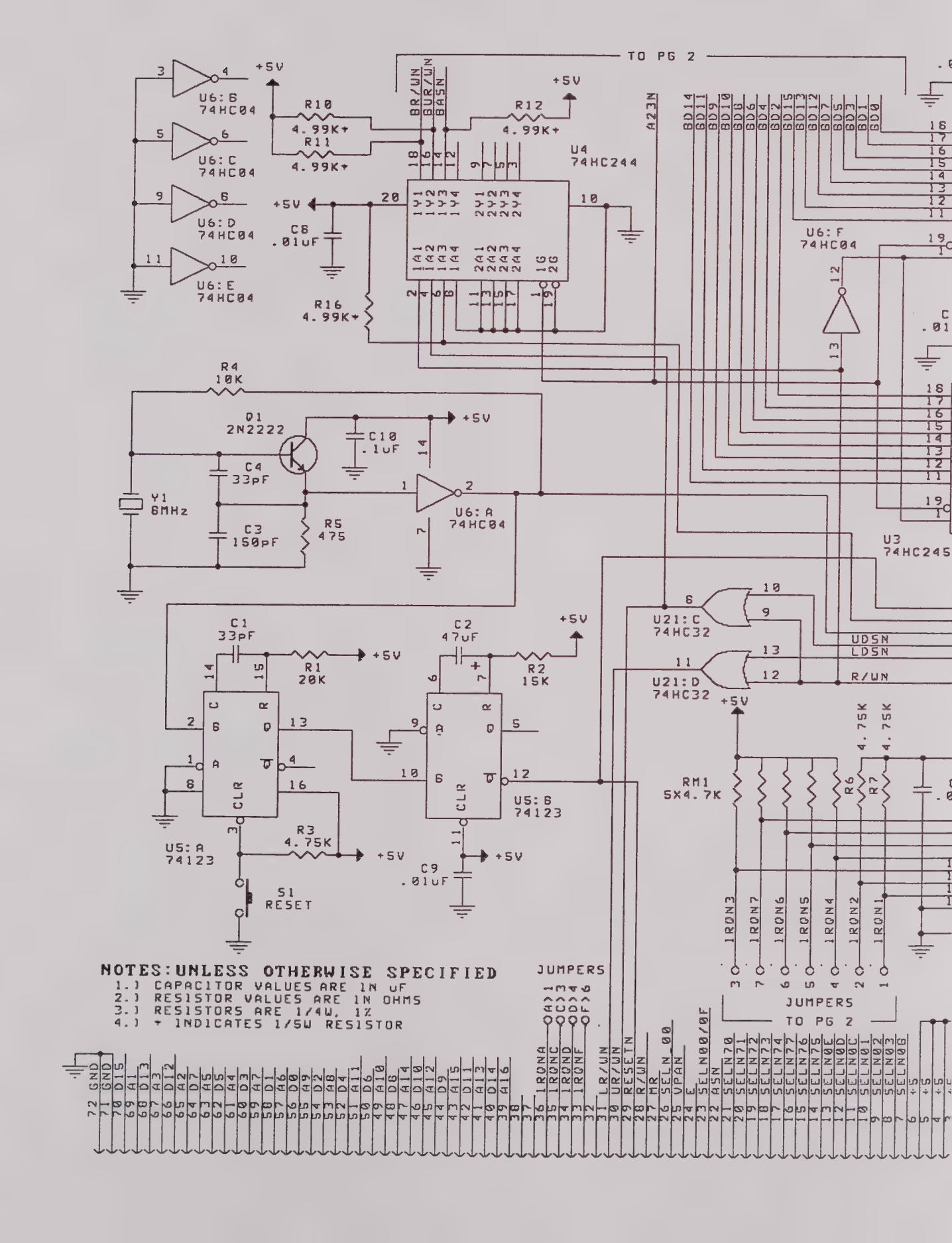
U2, 3 and 4 buffer the output to the I/O data bus.

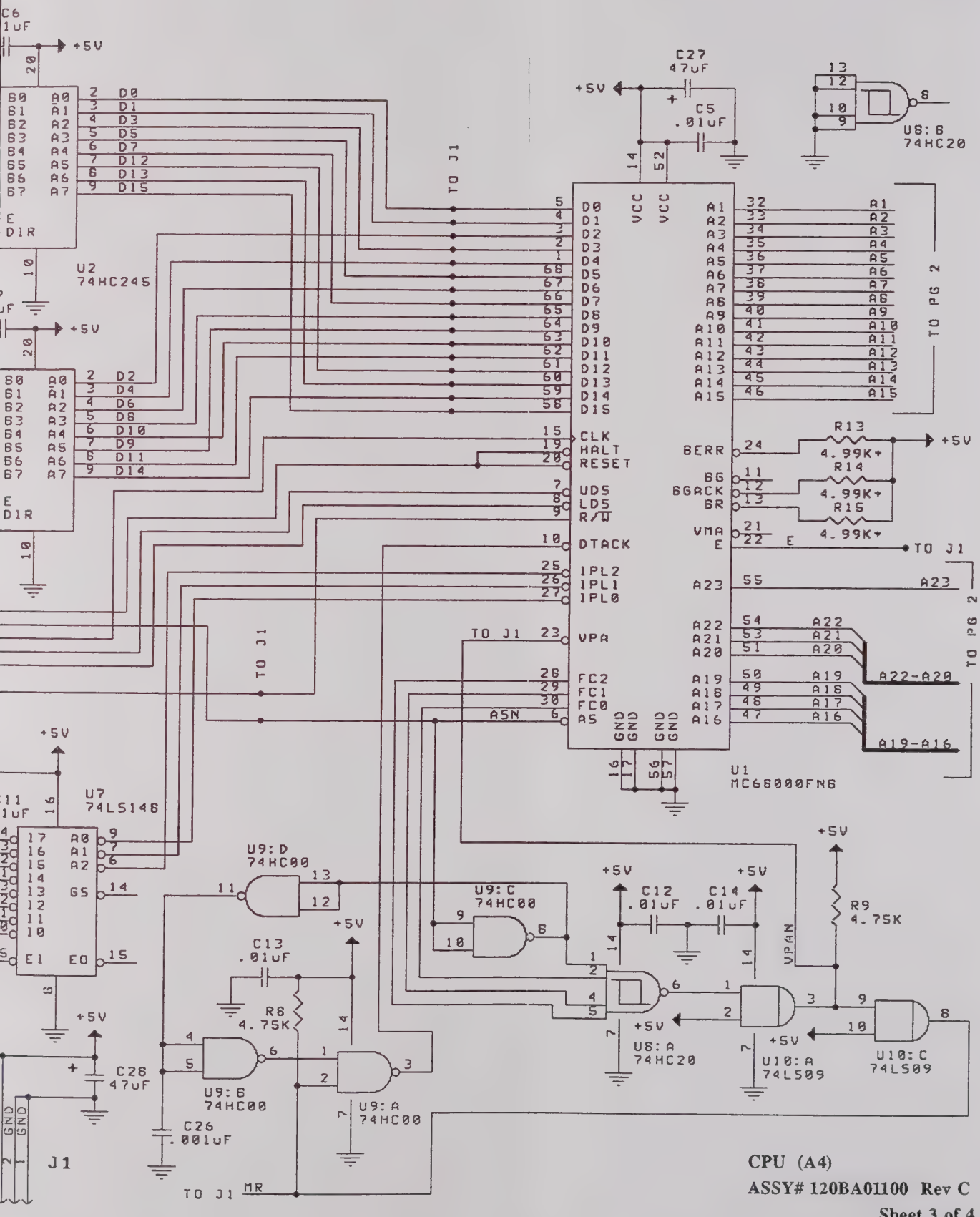
U5 A and B make up the power on reset logic. The presence of the clock is detected at pin 2. There is a set delay before the reset line switches to prevent failures during brownout or power glitch conditions.

U7 decodes interrupts. When the CPU receives an interrupt, one of the FC0 - FC2 lines is activated causing U8, 9 and 10 to generate several different logic signals. VPAN puts the CPU into the non-vectored interrupt mode in order to handle the interrupt. The MR (memory ready) logic is also generated, which slows the CPU for read/write cycles.

U11 and 12 serve to buffer between the I/O bus and the CPU.

On sheet 4, U13, 14, 15, 16, 17 and 18 decode chip selects for boards or circuits on the I/O bus. U19, 20 and 21 give a startup vector to the CPU on power up.


TO PG 2
U6:B 74HC04
U6:C 74HC04
U6:D 74HC04
U6:E 74HC04
U6:F 74HC04
U6:A 74HC04
U4 74HC244
U3 74HC245
U21:C 74HC32
U21:D 74HC32
U5:A 74123
U5:B 74123
R10 4.99K+
R11 4.99K+
R12 4.99K+
R16 4.99K+
R4 10K
R5 475
R1 20K
R2 15K
R3 4.75K
RM1 5X4.7K
R6 4.75K
R7 4.75K
C8 .01uF
C10 .1uF
C4 33pF
C3 150pF
C1 33pF
C2 47uF
C9 .01uF
Q1 2N2222
Y1 6MHz
S1 RESET
+5V
UDSN
LDSN
R/WN
A23N
JUMPERS
JUMPERS TO PG 2
NOTES: UNLESS OTHERWISE SPECIFIED
1.) CAPACITOR VALUES ARE IN uF
2.) RESISTOR VALUES ARE IN OHMS
3.) RESISTORS ARE 1/4W, 1%
4.) + INDICATES 1/5W RESISTOR

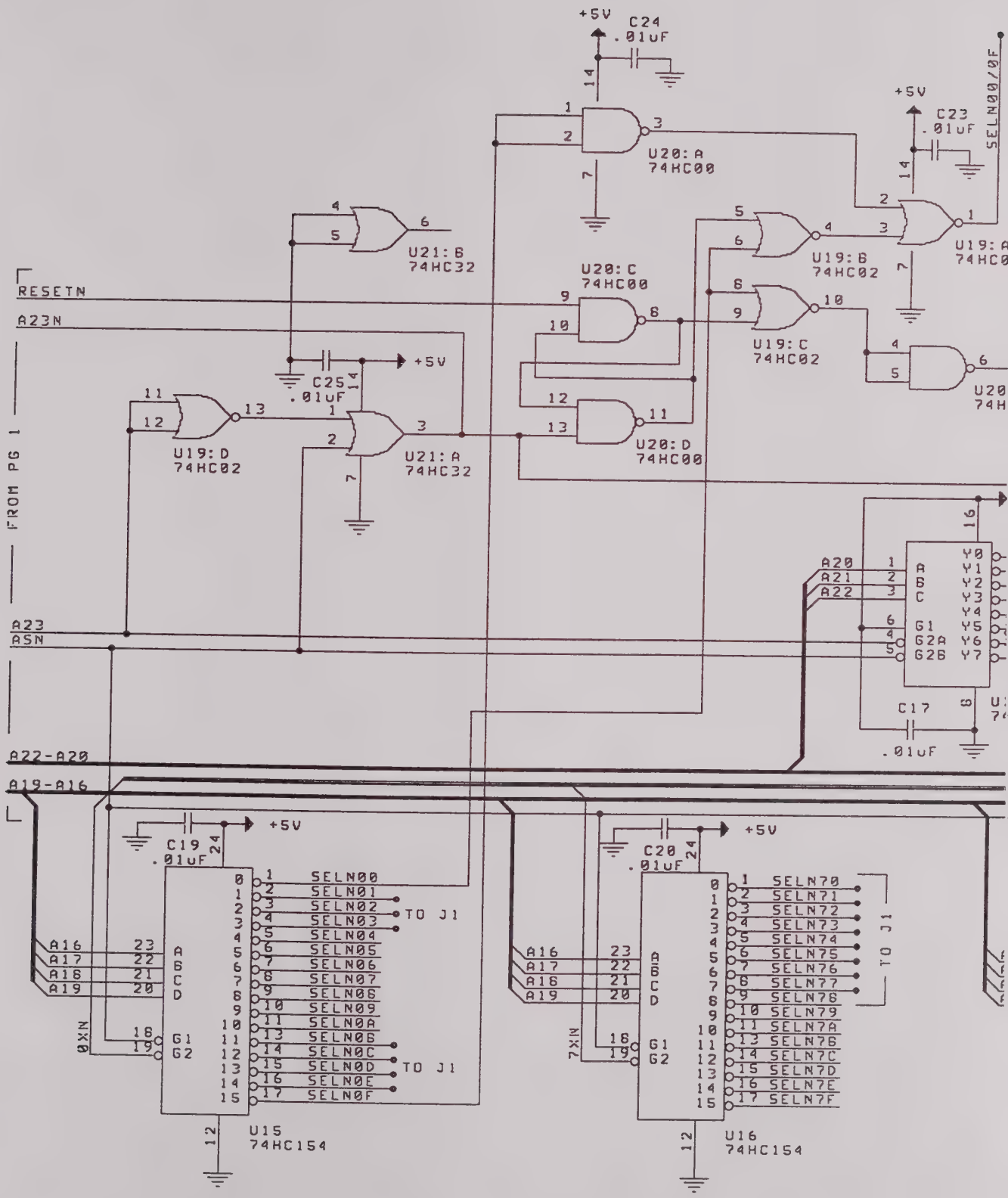


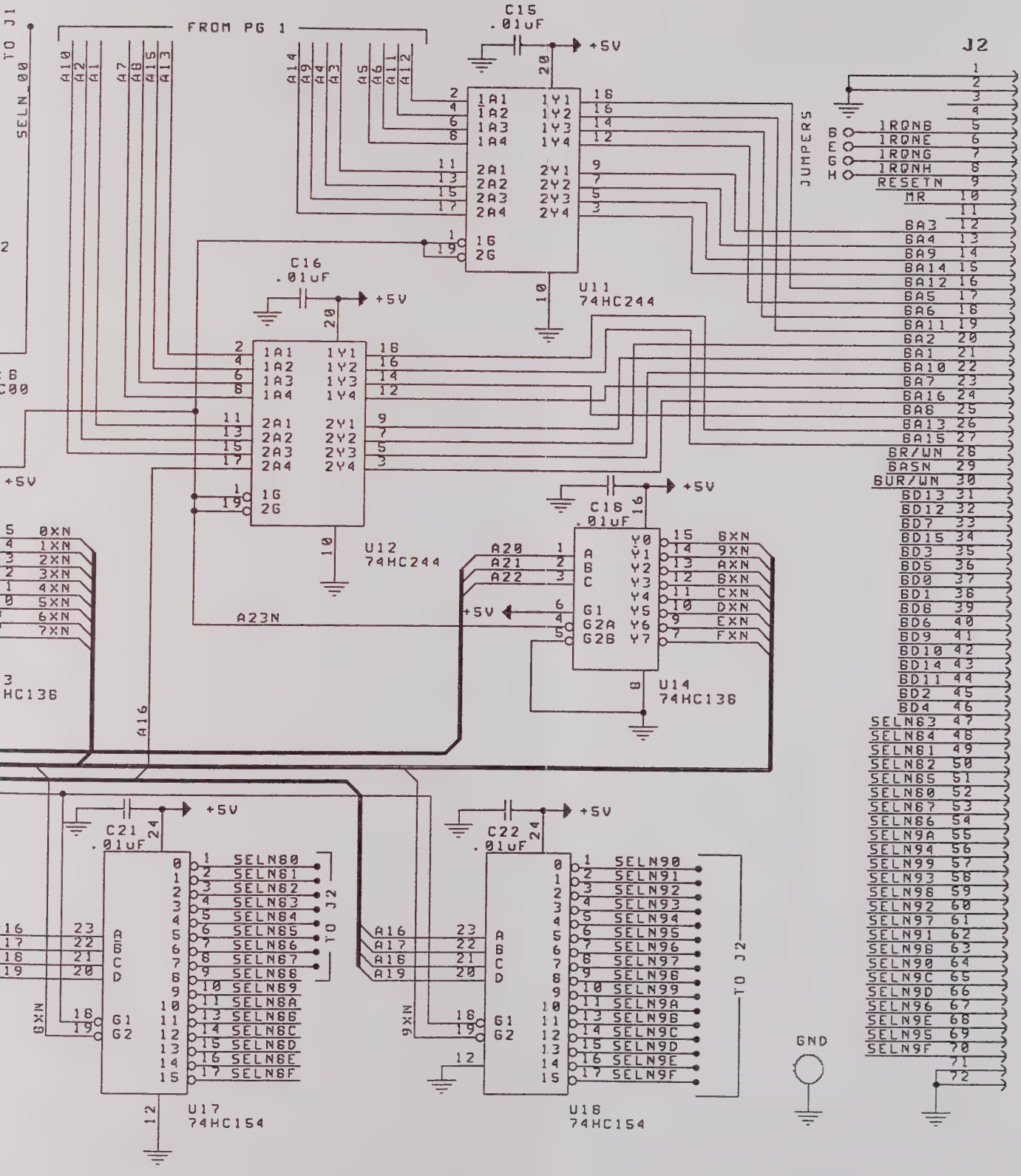

**CPU (A4)**

**ASSY# 120BA01100 Rev C**

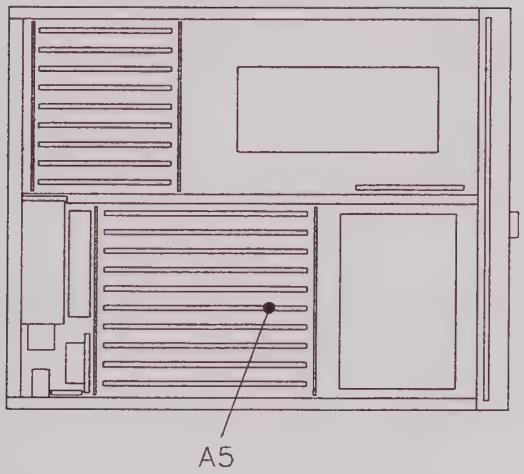
**Sheet 3 of 4**

**7-A4-3**

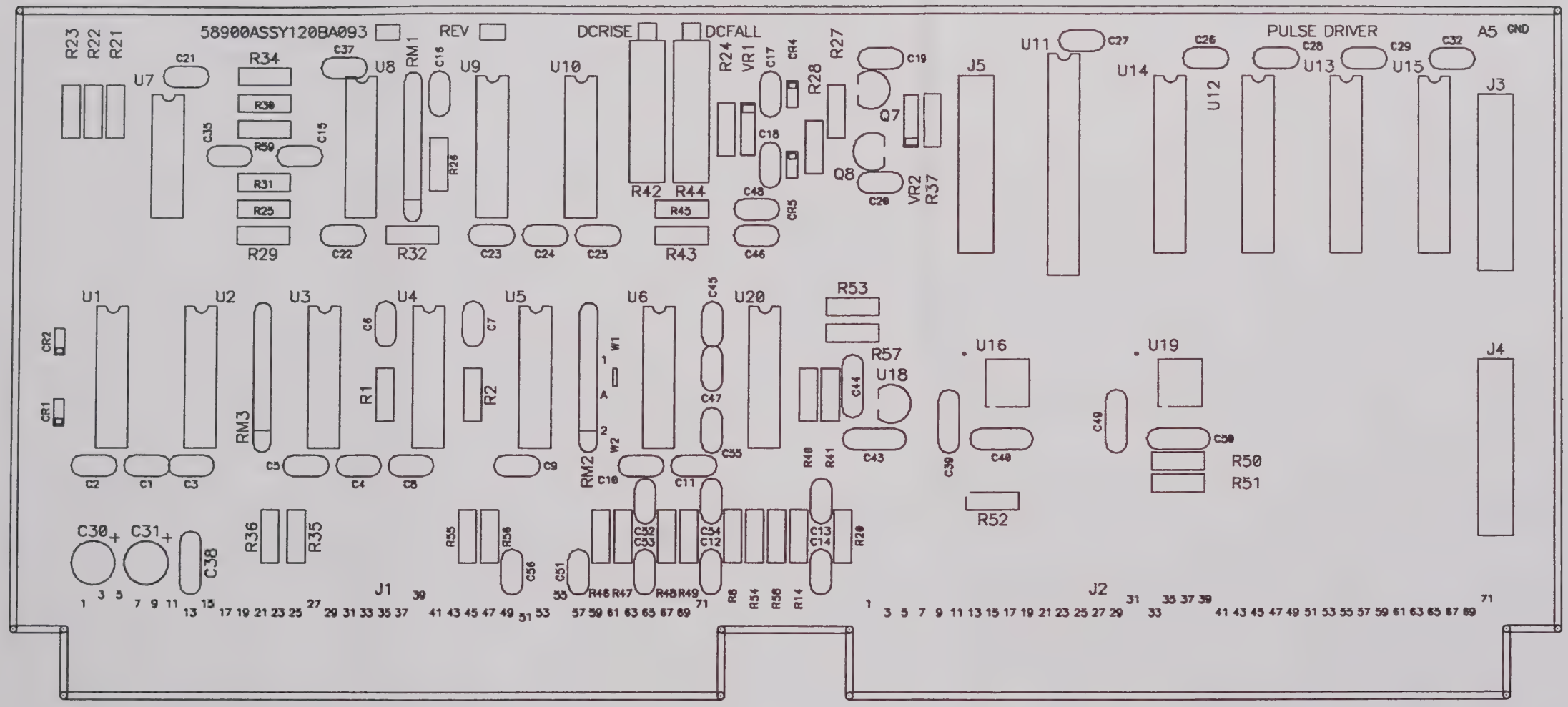

+5V
C24
.01uF
U20:A
74HC00
C23
.01uF
SELN00/0F
U21:B
74HC32
U19:B
74HC02
U20:C
74HC00
RESETN
A23N
U19:C
74HC02
C25
.01uF
U19:D
74HC02
U21:A
74HC32
U20:D
74HC00
FROM PG 1
A20
A21
A22
A23
ASN
C17
.01uF
A22-A20
A19-A16
C19
.01uF
C20
.01uF
SELN00
SELN01
SELN02
SELN03
SELN04
SELN05
SELN06
SELN07
SELN08
SELN09
SELN0A
SELN0B
SELN0C
SELN0D
SELN0E
SELN0F
TO J1
A16
A17
A18
A19
0XN
U15
74HC154
SELN70
SELN71
SELN72
SELN73
SELN74
SELN75
SELN76
SELN77
SELN78
SELN79
SELN7A
SELN7B
SELN7C
SELN7D
SELN7E
SELN7F
7XN
U16
74HC154




**CPU (A4)**
**ASSY# 120BA01100 Rev C**
**Sheet 4 of 4**
**7-A4-4**




**Pulse Driver (A5)**
**ASSY# 120BA09303 Rev D**
**Sheet 1 of 4**
**7-A5-1**




**PULSE DRIVER -- PC ASSY A5**

The pulse driver PCA has various logic circuits required for directing the pulse signals to the proper locations, as well as the actual pulse driver circuitry which drives the pulse modulators. U12, 13, 14 and 15 are latches providing interface between the I/O bus and the individual circuits on the driver board as well as the pulse generator board (A5A1). U11 decodes the chip selects for the latches and other circuitry.

When EXT Pulse Modulation is selected, the external pulse signal is received at PM_IN, U1-5. The external signal and its complement are output on U1-2 and U1-4. EPM- logic at U1-7 selects one of the signals to propagate U2 A or B, selecting + or - edge trigger when EXT TRIG (+ or -) or EXT PULS (+ or - ) is selected. In the case of EXT TRIG the trigger signal (TRIGN) is supplied to the pulse generator PCA (A5A1) via U4 D, U8 C and U9 C. The external pulse signal from U2 A or B is allowed to propagate thru U2 D and ultimately on to the pulse drivers, when U2 D is enabled via U3 A and the EXTPUL logic signal.

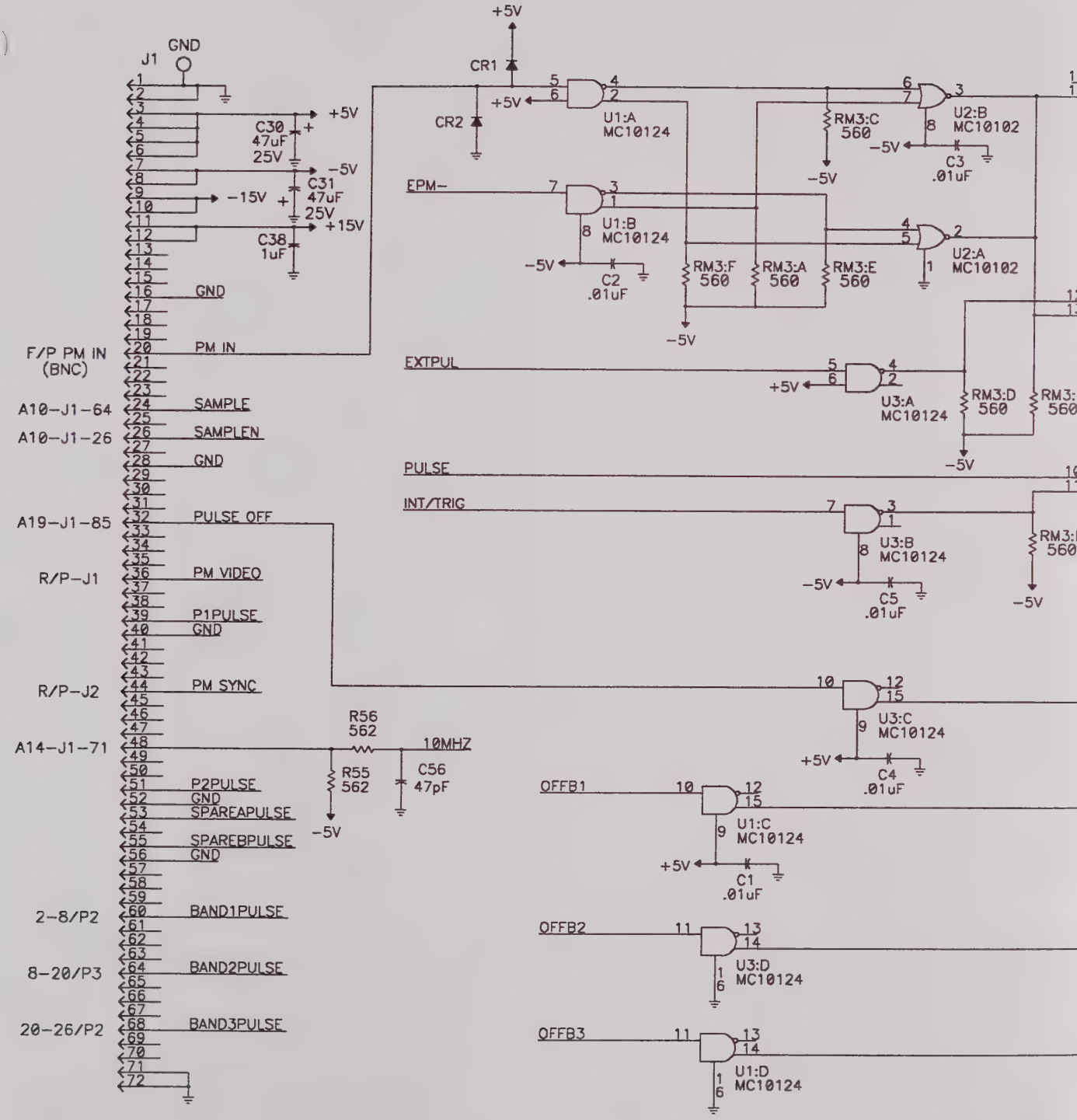
The PULSE signal from the pulse generator PCA is allowed to propagate thru U2 C and ultimately on to the pulse driver circuitry, when the INT/TRIG signal is true. This allows only one signal at a time, either the external pulse signal or the internal pulse signal, to drive the pulse modulators.

The selected pulse signal is provided to the rear panel as the PM_VIDEO signal after being translated to a TTL signal.

U6 A, U4 and associated components allow the rising and falling edge of this signal to be positioned to align with the actual pulsed RF out of the unit. In addition the selected pulse signal (referred to as SAMPN on the schematic) is used for the purpose of sampling the detector voltage on the leveling board when the RF is on. In order to do this it is necessary to delay and shorten the pulse. This is done by U8 A, B, D, U9 A, B and D. The signal is then translated by U10 A, B, Q7 and Q8 to signal levels which are capable of switching the FET samplers on the Leveling PCA. The resulting signal is called SAMPLE.

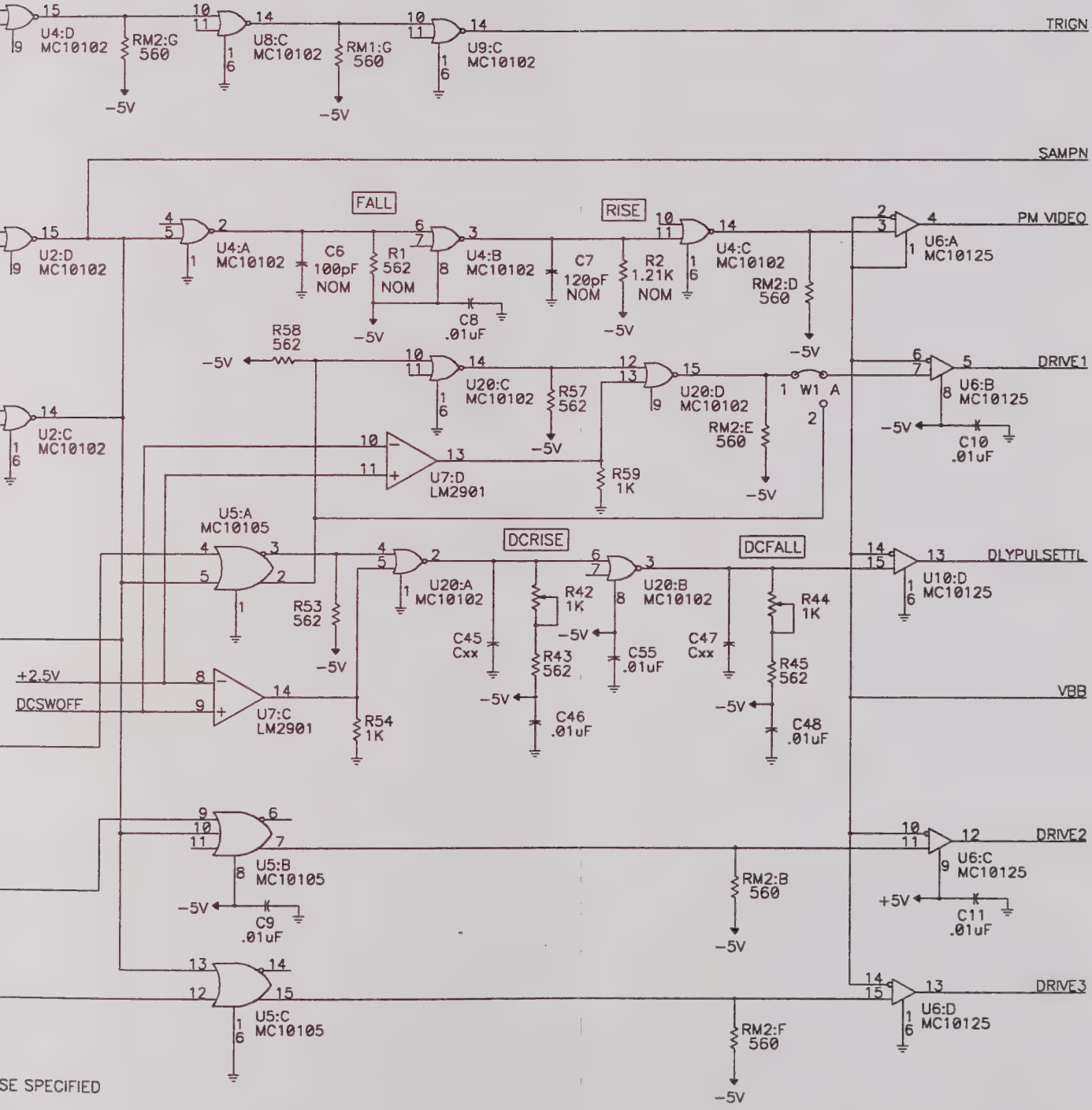
U1 C and D, and U3 D handle the logic which selects the proper driver to be enabled at U5 A, B or C. The pulse signal is translated to TTL levels at U6 B thru D.

When pulse modulation is not selected the FET samplers on the leveling PCA must stay on continuously. The PULSE_OFF logic signal serves this purpose via U3 C and U7 A.




NOTES: UNLESS OTHERW

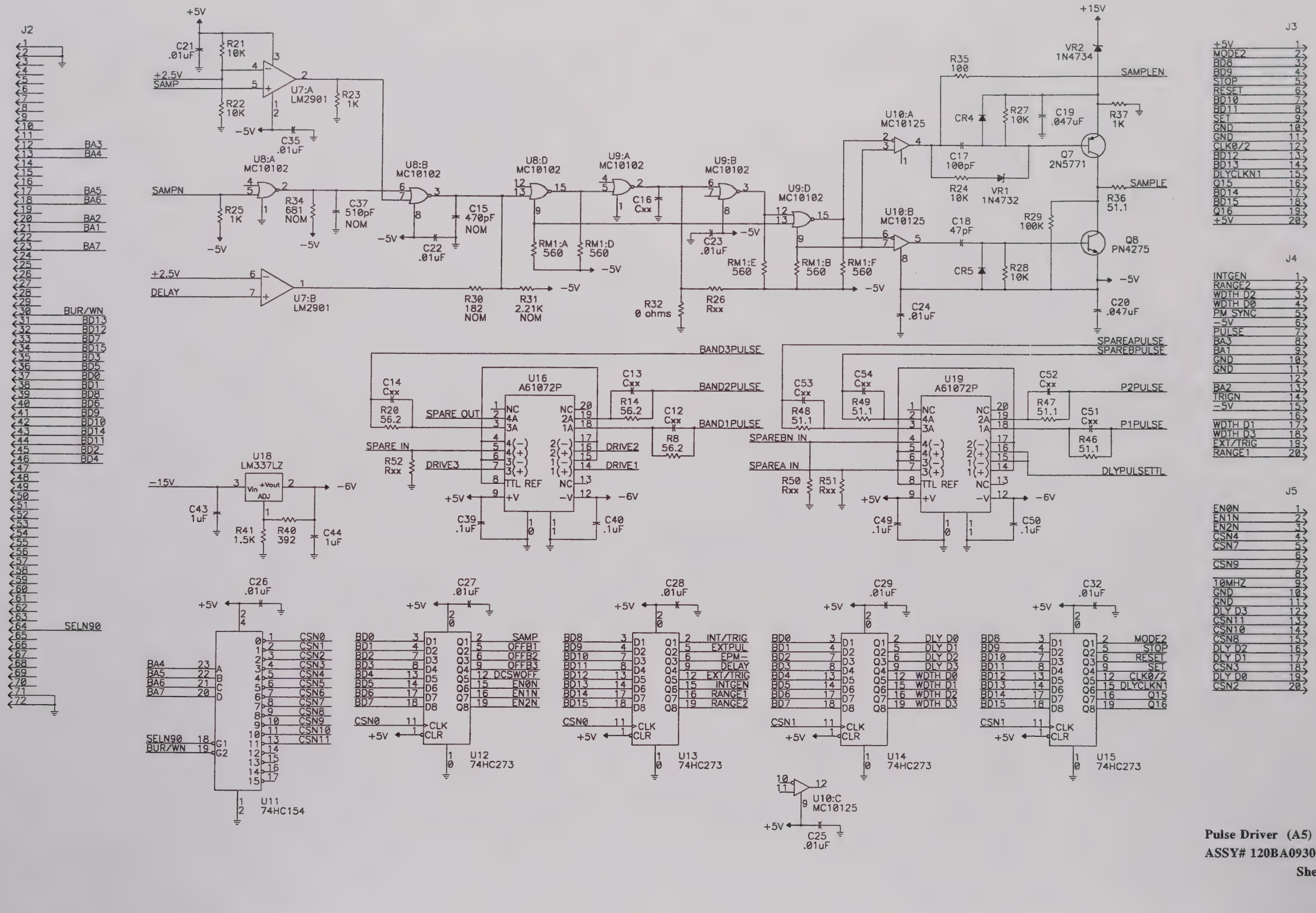
1. CAPACITOR VALUES
2. RESISTOR VALUES A
3. RESISTORS ARE 1/4
4. DIODES ARE 1N4148



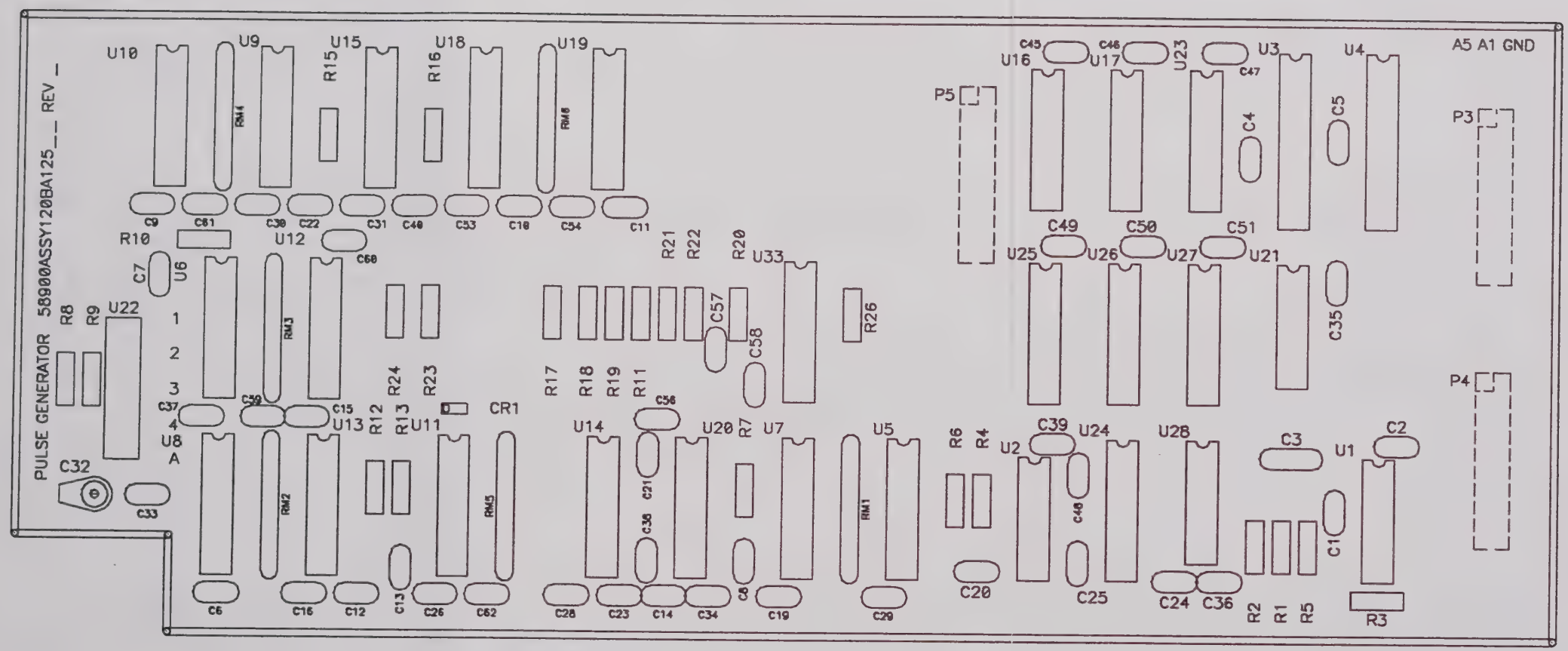

SE SPECIFIED

ARE IN uF.
RE IN OHMS
W, 1%

**Pulse Driver (A5)**
**ASSY# 120BA09303 Rev D**
**Sheet 3 of 4**
**7-A5-3**




**Pulse Driver (A5)**
**ASSY# 120BA09303 Rev D**
**Sheet 4 of 4**
**7-A5-4**




**PULSE GENERATOR -- PC ASSY A5A1**

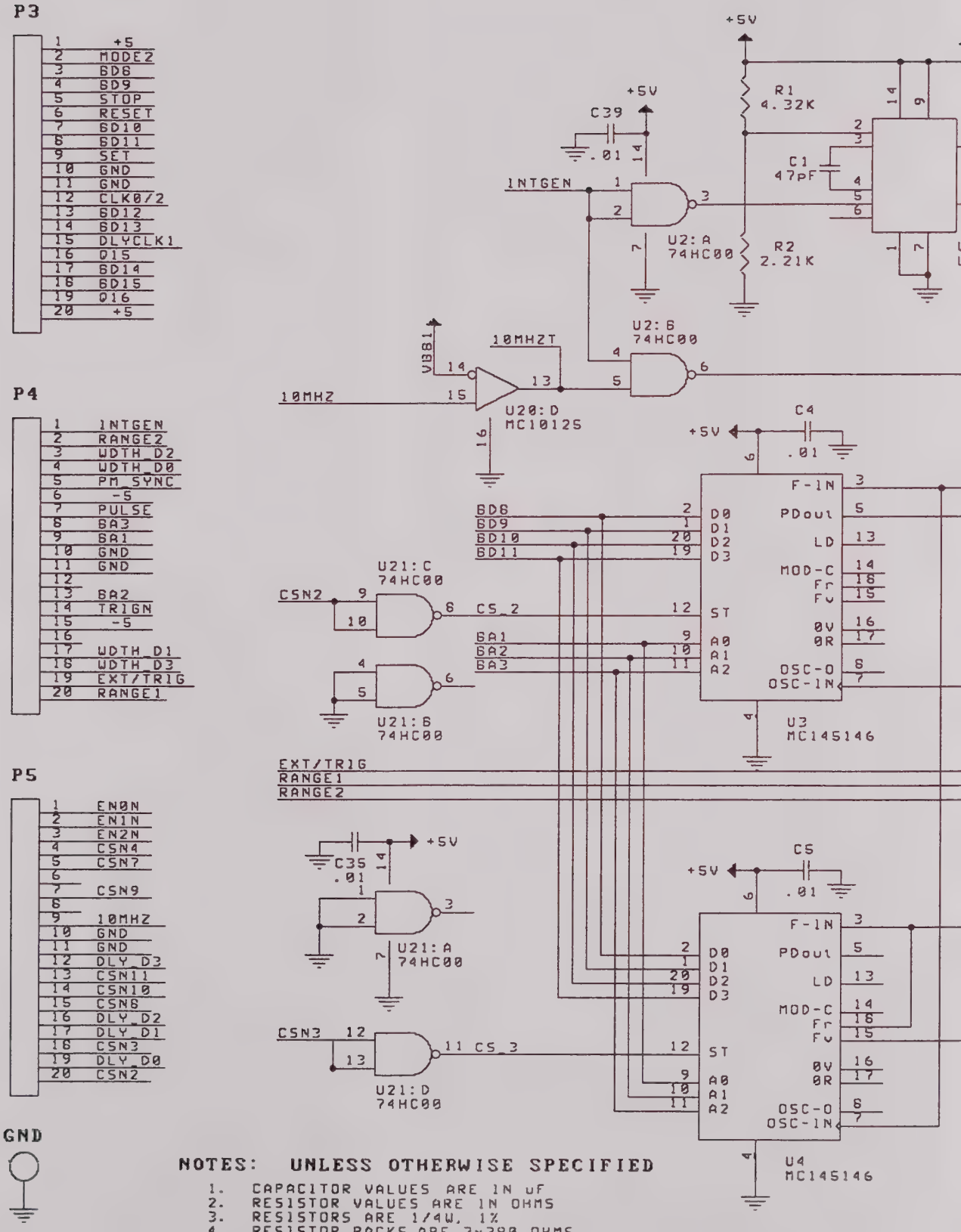
The pulse generator consists of three sections: the rate generator, the delay generator, and the width generator.

The rate generator employs a programmable phase lock loop circuit, consisting of a 3-10 MHz VCO (U1), and two synthesizer chips (U3/U4) containing phase comparators and programmmable dividers. The PLL circuit uses the instrument's 10 MHz timebase (translated to TTL levels by U20-D and enabled by U2-B when the internal pulse mode is selected) as a reference input, and generates a series of stable frequencies, selected by the programming of the synthesizer chips. There are actually two ranges of frequencies, depending on whether U2-C (RANGE 1) or U2-D (RANGE 2) is enabled; the signal propagates through U5-A and U5-B to U33-A. In the case of externally triggered modulation, U7-A is enabled and the 'TRIGN' input propagates through it to U33-A. The output of U33-A ('STARTN') is used to gate (via U6-A) a 100 MHz delay line clock consiting of U8-D, U22, C32 and C33. This signal is turned into a PM_SYNC signal by U33-D, U7-B, U7-C, U33-C, and U20C, for output to the rear panel.

The delay is generated in 10 ns increments by multiple counters which are clocked by the 100 MHz clock described above. U10 is a 4 bit counter which counts delays up to 160 ns; U16 is an 8 bit counter which counts up to approximately 40.9 µs in 160 ns increments. U17 counts up to approximately 10.485 ms in 40.9 µs increments and U23 counts up to approximately 2.6 s in 10.485 µs increments. These counters are programmed by the computer, allowing up to 2 seconds of delay, programmable in 10 ns increments. When the delay cycle is completed and the DEND from U28-A and the COUT from U10 have propagated thru the gates giving low inputs at U8-6 and U8-7, U6-10 is toggled and the width cycle starts on the next clock cycle. The beginning of the width cycle causes U6-15 to go high; this signal, after propagating thru U13-A and U33-B, is the actual pulse signal which will ultimately drive the RF pulse modulators.

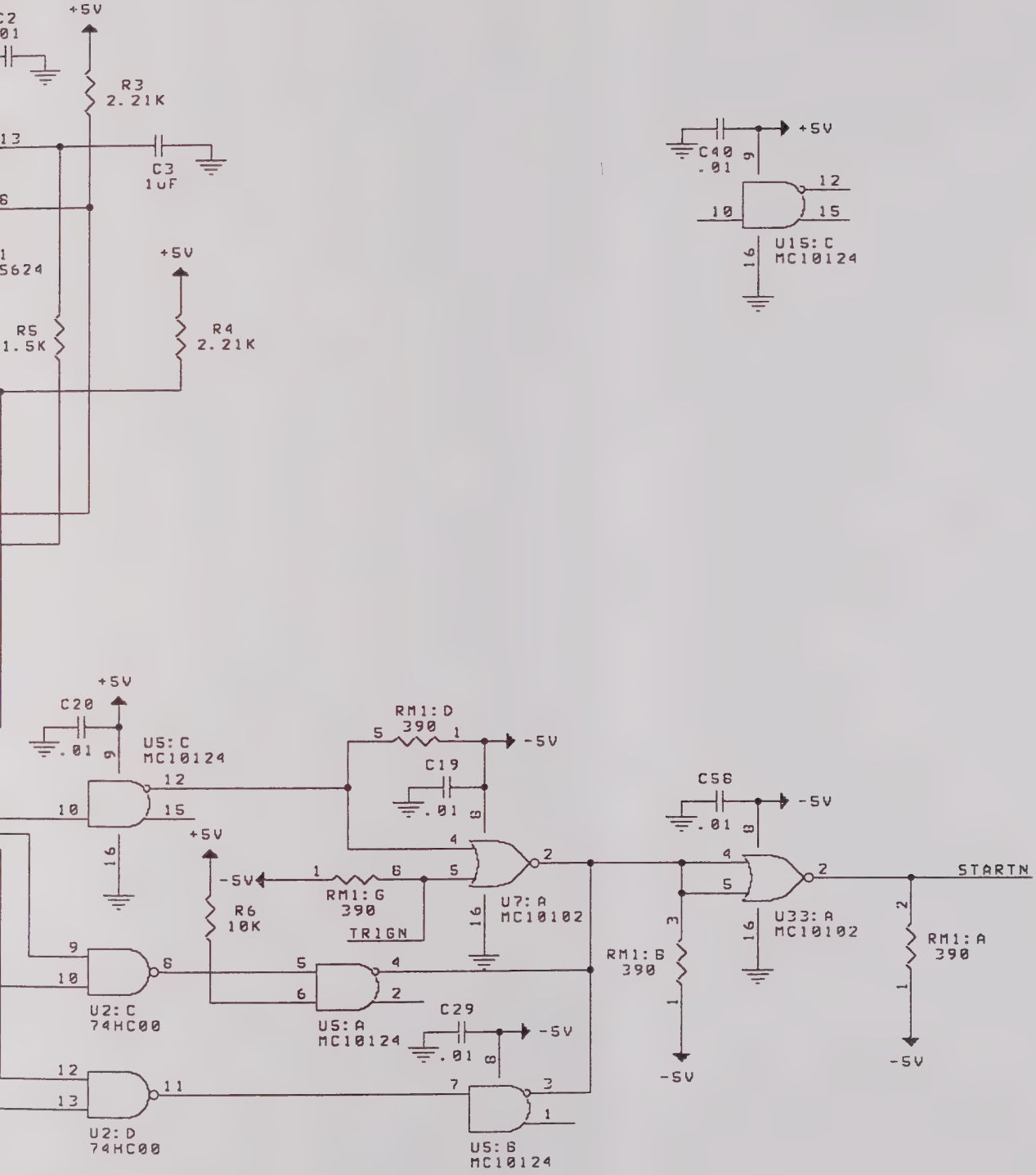
The width is also generated in 10 ns increments and the counters (U11, U25, U26 and U27) are set up similarly to those which control the delay cycles. The width cycle ends when both inputs to U8-C are low (this is controlled by U11 COUT and U28 DEND), causing U6 to be reset.

The next trigger from the rate generator will start another delay and width cycle.

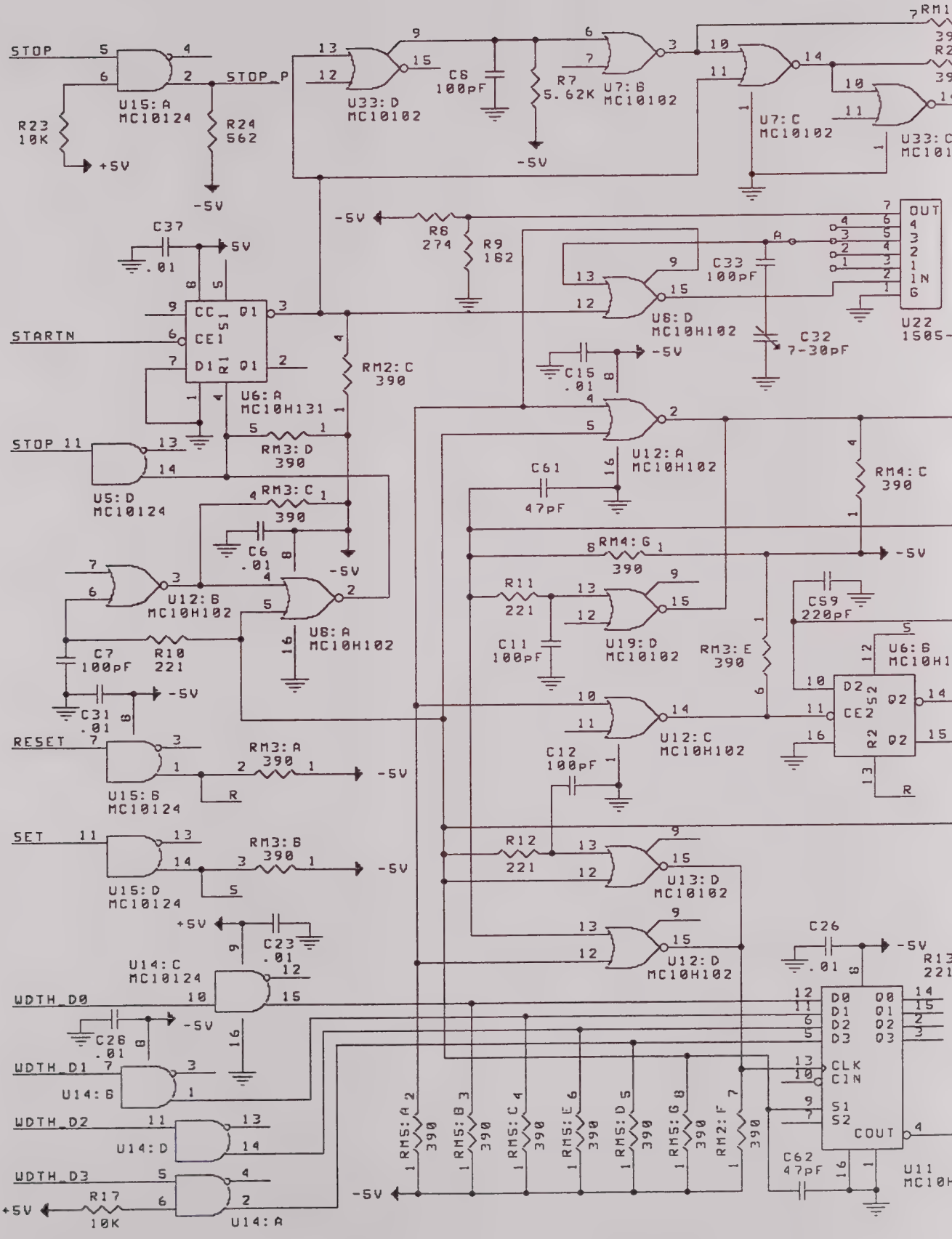


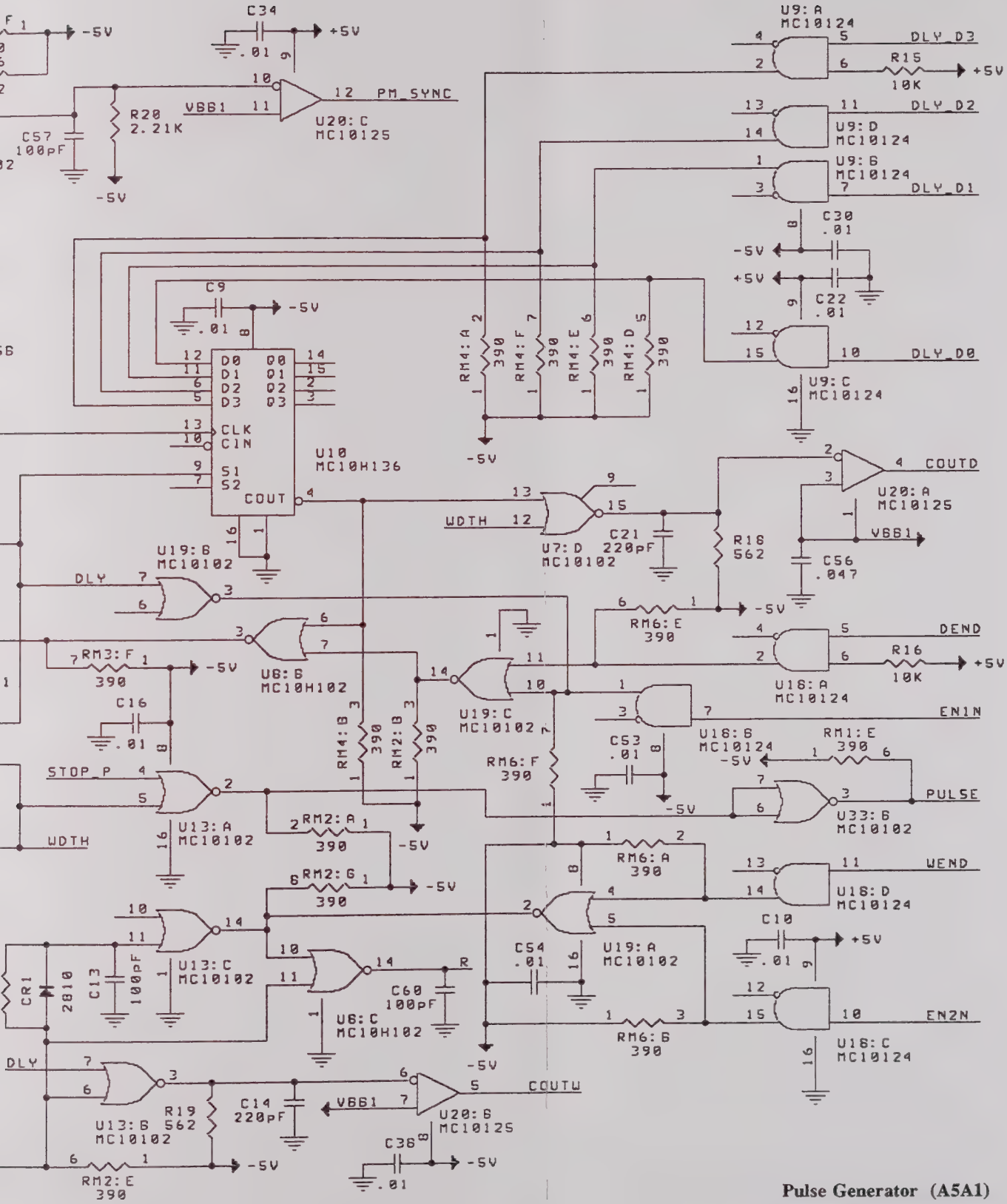

**NOTES: UNLESS OTHERWISE SPECIFIED**

1. CAPACITOR VALUES ARE IN uF
2. RESISTOR VALUES ARE IN OHMS
3. RESISTORS ARE 1/4W, 1%
4. RESISTOR PACKS ARE 7x390 OHMS

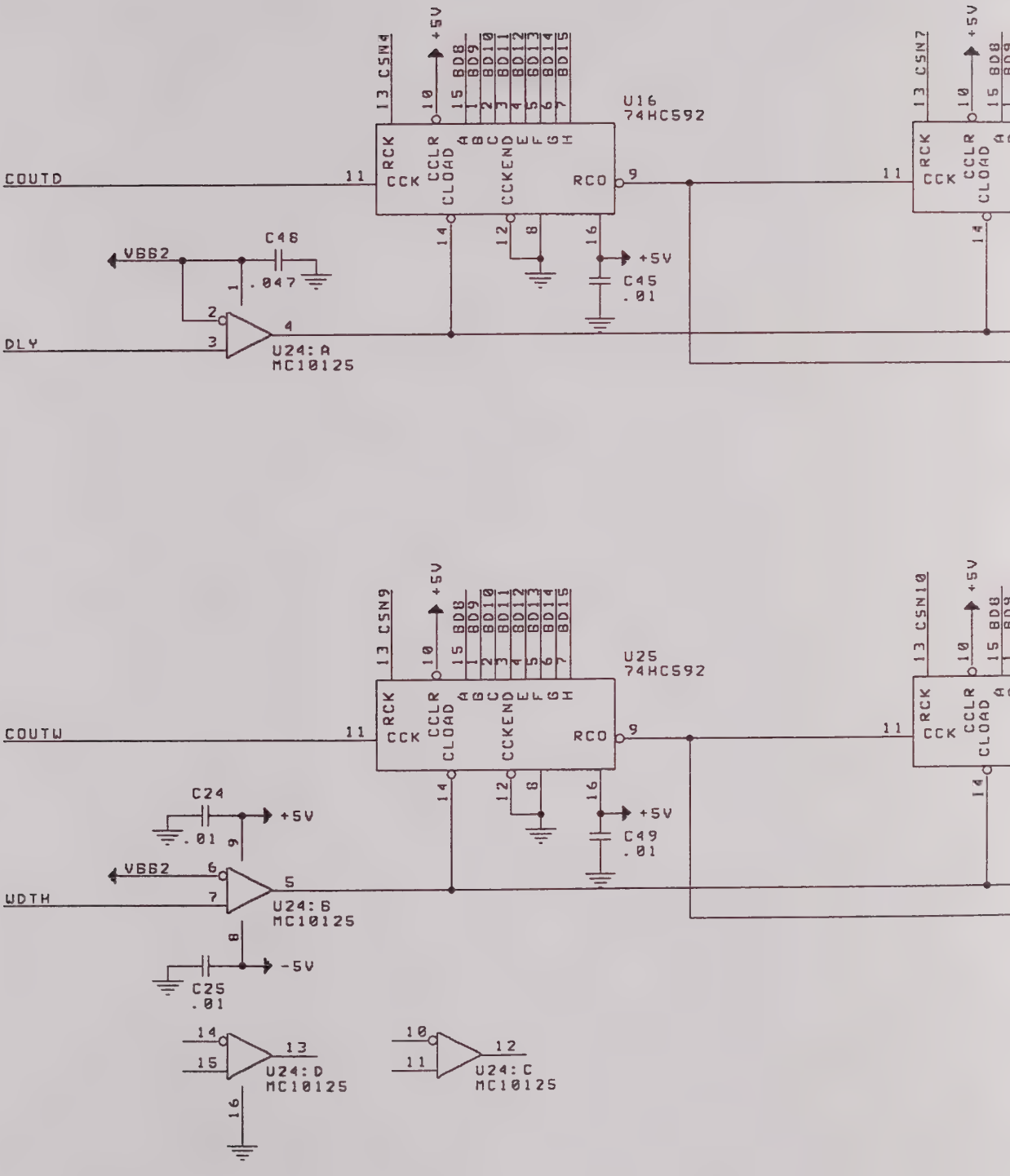


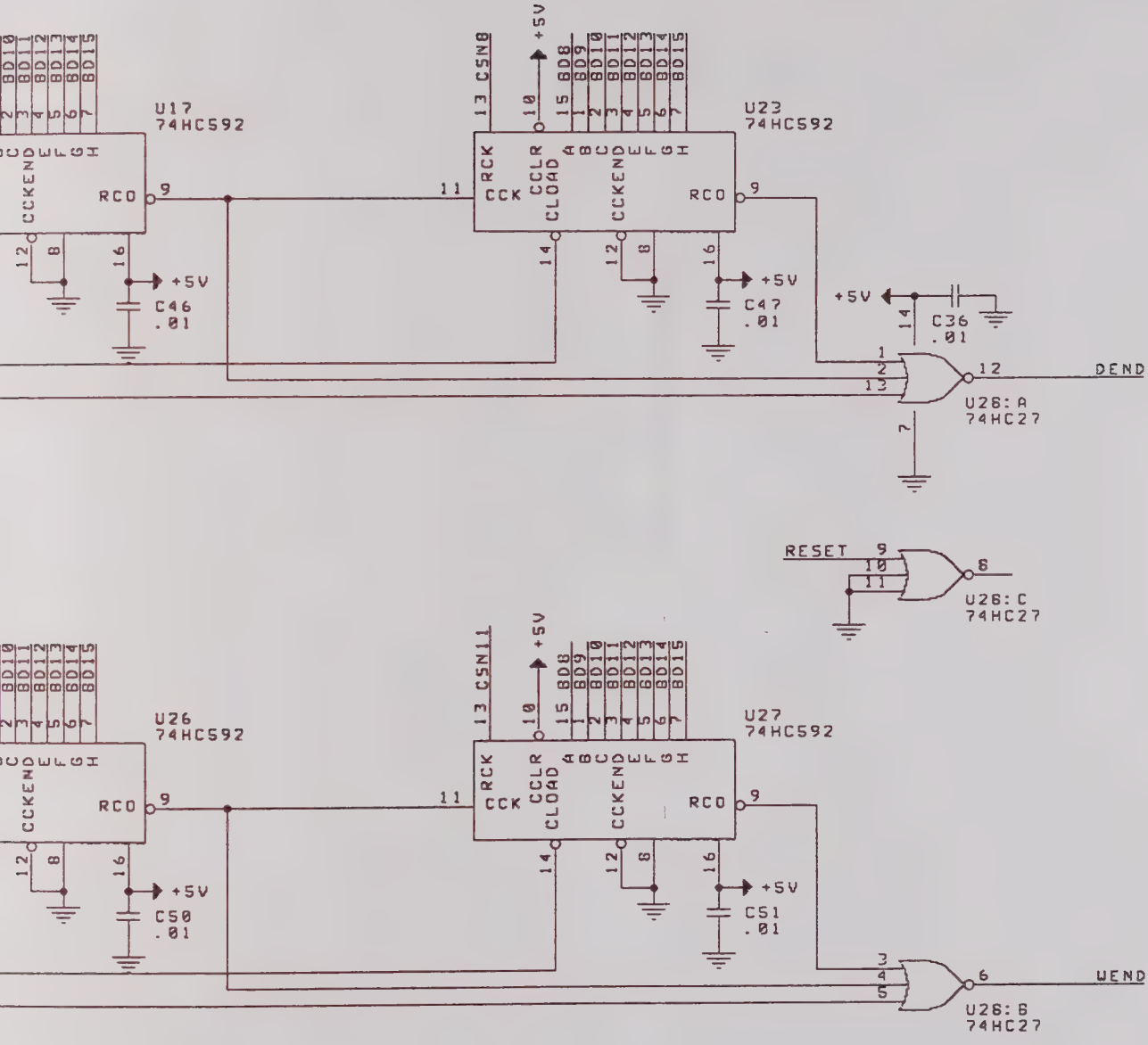

**Pulse Generator (A5A1)**
**ASSY# 120BA12550 Rev A**
**Sheet 2 of 4**
**7-A5-6**


STOP
STOP_P
U15:A MC10124
R23 10K
+5V
R24 562
-5V
U33:D MC10102
C6 100pF
R7 5.62K
U7:B MC10102
U7:C MC10102
U33:C MC101
RM1
C37 .01
STARTN
CC
CE1
D1
Q1
U6:A MC10H131
RM2:C 390
R8 274
R9 162
C33 100pF
U8:D MC10H102
C32 7-30pF
OUT
U22 1505
C15 .01
STOP 11
U5:D MC10124
RM3:D 390
C61 47pF
U12:A MC10H102
RM4:C 390
RM3:C 390
C6 .01
U12:B MC10H102
U8:A MC10H102
RM4:G 390
R11 221
U19:D MC10102
C11 100pF
RM3:E 390
C59 220pF
U6:B MC10H1
C7 100pF
R10 221
C31 .01
U12:C MC10H102
C12 100pF
RESET
U15:B MC10124
RM3:A 390
R
SET
U15:D MC10124
RM3:B 390
S
R12 221
U13:D MC10102
U12:D MC10H102
C23 .01
U14:C MC10124
C26 .01
C26
R13 221
WDTH_D0
WDTH_D1
WDTH_D2
WDTH_D3
U14:B
U14:D
U14:A
R17 10K
RM5:A 2 390
RM5:B 3 390
RM5:C 4 390
RM5:E 6 390
RM5:D 5 390
RM5:G 8 390
RM2:F 7 390
D0
D1
D2
D3
CLK
CIN
S1
S2
COUT
C62 47pF
U11 MC10H




**Pulse Generator (A5A1)**
**ASSY# 120BA12550 Rev A**
**Sheet 3 of 4**
**7-A5-7**


COUTD
COUTW
DLY
WDTH
VBB2
U16
74HC592
U25
74HC592
U24:A
MC10125
U24:B
MC10125
U24:C
MC10125
U24:D
MC10125
C48
.047
C45
.01
C24
.01
C49
.01
C25
.01
+5V
-5V
RCK
CCK
CCLR
CLOAD
CCKEN
RCO
CSN4
CSN7
CSN9
CSN10
BD8
BD9
BD10
BD11
BD12
BD13
BD14
BD15

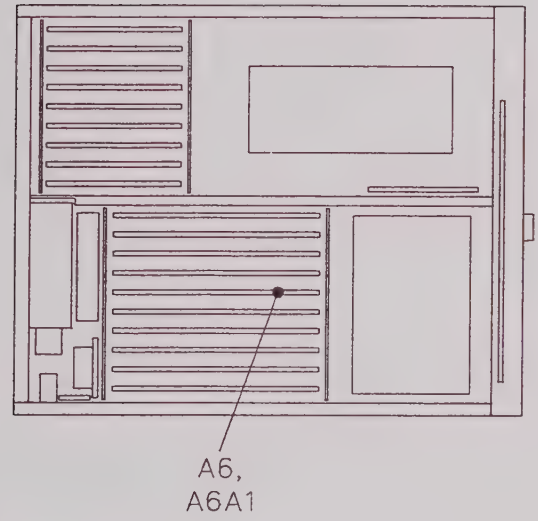




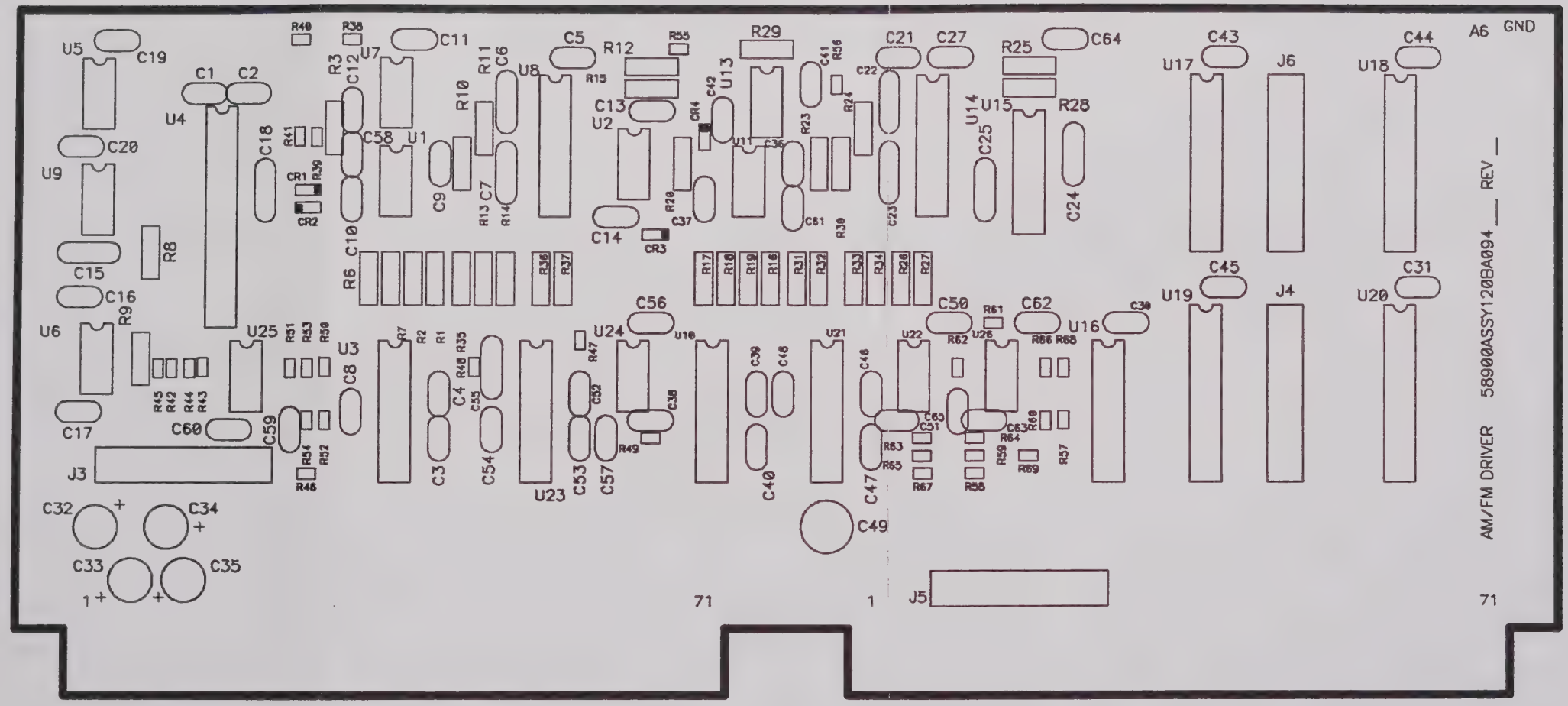





**Pulse Generator (A5A1)**
**ASSY# 120BA12550 Rev A**
**Sheet 4 of 4**
**7-A5-8**




**AM/FM Driver (A6)**
**ASSY# 120BA09401 Rev A**
**Sheet 1 of 4**
**7-A6-1**



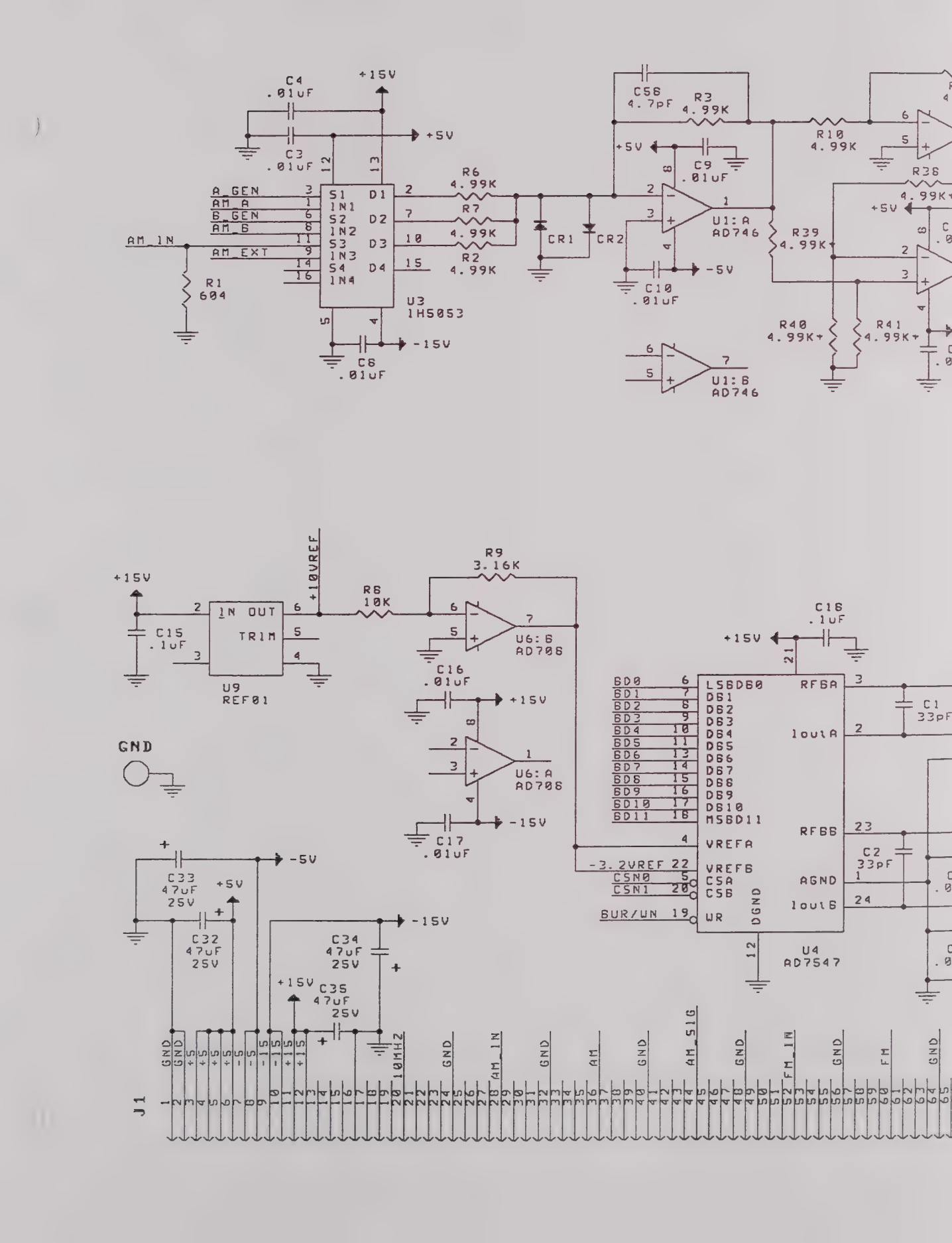

**AM/FM DRIVER -- PC ASSY A6**

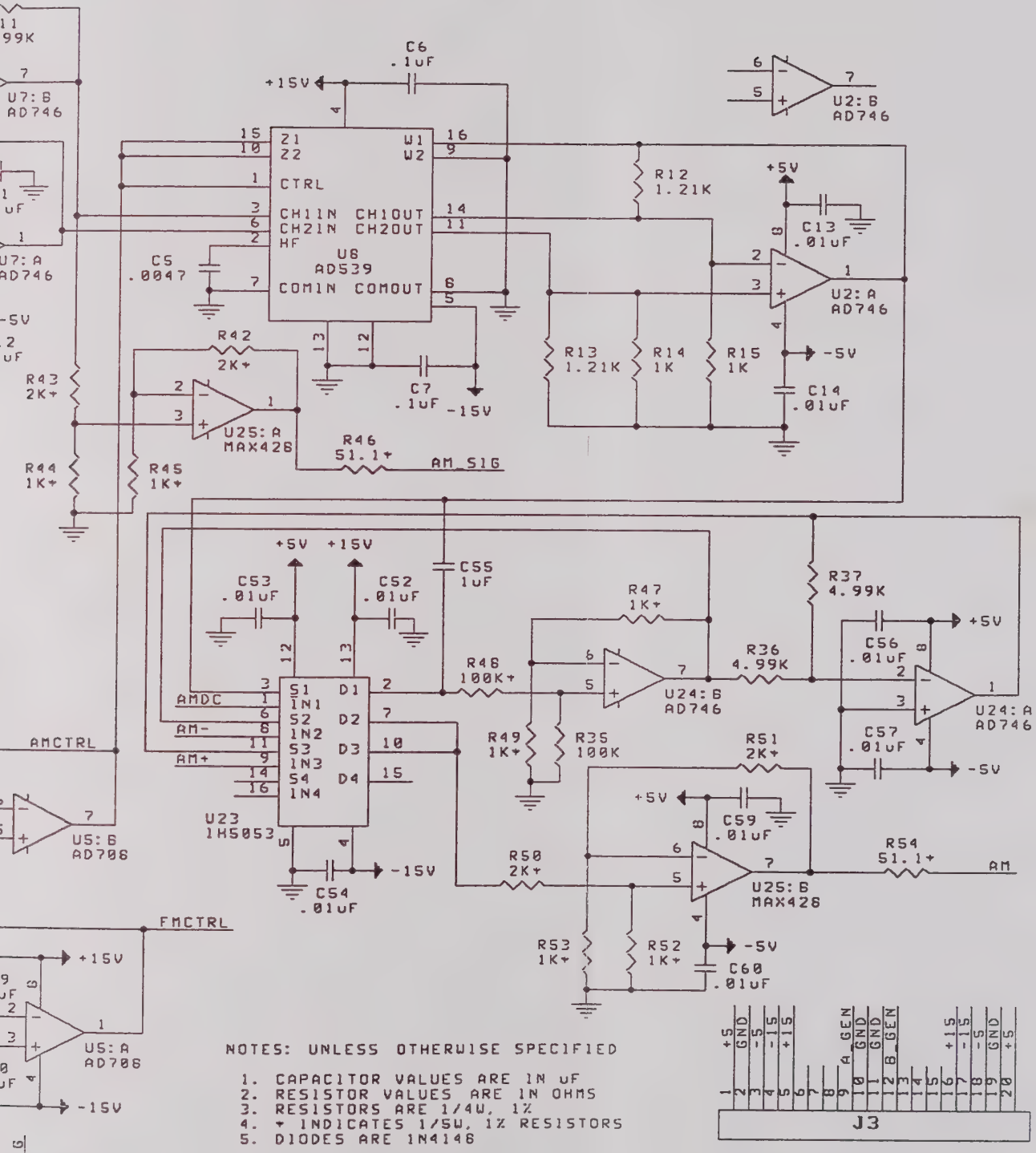
The AM/FM driver PCA has two main functions. The first is to select the internal or external AM or FM signal. The second is to adjust the amplitude of the selected signal according to the depth or deviation required before outputting the signal to the level board (for AM) or the output PLL (for FM).

U3 is an analog switch which is used to select the external AM signal or a signal from the internal generator. The selected signal is buffered by U1 and then converted to a differential signal by U7 A and B. One side of this differential signal is buffered by U25 A for output to the rear panel as the AM_SIG output. Modulator IC, U8, functions as a variable attenuator which is controlled by a voltage from the DAC U4. The voltage at U5-7 changes according to the selected AM depth of modulation. The DAC has a reference voltage which is derived from U9, inverted and attenuated to give 3.2 volts. The output of the variable attenuator U8 is a differential signal which is combined by U2 A to give a single AM signal output. U23 switches this output (the signal can be switched to be DC coupled or inverted to give an output which is 180 degrees out of phase with the input signal) to the input of U25 B which provides the AM signal to the level board A10.

U10 is an analog switch which is used to select the external FM signal or a signal from the internal generator. The selected signal is buffered by U11 and then converted to a differential signal by U13 A and B. One side of this differential signal is buffered by U26 A for output to the rear panel as the FM_SIG output. The voltage from DAC U4 and U5 A controls the amplitude of the FM signal via U14, depending on the deviation selected. The output of the variable attenuator U14 is a differential signal which is combined by U15 to give a single signal output. This output is then switched by U21 (the signal can be switched to be DC coupled or inverted to give an output which is 180 degrees out of phase with the input signal) to the input of U26 B which provides the FM signal for the output PLL board A18.

U16 decodes chip select lines for other IC's on the board. U17 thru U20 are required to latch data for circuits on this board and also for circuits on the A6A1 PCA.

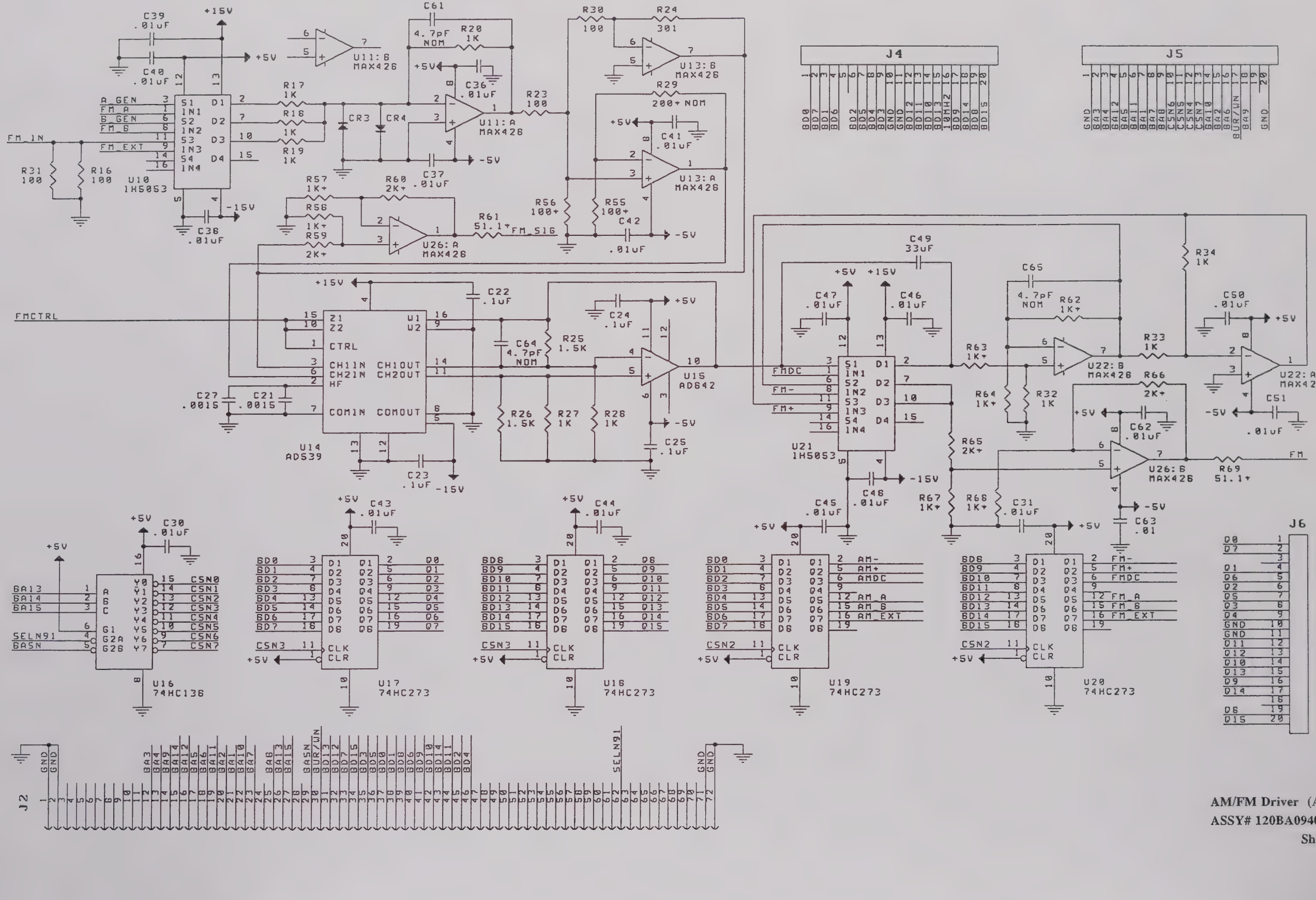

C4
.01uF
+15V
C3
.01uF
+5V
C56
4.7pF
R3
4.99K
R10
4.99K
C9
.01uF
R38
4.99K
A_GEN
AM_A
B_GEN
AM_B
AM_EXT
AM_IN
S1
1N1
S2
1N2
S3
1N3
S4
1N4
D1
D2
D3
D4
U3
1H5053
R6
4.99K
R7
4.99K
R2
4.99K
R1
604
CR1
CR2
U1:A
AD746
R39
4.99K
C10
.01uF
-5V
R40
4.99K
R41
4.99K
U1:B
AD746
-15V
C8
.01uF
+10VREF
R9
3.16K
R8
10K
C15
.1uF
IN
OUT
TRIM
U9
REF01
U6:B
AD706
C16
.01uF
U6:A
AD706
C17
.01uF
GND
C18
.1uF
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
BD8
BD9
BD10
BD11
LSBDB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DB8
DB9
DB10
MSBD11
VREFA
-3.2VREF
VREFB
CSN0
CSN1
CSA
CSB
BUR/WN
WR
DGND
RFBA
IoutA
RFBB
AGND
IoutB
C1
33pF
C2
33pF
U4
AD7547
C33
47uF
25V
C32
47uF
25V
C34
47uF
25V
C35
47uF
25V
J1
GND
+5V
-5V
-15V
+15V
10MHZ
AM_IN
AM
AM_SIG
FM_IN
FM



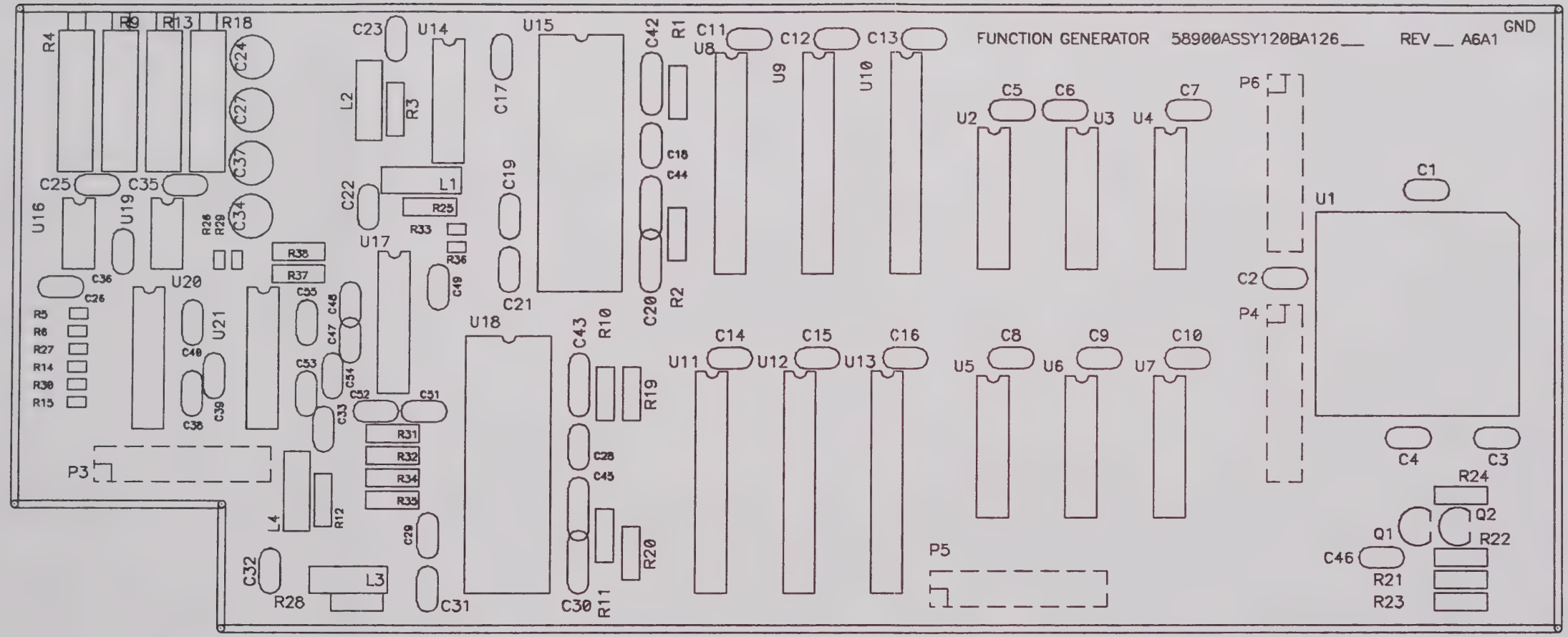

NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPACITOR VALUES ARE IN uF
2. RESISTOR VALUES ARE IN OHMS
3. RESISTORS ARE 1/4W, 1%
4. + INDICATES 1/5W, 1% RESISTORS
5. DIODES ARE 1N4148

**AM/FM Driver (A6)**
**ASSY# 120BA09401 Rev A**
**Sheet 3 of 4**
**7-A6-3**




**AM/FM Driver (A6)**
**ASSY# 120BA09401 Rev A**
**Sheet 4 of 4**
**7-A6-4**

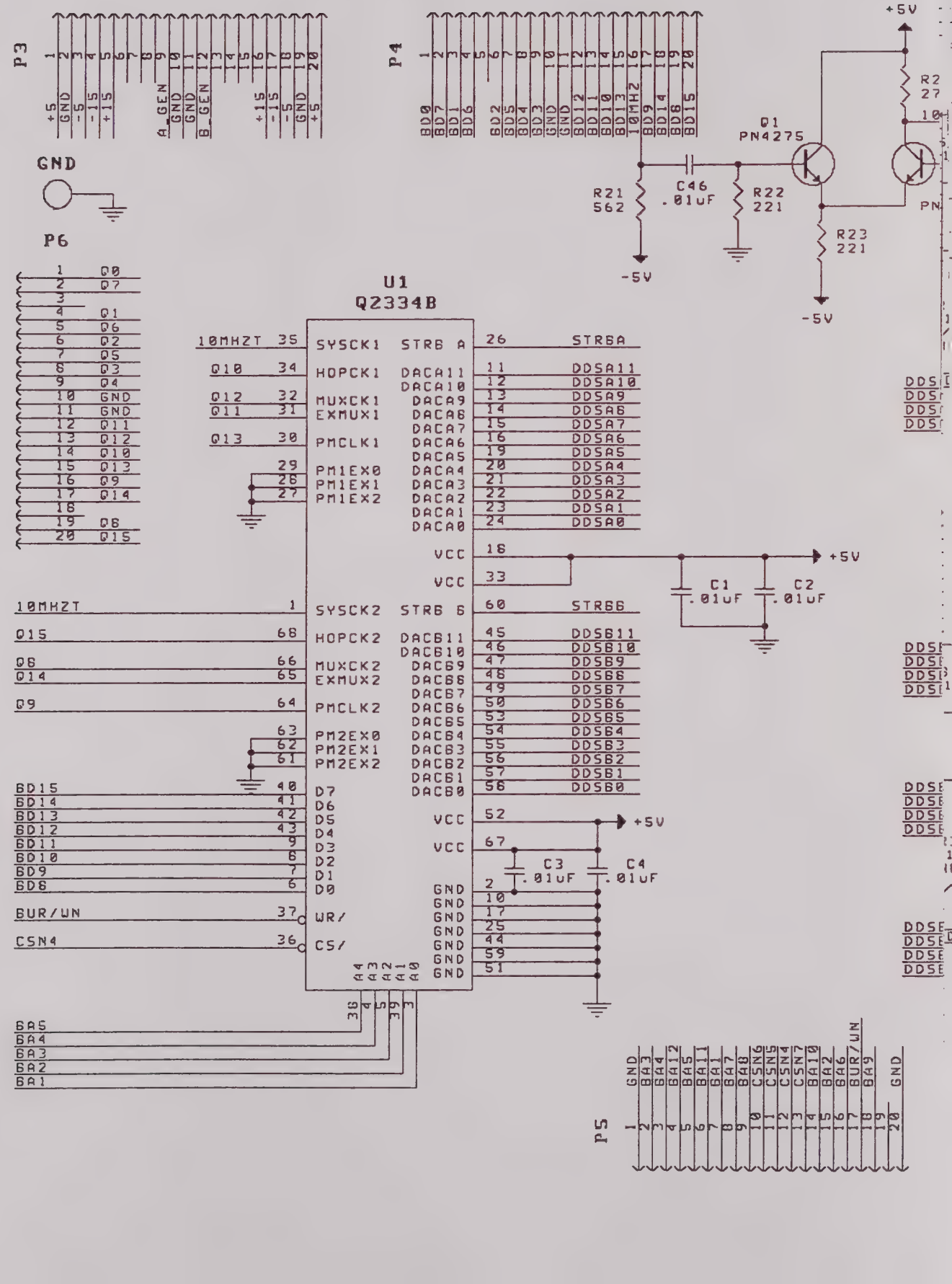


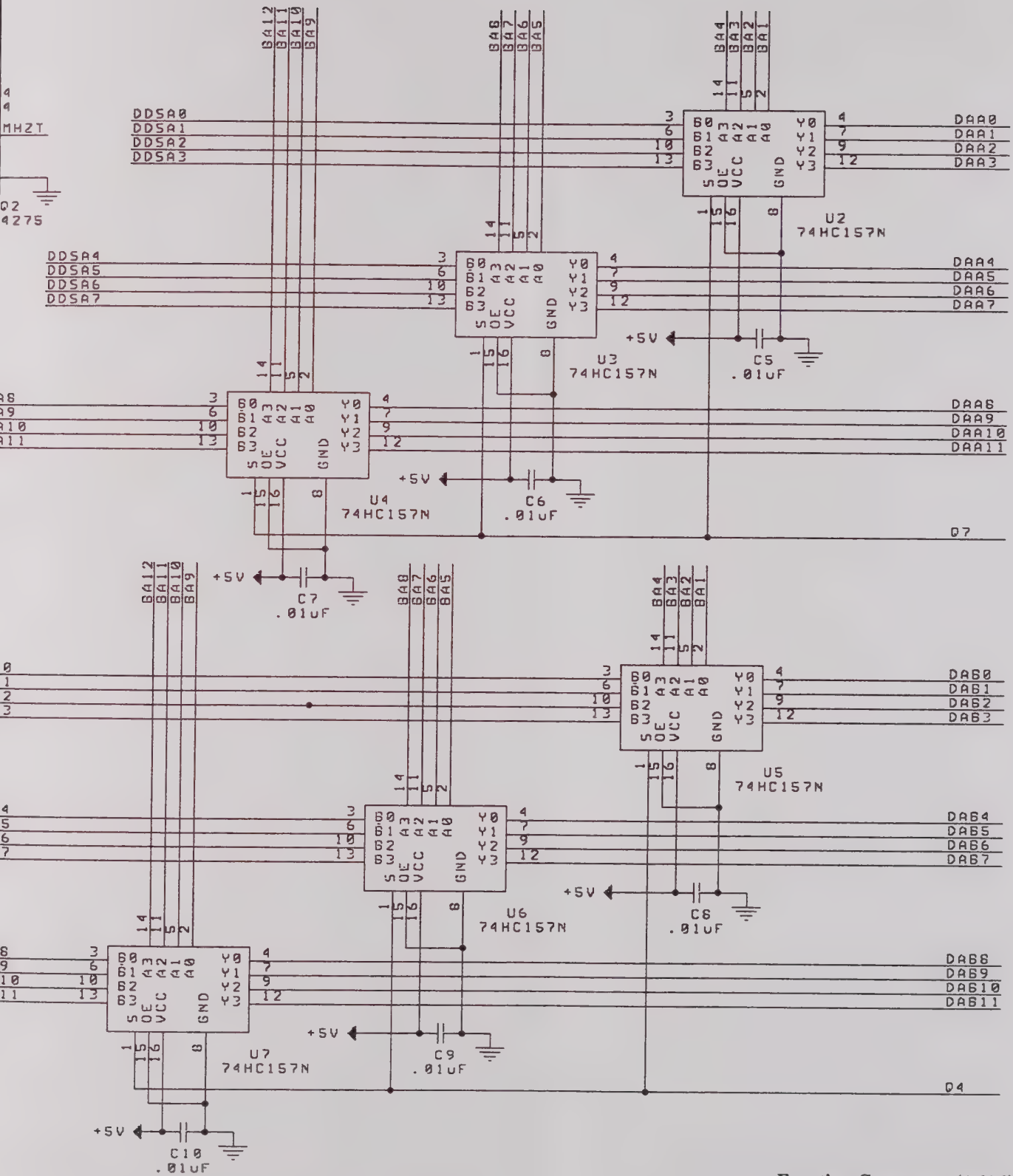

**FUNCTION GENERATOR -- PC ASSY A6A1**

The heart of the Function Generator board is the "Function Generator" chip U1. This IC requires a 10 MHz clock which is supplied external to the board but buffered on board by Q1 and Q2. The IC actually contains two function generators which have been designated as gen A and gen B.

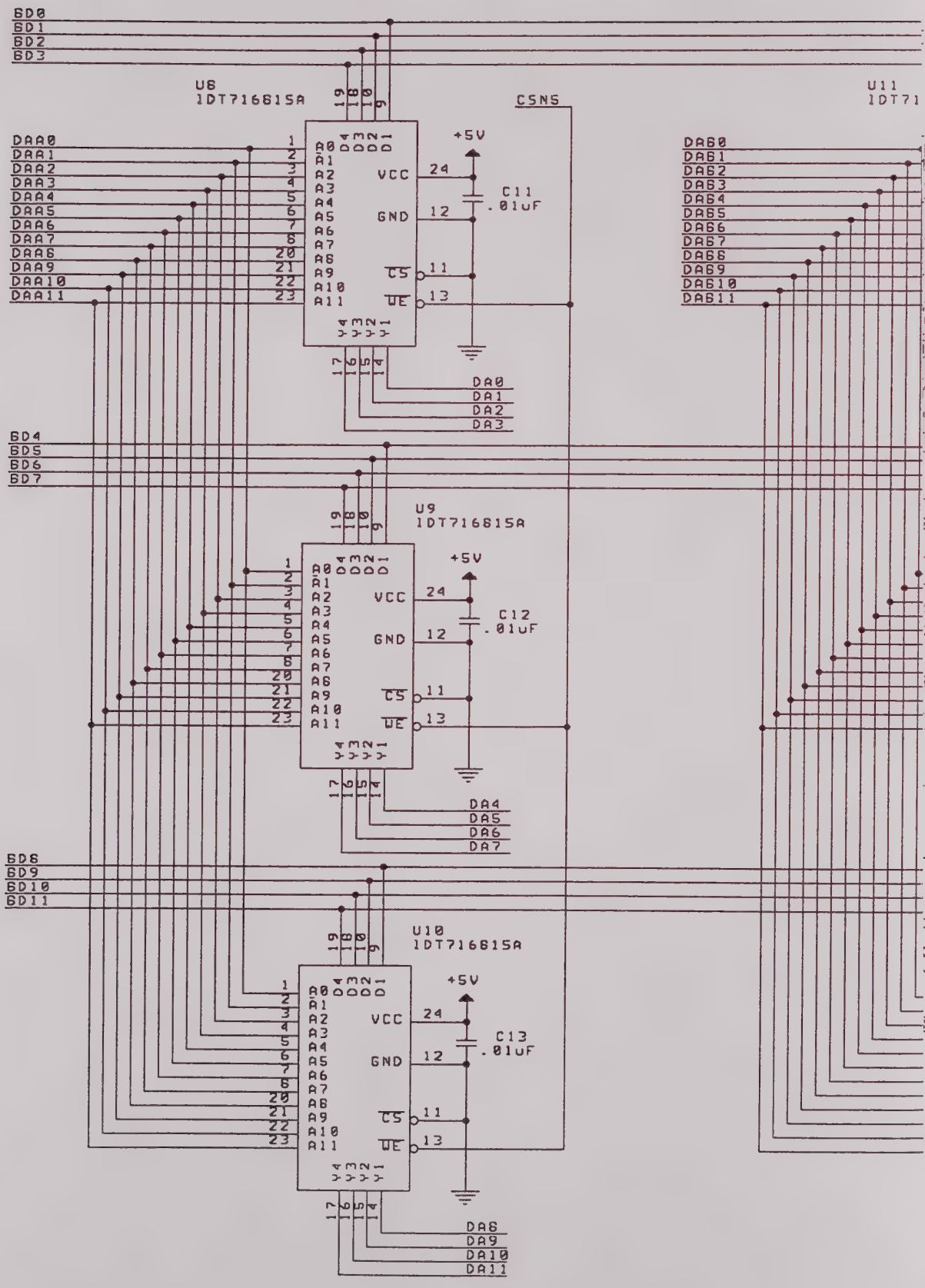
For gen A multiplexers U2, U3 and U4 are used to address RAMs U8, U9 and U10. If INT SINE wave is selected then the computer stores data into the RAMs which is equal to the address which is being programmed. However if INT TRI wave is selected, the computer performs a function on the address data which turns the data from sine data into triangle data and stores the new data into the RAMs. Now a sine or triangle wave is created when the function generator chip outputs data which addresses the RAM and the RAM data becomes DAC U15 input data. The output of this DAC will be the sine or triangle wave (whichever was selected). The components L1, L2, C21, C22, C23 create a low pass filter required to filter out the 10 MHz clock glitches. The SINE CAL pot R4 is used to adjust the amplitude of the sine wave which is then amplified by U16 A the output of which is switched by analog switch U20 or U21. U21 can be switched to allow the sine wave to be converted to a square wave, via U17, the duty cycle of which can be adjusted using R31 and R32. The output of U17 A drives the SQR CAL pot which allows adjustment of the amplitude of the square wave which is then buffered by U16 B before arriving at U20 analog switch. At U20 the Sine or Square wave signal is switched for A_GEN output to the AM/FM Driver PCA (A6).

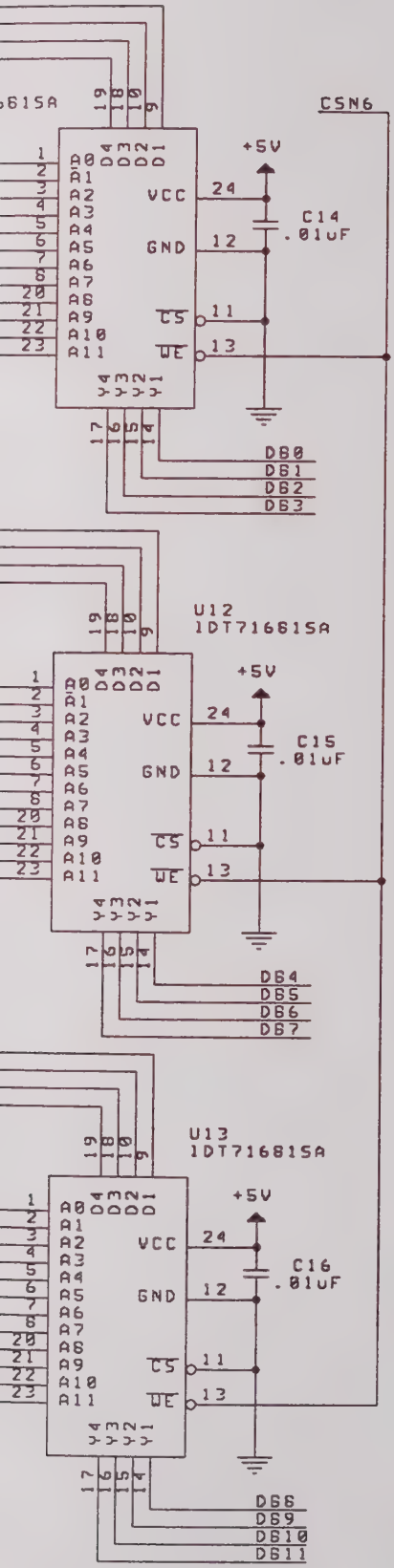
Generator B operates identically to generator A and has its own set of multiplexers U5, U6 and U7, RAM's U11, U12, U13, DAC U18 and sine wave to square wave converter U17 D.


P3
P4
P5
P6
GND
U1
Q2334B
+5V
-5V
R21 562
C46 .01uF
R22 221
R23 221
Q1 PN4275
R2 27
C1 .01uF
C2 .01uF
C3 .01uF
C4 .01uF
10MHZT
SYSCK1
SYSCK2
STRB A
STRB B
STRBA
STRBB
HOPCK1
HOPCK2
MUXCK1
MUXCK2
EXMUX1
EXMUX2
PMCLK1
PMCLK2
PM1EX0
PM1EX1
PM1EX2
PM2EX0
PM2EX1
PM2EX2
DACA11
DACA10
DACA9
DACA8
DACA7
DACA6
DACA5
DACA4
DACA3
DACA2
DACA1
DACA0
DACB11
DACB10
DACB9
DACB8
DACB7
DACB6
DACB5
DACB4
DACB3
DACB2
DACB1
DACB0
DDSA11
DDSA10
DDSA9
DDSA8
DDSA7
DDSA6
DDSA5
DDSA4
DDSA3
DDSA2
DDSA1
DDSA0
DDSB11
DDSB10
DDSB9
DDSB8
DDSB7
DDSB6
DDSB5
DDSB4
DDSB3
DDSB2
DDSB1
DDSB0
VCC
GND
D7
D6
D5
D4
D3
D2
D1
D0
WR/
CS/
BUR/WN
CSN4
BD15
BD14
BD13
BD12
BD11
BD10
BD9
BD8
BA5
BA4
BA3
BA2
BA1
A4
A3
A2
A1
A0
Q0
Q7
Q1
Q6
Q2
Q5
Q3
Q4
Q11
Q12
Q10
Q13
Q9
Q14
Q8
Q15



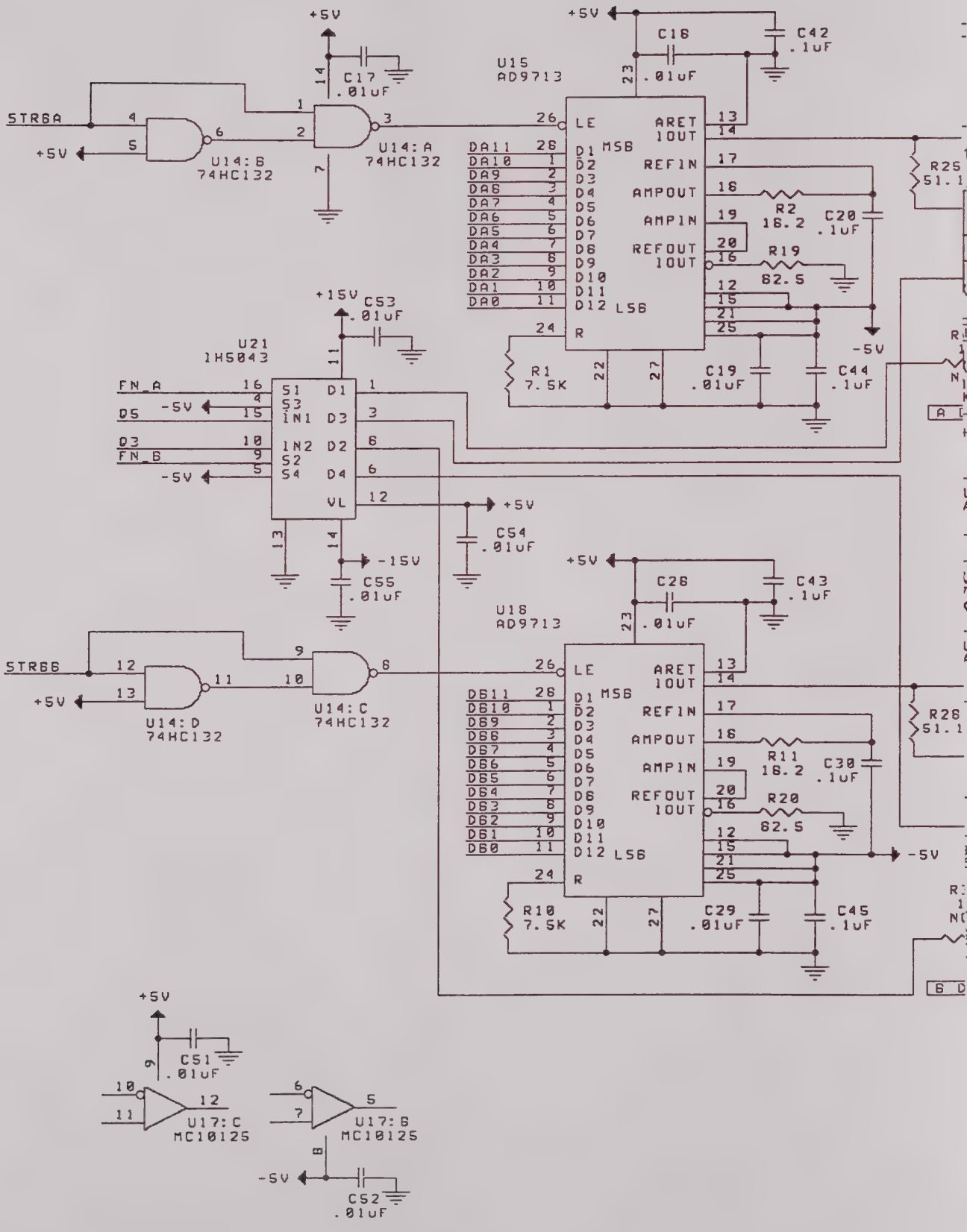

**Function Generator (A6A1)**
**ASSY# 120BA12601 Rev C**
**Sheet 2 of 4**
**7-A6-6**

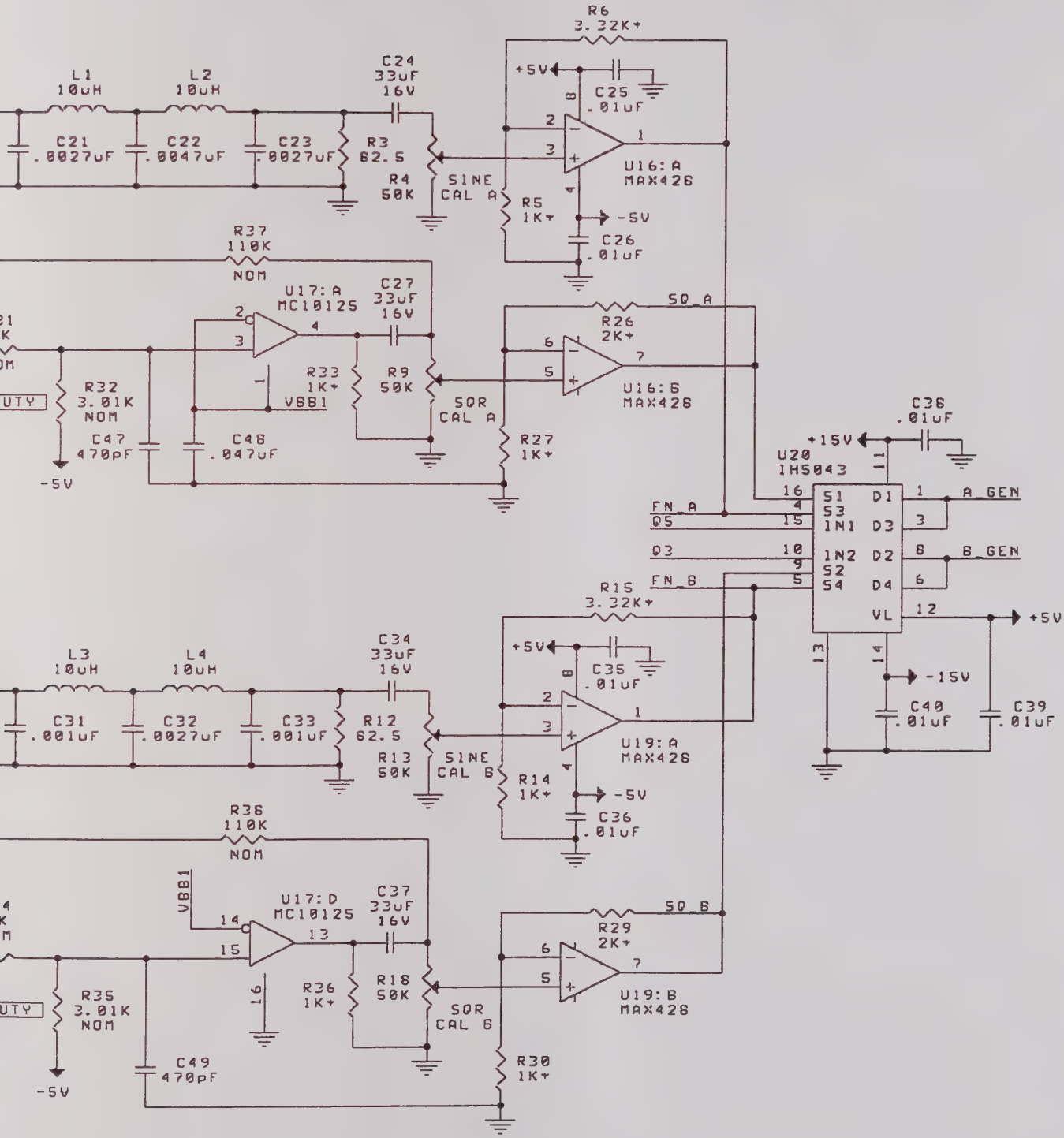

BD0
BD1
BD2
BD3
U8
IDT716815A
CSNS
+5V
DAA0
DAA1
DAA2
DAA3
DAA4
DAA5
DAA6
DAA7
DAA8
DAA9
DAA10
DAA11
VCC
GND
CS
WE
C11
.01uF
DA0
DA1
DA2
DA3
BD4
BD5
BD6
BD7
U9
IDT716815A
C12
.01uF
DA4
DA5
DA6
DA7
BD8
BD9
BD10
BD11
U10
IDT716815A
C13
.01uF
DA8
DA9
DA10
DA11
U11
IDT71
DAB0
DAB1
DAB2
DAB3
DAB4
DAB5
DAB6
DAB7
DAB8
DAB9
DAB10
DAB11



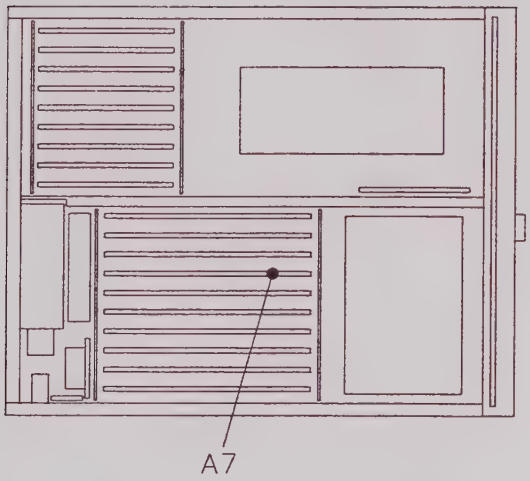

**NOTES: UNLESS OTHERWISE SPECIFIED**

1. CAPACITOR VALUES ARE IN uF
2. RESISTOR VALUES ARE IN OHMS
3. RESISTORS ARE 1/4W, 1%
4. * INDICATES 1/5W, 1% RESISTORS

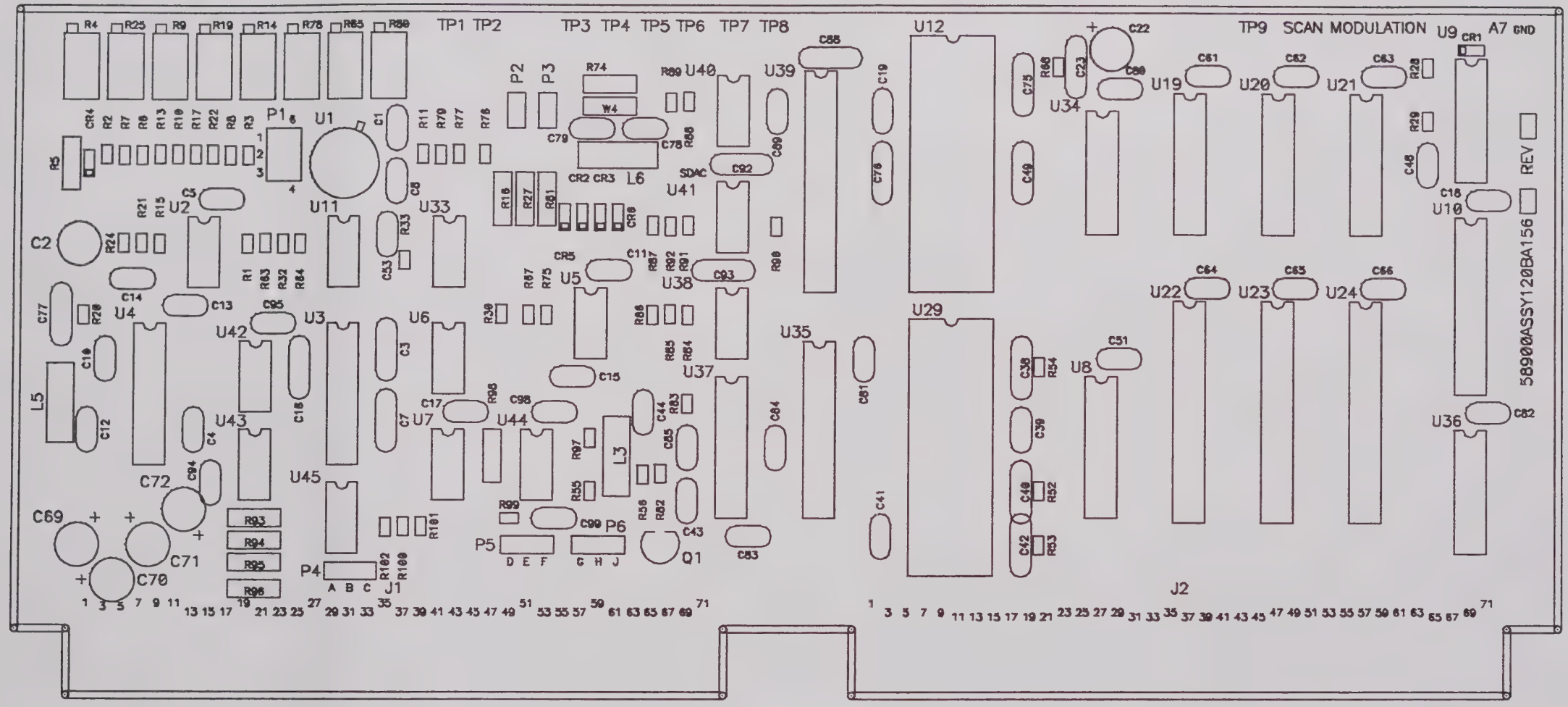

+5V
C17
.01uF
STRBA
U14:B
74HC132
U14:A
74HC132
U15
AD9713
C16
.01uF
C42
.1uF
DA11
DA10
DA9
DA8
DA7
DA6
DA5
DA4
DA3
DA2
DA1
DA0
LE
MSB
LSB
ARET
IOUT
REFIN
AMPOUT
AMPIN
REFOUT
R25
51.1
R2
18.2
C20
.1uF
R19
82.5
-5V
R1
7.5K
C19
.01uF
C44
.1uF
+15V
C53
.01uF
U21
1HS043
FN_A
DS
D3
FN_B
S1
S3
IN1
IN2
S2
S4
D1
D3
D2
D4
VL
C54
.01uF
C55
.01uF
-15V
U18
AD9713
C28
.01uF
C43
.1uF
STRBB
U14:D
74HC132
U14:C
74HC132
DB11
DB10
DB9
DB8
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
R28
51.1
R11
18.2
C30
.1uF
R20
82.5
R10
7.5K
C29
.01uF
C45
.1uF
C51
.01uF
U17:C
MC10125
U17:B
MC10125
C52
.01uF




**Function Generator (A6A1)**
**ASSY# 120BA12601 Rev C**
**Sheet 4 of 4**
**7-A6-8**




**Scan Modulation (A7)**
**ASSY# 120BA15650 Rev 1**
**Sheet 1 of 5**
**7-A7-1**




**SCAN MODULATION -- PC ASSY A7**

This circuit translates the internal or external modulating signal into a control signal for regulating the attenuation of the scan module.

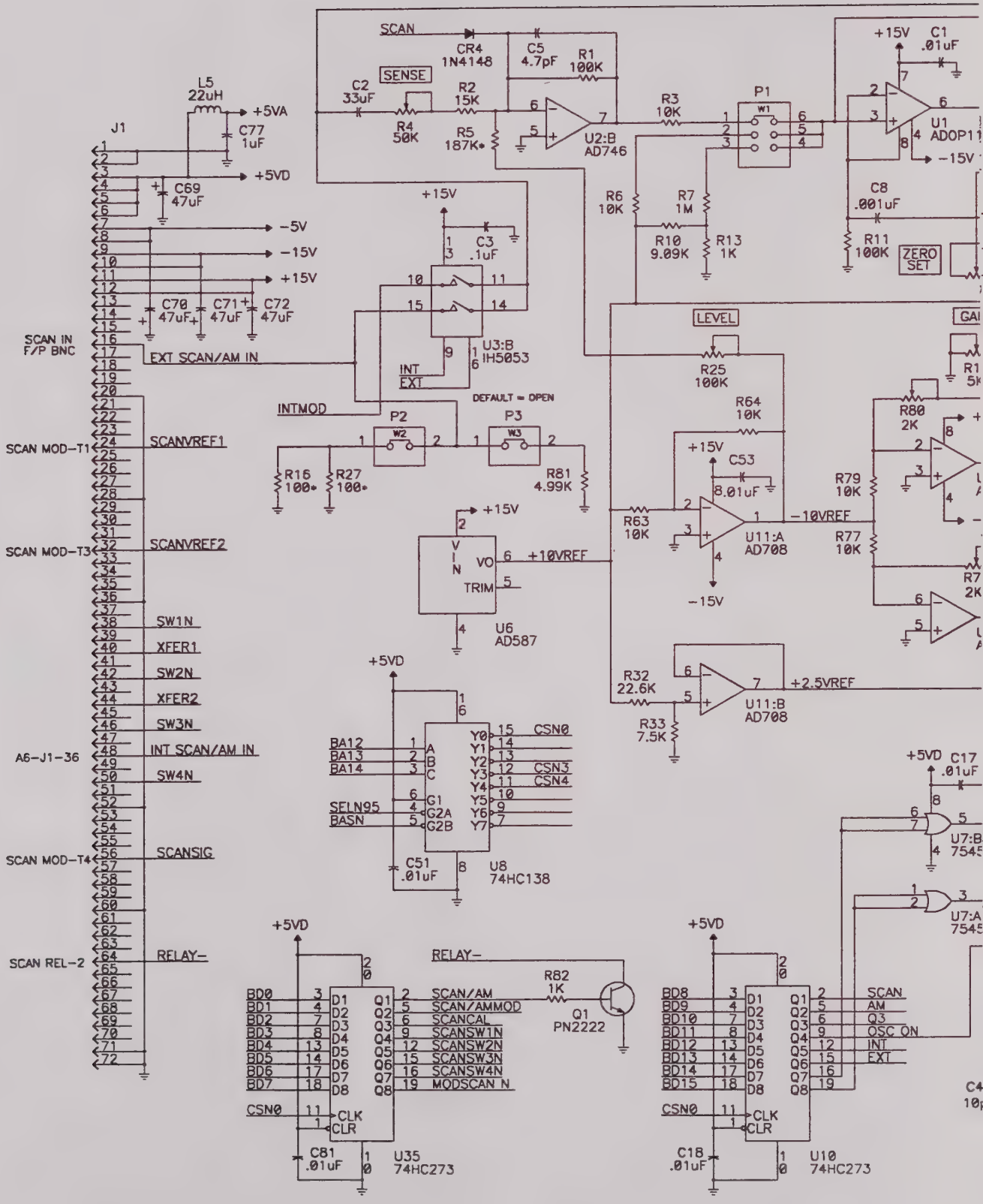
U10 and U35 decode certain control inputs from the computer; U10 activates and deactivates the 10 MHz clock (used to drive DACs and ADCs on this circuit board when they are needed), and U35 switches Q1 on and off to control the relay that switches the scan module into or out of the instrument's RF output path. U11-B generates a reference voltage needed by the analog-to-digital converter U12; U11-A generates a reference voltage needed by U2-B, U33-A, and U33-B; U33-A and U33-B generate reference voltages needed by FETs in the scan module.

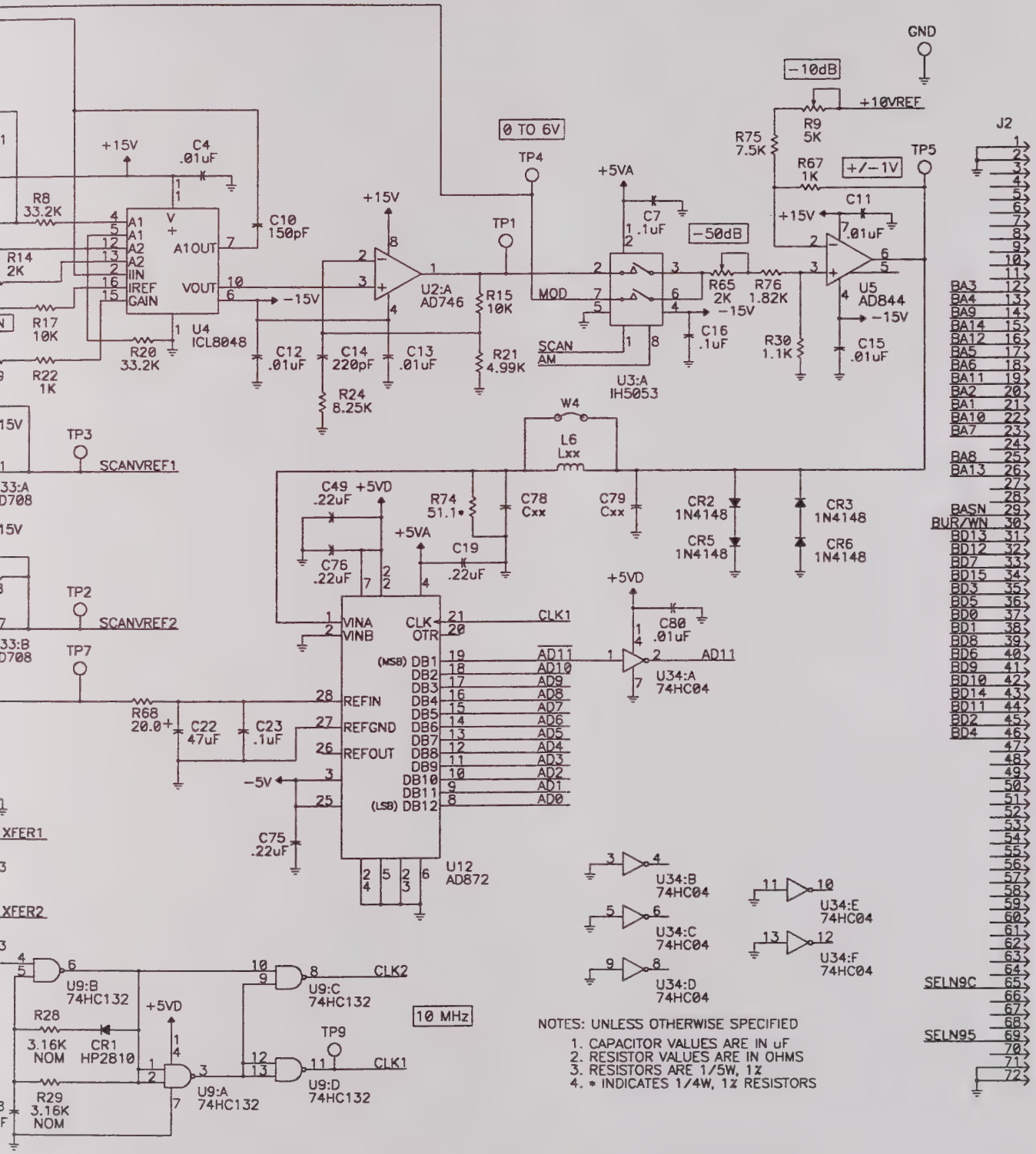
The modulating input signal (internal or external in origin) is received by switch U3-B (jumpers P2 and P3 control the input impedance for the external modulation input; normally it is 50 ohms). Between U3-B and a second switch (U3-A) are two paths for the modulating signal: an 'AM' path which includes scaling and logarithmic amplification circuits (U2-B, U1, U4, U2-A) needed in the 'linear AM' mode, and a 'Scan' path which bypasses these. After U3-A, the modulating signal passes through a shaper circuit (U5) which compresses its range to ±1 V, so that it can drive U12, an analog-to-digital converter.

The digital outputs of the ADC are applied to the address switches (U19, U20, U21) which control addressing of the RAMs U22, U23, and U24; together, these RAMs make up a 4K X 12 volatile memory (scan module correction data are downloaded into this memory from ROM when scan modulation is selected).

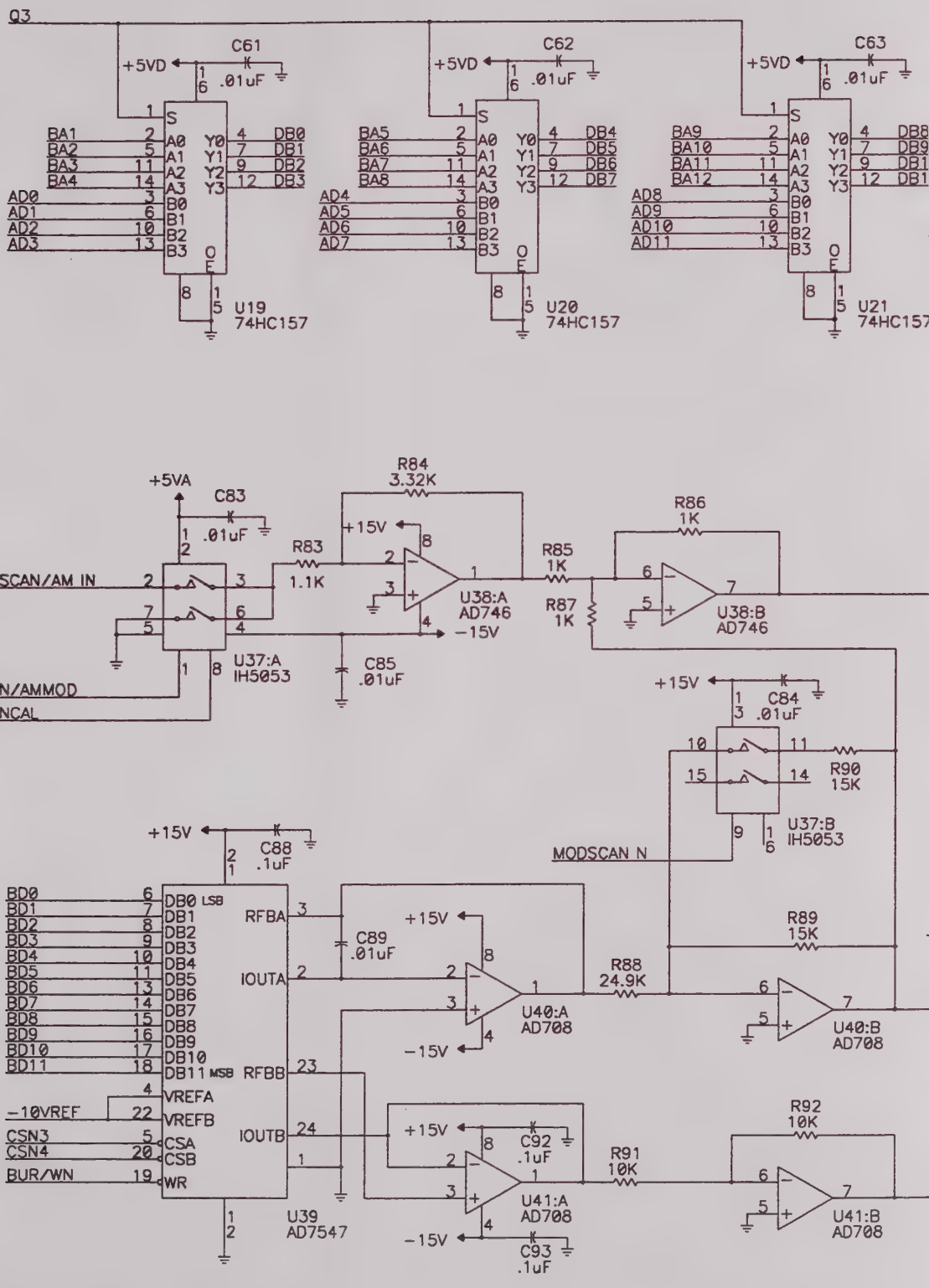
As the modulating input changes, the digital output of the ADC tracks it, retrieving from RAM the appropriate correction data at each point; the data from RAM is applied to the DAC, U29, which converts it into an analog control signal to drive the scan module (via U44 and U45).

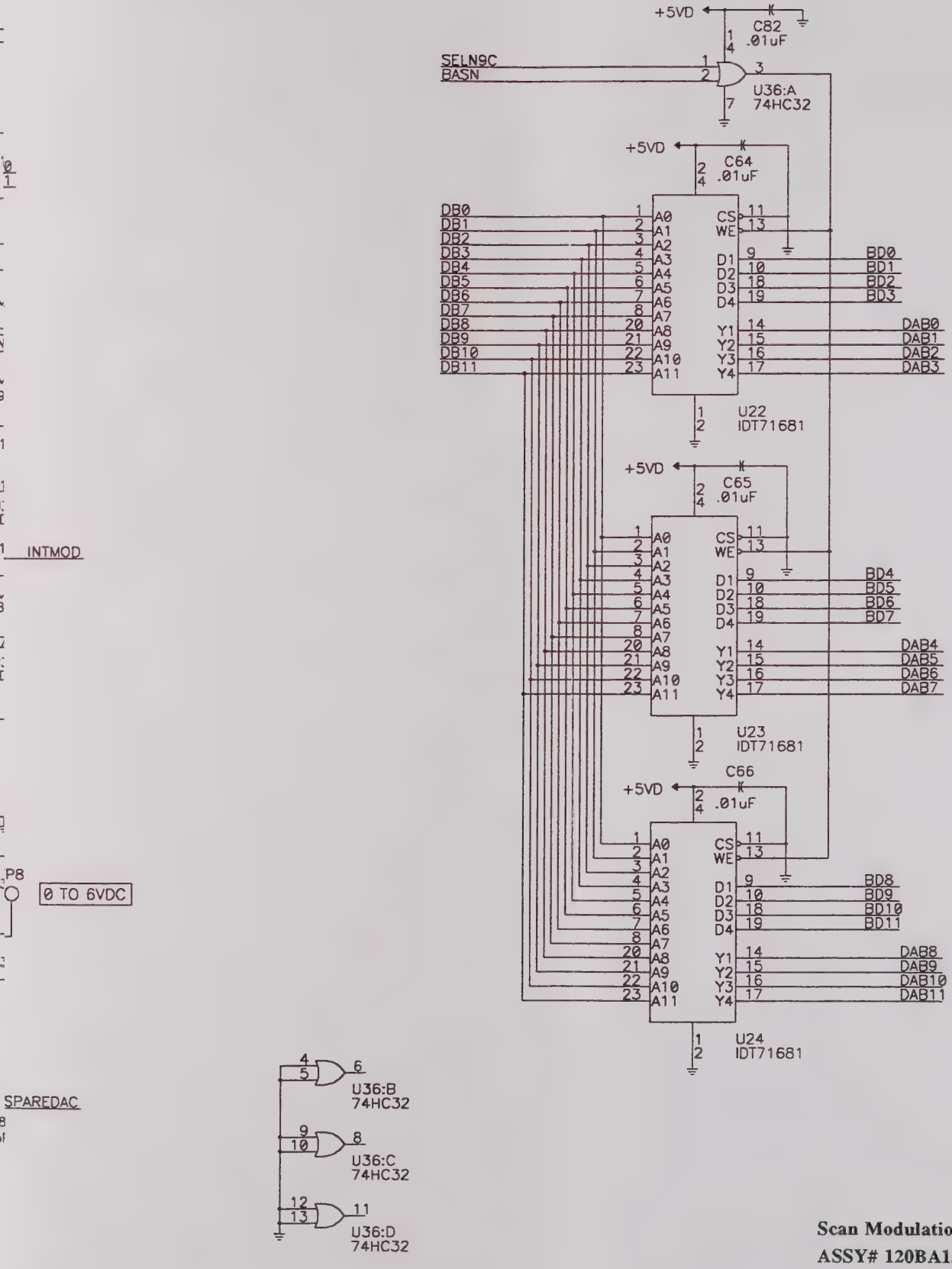
For internal modulation, the DAC, U39, is used by the computer to add an offset to the internal modulating signal, in order to control the depth of modulation. The DAC output, amplified by U40-A and U40-B, is summed with the internal modulating signal at U38-6. Switch U37-B controls the gain of U40-B, which is reduced by half when the variable attenuation mode is selected.


SCAN
CR4
1N4148
C5
4.7pF
R1
100K
SENSE
C2
33uF
R2
15K
R4
50K
R5
187K*
U2:B
AD746
R3
10K
P1
W1
+15V
C1
.01uF
U1
ADOP11
-15V
C8
.001uF
R6
10K
R7
1M
R10
9.09K
R13
1K
R11
100K
ZERO
SET
L5
22uH
+5VA
C77
1uF
J1
+5VD
C69
47uF
-5V
-15V
+15V
C70
47uF
C71
47uF
C72
47uF
C3
.1uF
U3:B
1H5053
INT
EXT
SCAN IN
F/P BNC
EXT SCAN/AM IN
DEFAULT = OPEN
INTMOD
P2
W2
P3
W3
R16
100*
R27
100*
R81
4.99K
LEVEL
R25
100K
R64
10K
R80
2K
C53
.01uF
R79
10K
R63
10K
U11:A
AD708
-10VREF
R77
10K
SCAN MOD-T1
SCANVREF1
SCAN MOD-T3
SCANVREF2
VIN
VO
TRIM
+10VREF
U6
AD587
SW1N
XFER1
SW2N
XFER2
SW3N
A6-J1-36
INT SCAN/AM IN
SW4N
R32
22.6K
R33
7.5K
U11:B
AD708
+2.5VREF
BA12
BA13
BA14
SELN95
BASN
CSN0
CSN3
CSN4
C51
.01uF
U8
74HC138
C17
.01uF
U7:B
7545
U7:A
7545
SCAN MOD-T4
SCANSIG
SCAN REL-2
RELAY-
R82
1K
Q1
PN2222
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
SCAN/AM
SCAN/AMMOD
SCANCAL
SCANSW1N
SCANSW2N
SCANSW3N
SCANSW4N
MODSCAN N
CLK
CLR
C81
.01uF
U35
74HC273
BD8
BD9
BD10
BD11
BD12
BD13
BD14
BD15
SCAN
AM
Q3
OSC ON
INT
EXT
C18
.01uF
U10
74HC273

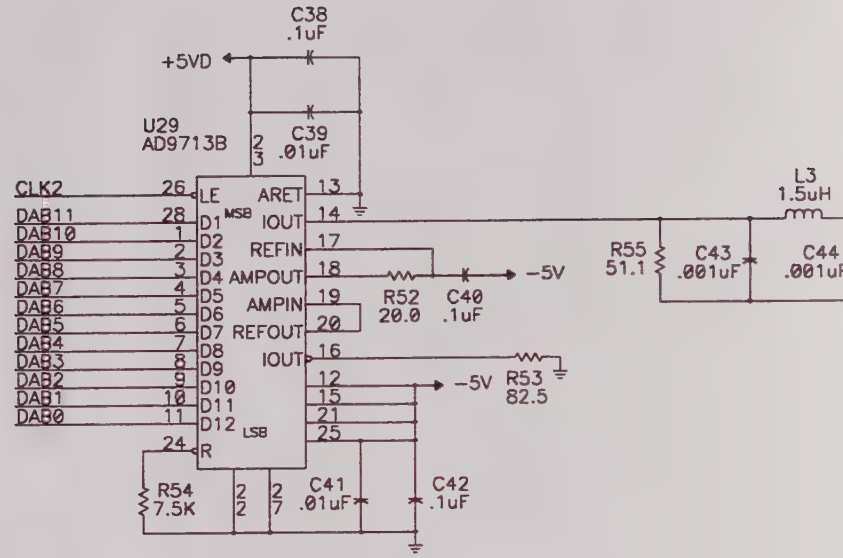


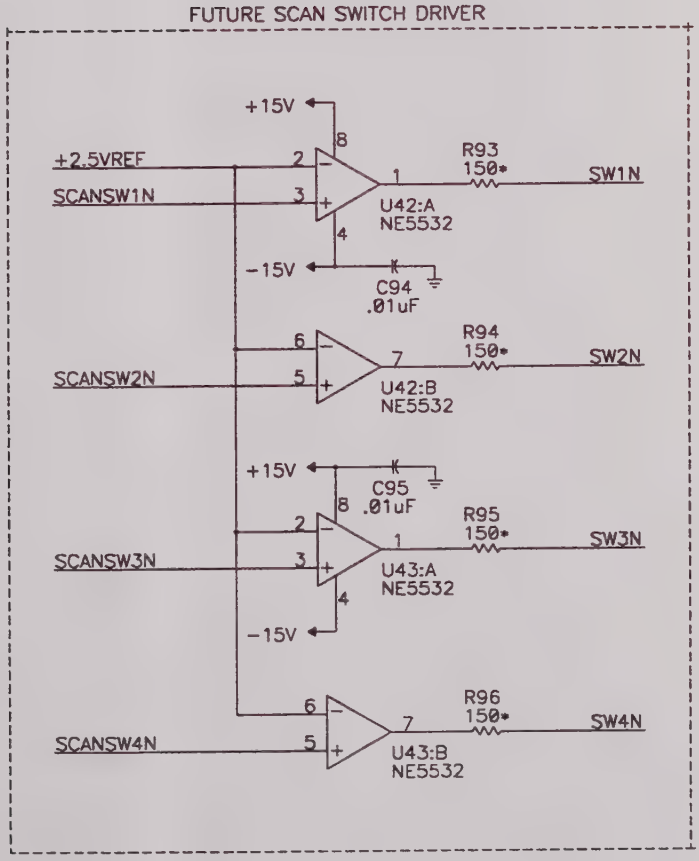

**Scan Modulation (A7)**
**ASSY# 120BA15650 Rev 1**
**Sheet 3 of 5**
**7-A7-3**

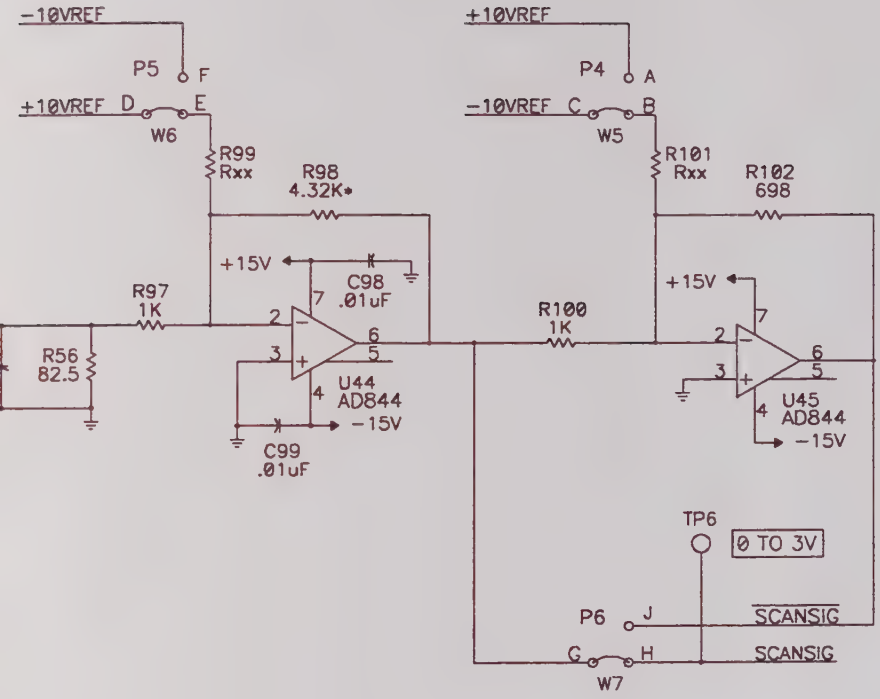

Q3
C61
+5VD
.01uF
BA1
BA2
BA3
BA4
AD0
AD1
AD2
AD3
DB0
DB1
DB2
DB3
U19
74HC157
C62
BA5
BA6
BA7
BA8
AD4
AD5
AD6
AD7
DB4
DB5
DB6
DB7
U20
74HC157
C63
BA9
BA10
BA11
BA12
AD8
AD9
AD10
AD11
DB8
DB9
DB1
U21
74HC157
+5VA
C83
R84
3.32K
+15V
R83
1.1K
R85
1K
R86
1K
INT SCAN/AM IN
U38:A
AD746
−15V
R87
1K
U38:B
AD746
U37:A
IH5053
C85
.01uF
SCAN/AMMOD
SCANCAL
C84
MODSCAN N
R90
15K
U37:B
IH5053
C88
.1uF
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
BD8
BD9
BD10
BD11
DB0 LSB
DB11 MSB
RFBA
IOUTA
RFBB
IOUTB
−10VREF
VREFA
VREFB
CSN3
CSN4
BUR/WN
CSA
CSB
WR
U39
AD7547
C89
.01uF
R88
24.9K
R89
15K
U40:A
AD708
U40:B
AD708
C92
.1uF
C93
.1uF
R91
10K
R92
10K
U41:A
AD708
U41:B
AD708



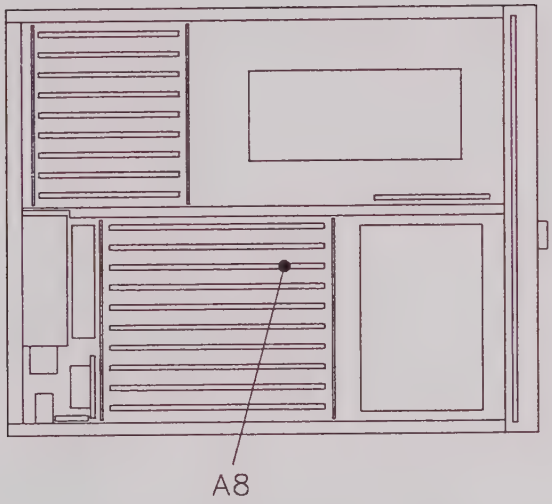

**Scan Modulation (A7)**
**ASSY# 120BA15650 Rev 1**
**Sheet 4 of 5**
**7-A7-4**


C38
.1uF
+5VD
U29
AD9713B
C39
.01uF
CLK2
DAB11
DAB10
DAB9
DAB8
DAB7
DAB6
DAB5
DAB4
DAB3
DAB2
DAB1
DAB0
LE
MSB
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
LSB
R
ARET
IOUT
REFIN
AMPOUT
AMPIN
REFOUT
IOUT
-5V
R52
20.0
C40
.1uF
R53
82.5
R54
7.5K
C41
.01uF
C42
.1uF
L3
1.5uH
R55
51.1
C43
.001uF
C44
.001uF

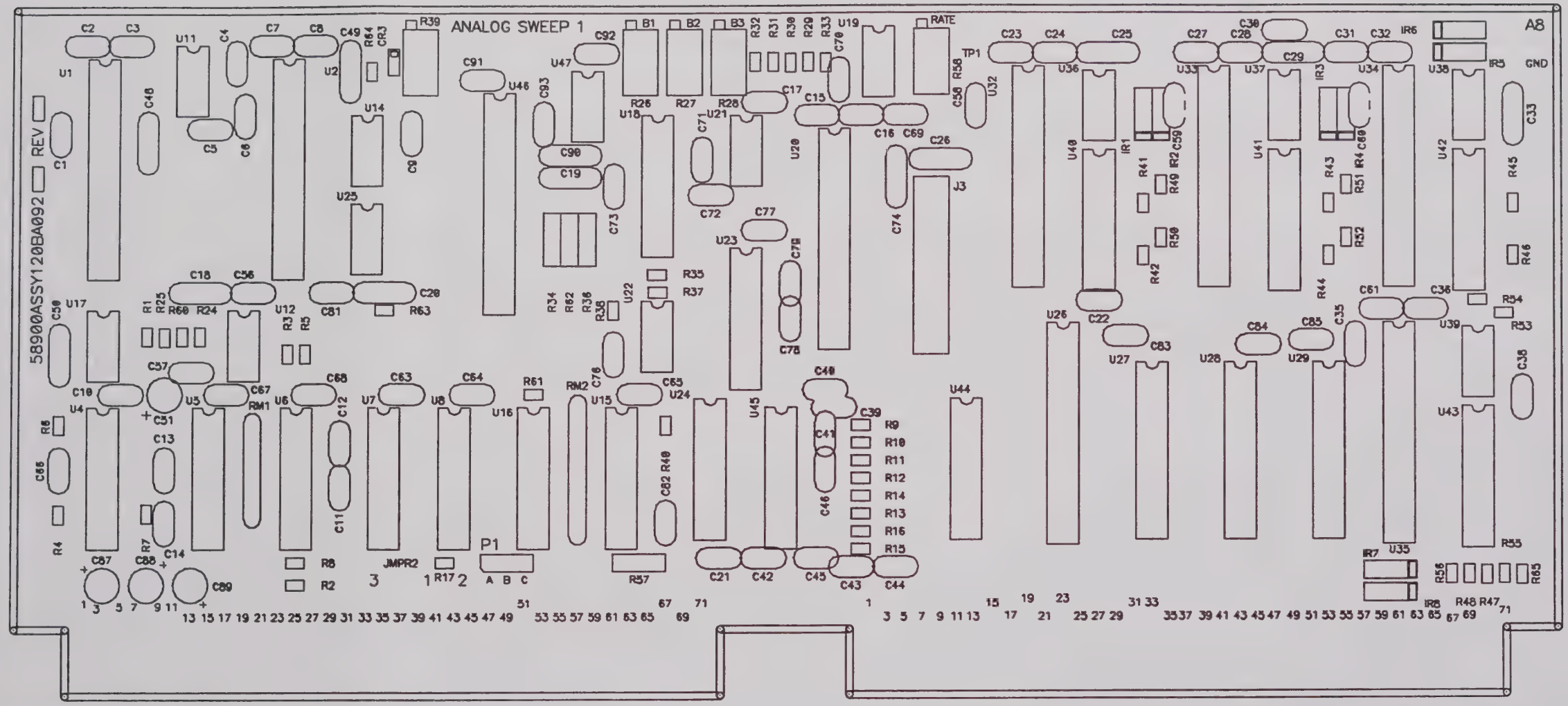

FUTURE SCAN SWITCH DRIVER
+15V
+2.5VREF
SCANSW1N
U42:A
NE5532
R93
150*
SW1N
-15V
C94
.01uF
SCANSW2N
U42:B
NE5532
R94
150*
SW2N
+15V
C95
.01uF
SCANSW3N
U43:A
NE5532
R95
150*
SW3N
-15V
SCANSW4N
U43:B
NE5532
R96
150*
SW4N




**Scan Modulation (A7)**
**ASSY# 120BA15650 Rev 1**
**Sheet 5 of 5**
**7-A7-5**




**Analog Sweep #1 (A8)**
**ASSY# 120BA09211 Rev A**
**Sheet 1 of 5**
**7-A8-1**




**ANALOG SWEEP #1 -- PC ASSY A8**

The analog sweep board provides many signals required during analog sweep. The board has DACs which provide ramps for driving the main tune coils of the YIGs. It also has DACs to provide ramp voltages which trigger a number of comparators, thus generating various logic signals necessary to switch various filters and bands. Another set of DACs is used to control comparator reference voltages according to the marker frequencies which may be set. These comparators then generate the marker pulses.

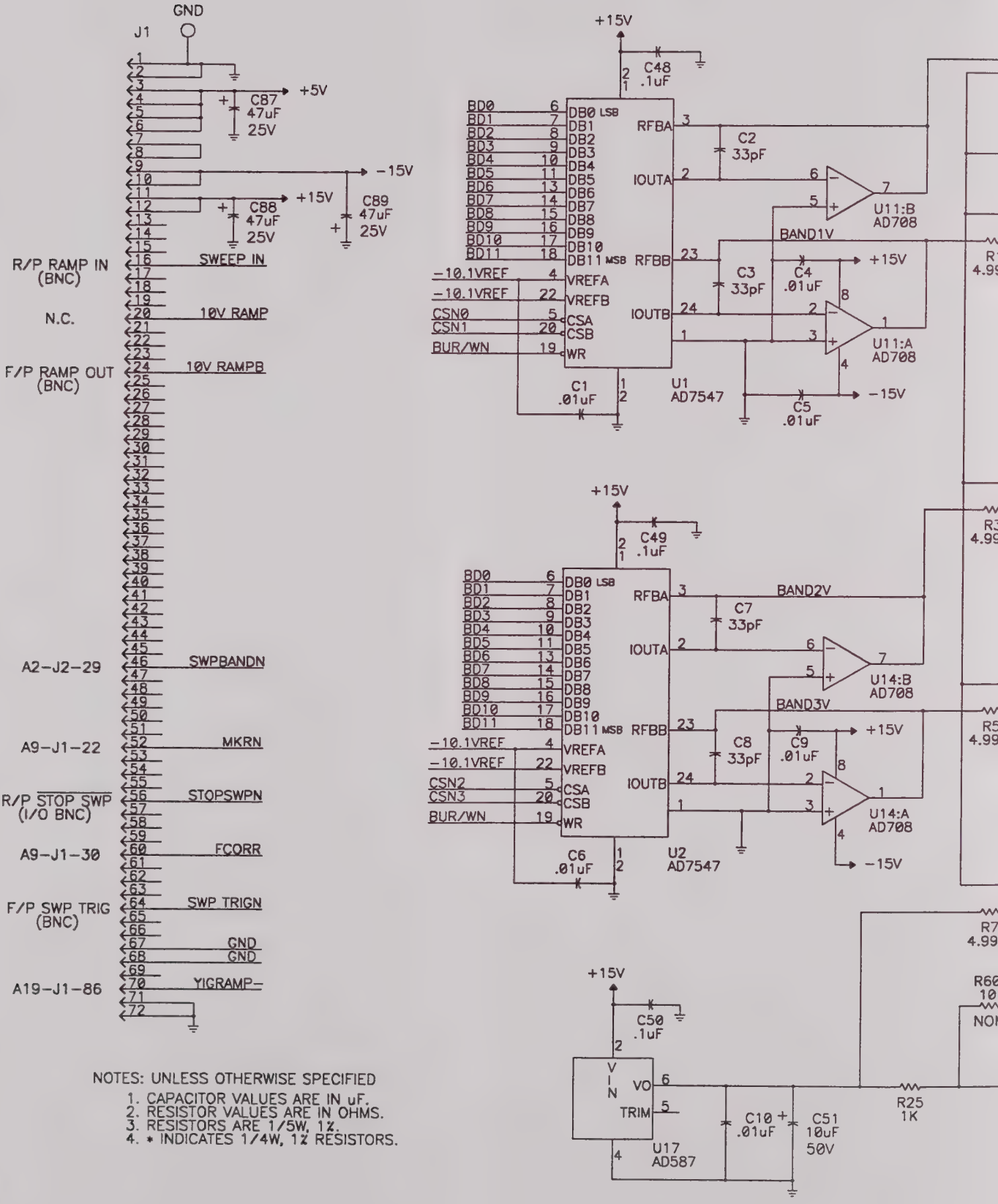
The DAC U1 section A gives a DC voltage at the output of U11 B which determines the rate at which the unit sweeps. DACs U1 B, U2 A and B are set up to give a voltage at the output of their respective amplifiers (U11 A, U14 B and A) which corresponds to frequency band changes (at 2, 8 and 20 GHz). Specifically, for the 2 GHz band switch point the voltage from U11-1 is the reference voltage for comparator U4 D. The 10V_RAMP from A8A1 is the other input to the comparator. When the ramp voltage reaches the reference voltage the comparator switches, resulting in a pulse at U6-8 which propagates thru U7 and U16, clocking flip flop U8 A. This causes the Q-not output to go low signaling the computer that a band change must take place. This Q-not output also causes the hold line (U15-10) to trigger thereby stopping the ramp on the A8A1 board. In addition the signal is output to the rear panel as the STOP SWP I/O logic signal. When the band change is complete the computer sends a signal CONTN to reset the flip flop U8. The 8 and 20 GHz band changes work similarly.

The 10 volt reference from U17 is inverted by U12 giving a negative reference. The +10V reference is used as the reference for the U4 C comparator. This comparator switches at the end of each sweep and generates a pulse. When the SWP_TRIGN signal is received, (this signal is produced by the front panel SWP TRIG input) U15 A and U8 B cause the RAMP_RESET line to reset the ramp voltage on A8A1.

The 10V_RAMP is applied to U19 A where it is inverted and then summed at U19 B with different offset voltages, switched by U18, at each band change. These offset voltages cause the ramp at U19-7 to start at 0V for each new band. The amplitude of the ramp is then adjusted by DAC U20 section A and B (using both sections gives a greater range). The resulting ramp is buffered by U47 B and summed together at U22 B with other signals, including the frequency correction signal from the digital ramp board A9. The switch U23 can then select the ramp or an inverted version of this ramp (U22 A) for output to the YIG driver, depending on whether the frequency sweep is increasing or decreasing. Another signal is summed into the ramp at U22 B; this signal is YIG lag compensation. At the start of each band U16 C triggers U24 A causing a pulse at the Q output. The negative going pulse at U25 A is turned into a negative going spike with decay by the diode CR3 and C20. This is buffered by U25 B and its amplitude is adjusted by DAC U46 according to the sweep rate. The amplitude of the spike is maximum for the highest sweep rate. The output of U47 A is then summed with the frequency correction and the ramp voltage at U22 B.

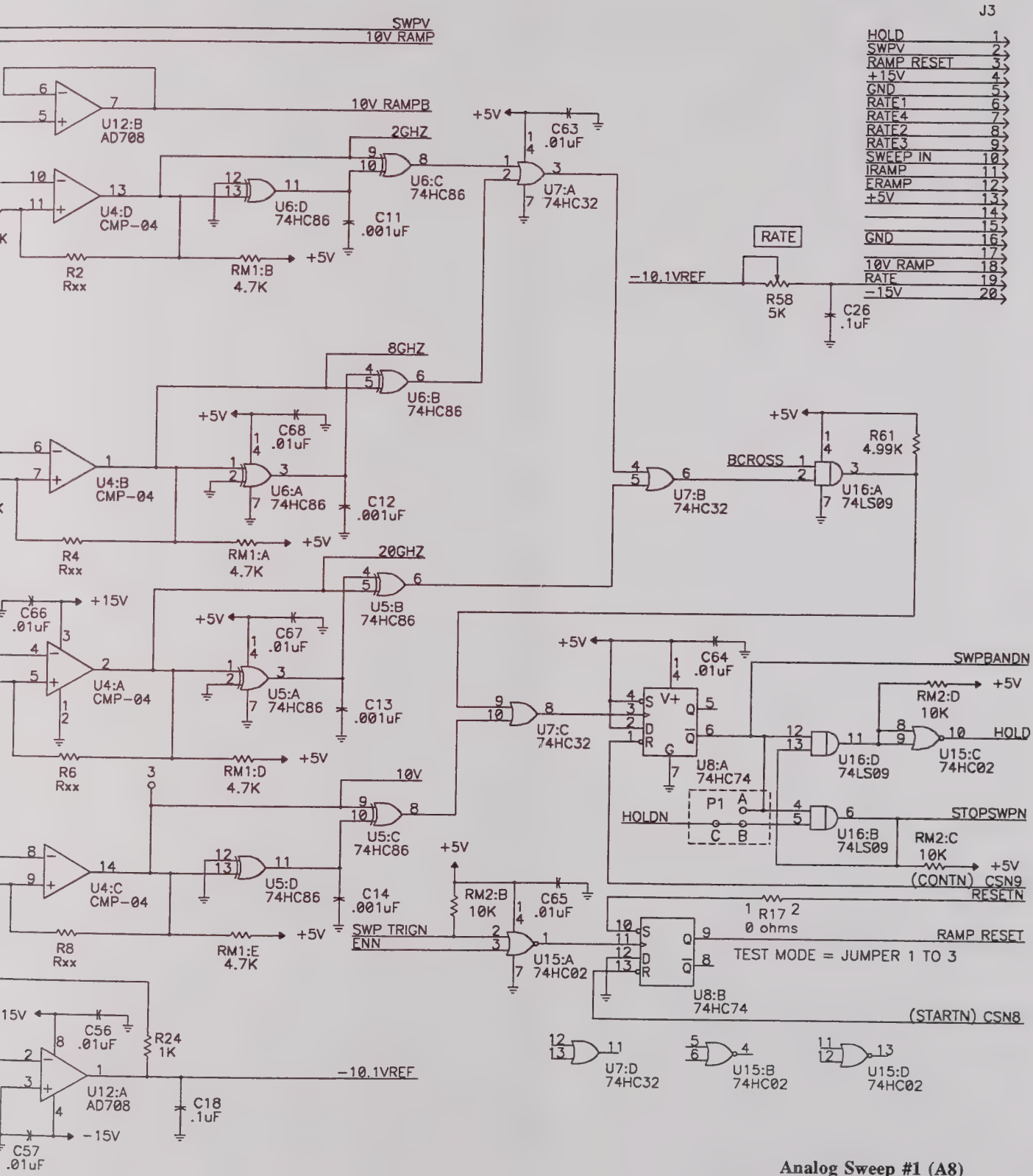
U32 thru U35 DACs provide reference voltages for up to 8 analog sweep markers. For example, when a marker is set, DAC U32 A generates a reference voltage at U36-7 for comparators U40 C and D. When the 10V_RAMP reaches the reference voltage the comparators flip, generating a marker pulse at the output U40 pin 13 and 14. The width of this pulse is determined by IR1 and R41. The pulse then propagates thru U45 and is buffered to be supplied to the rear panel. The rest of the markers are generated in the same way and are NOR'ed together at U45.

U44 and U26 decode chip selects for the board. U27, U28 and U29 provide buffering necessary for computer bus interface.

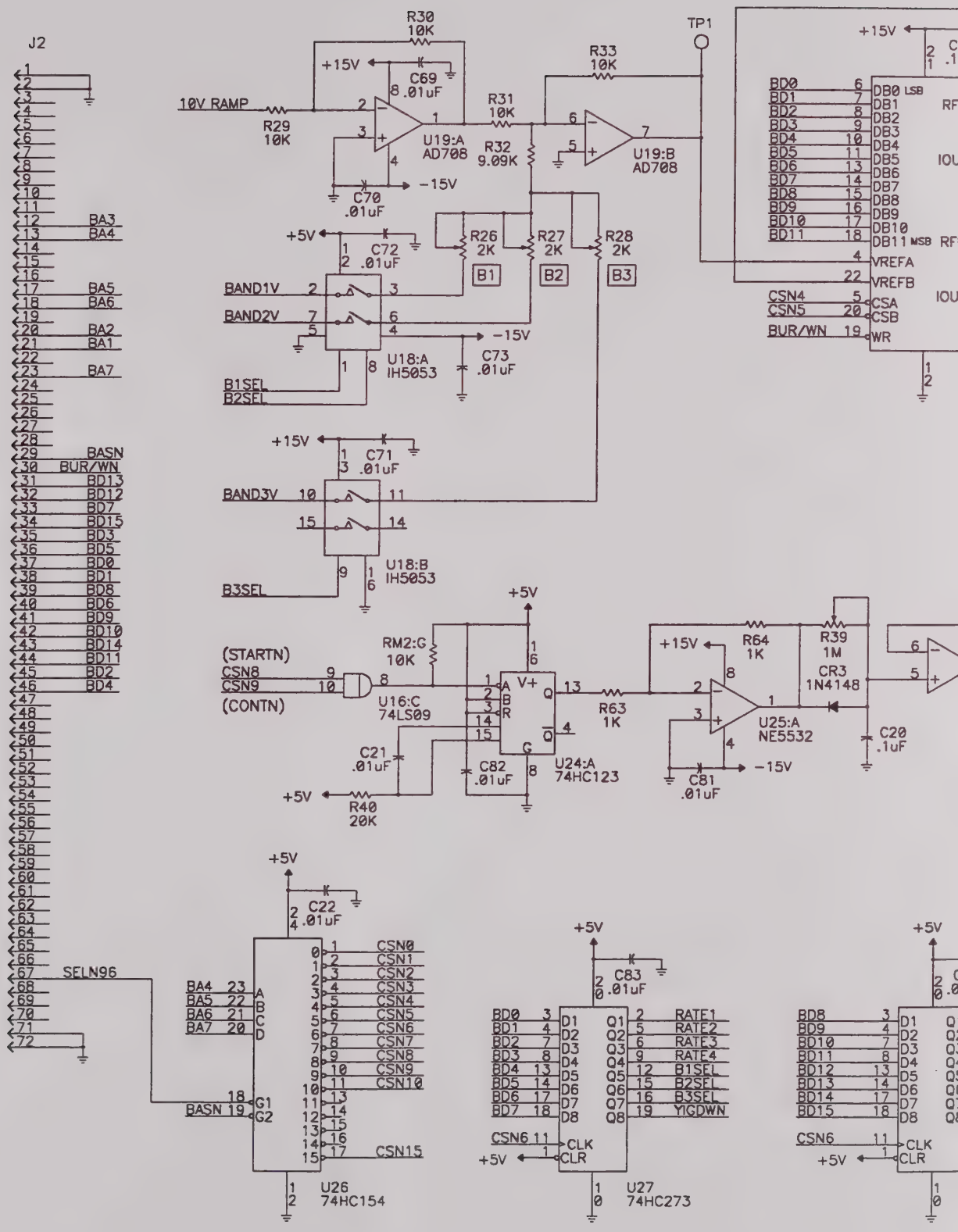


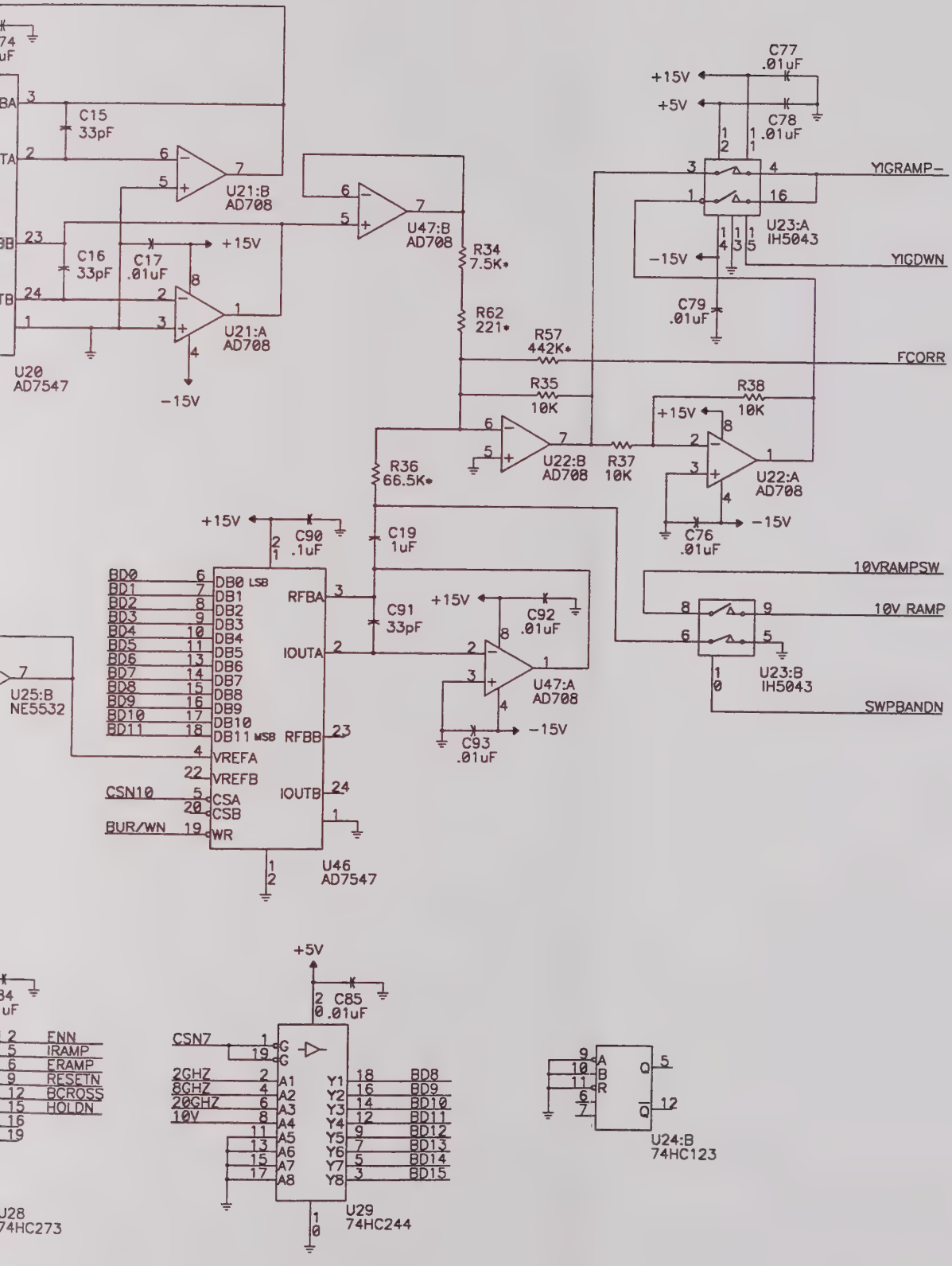

NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPACITOR VALUES ARE IN uF.
2. RESISTOR VALUES ARE IN OHMS.
3. RESISTORS ARE 1/5W, 1%.
4. * INDICATES 1/4W, 1% RESISTORS.

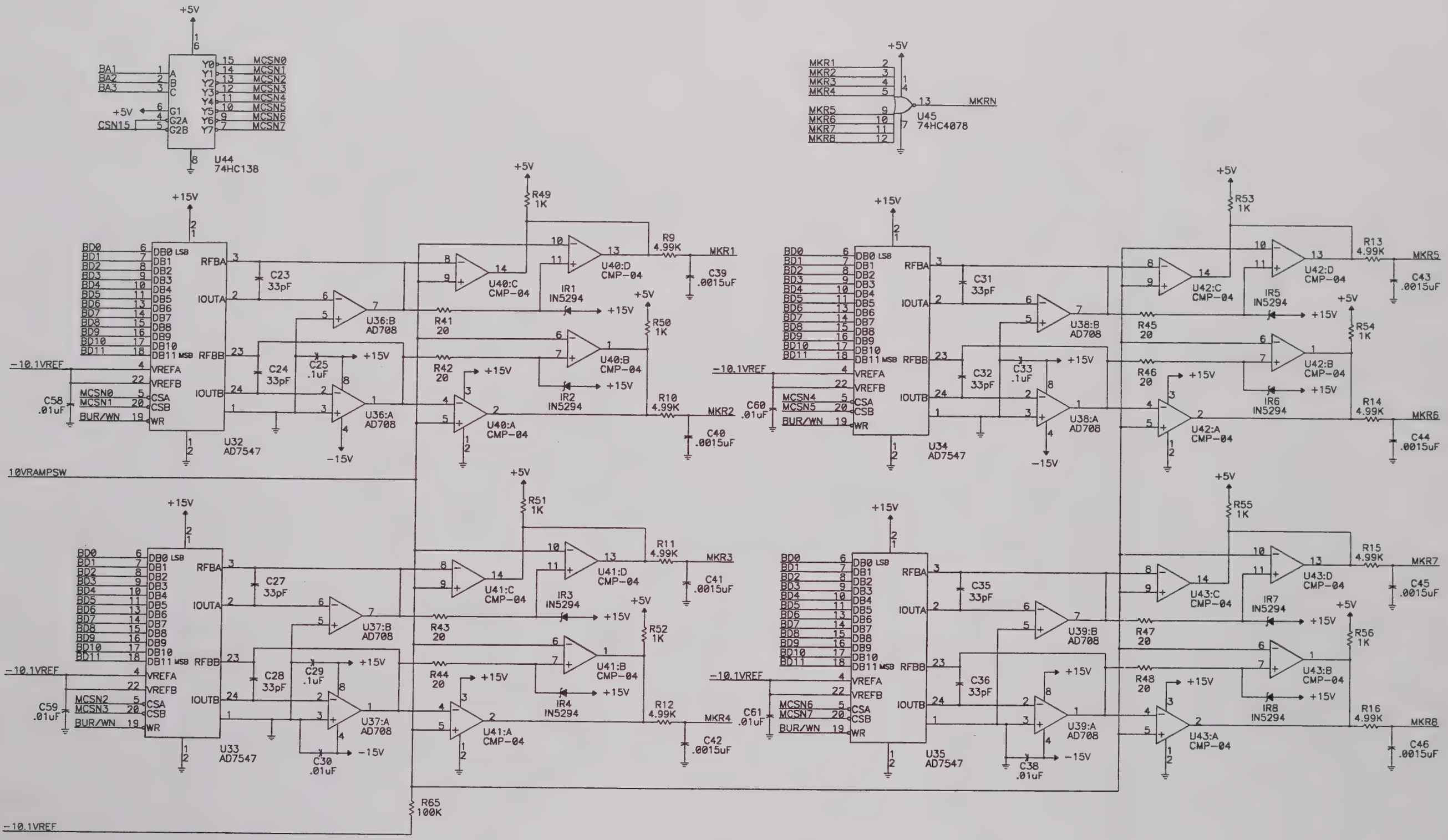



**Analog Sweep #1 (A8)**
**ASSY# 120BA09211 Rev A**
**Sheet 3 of 5**
**7-A8-3**

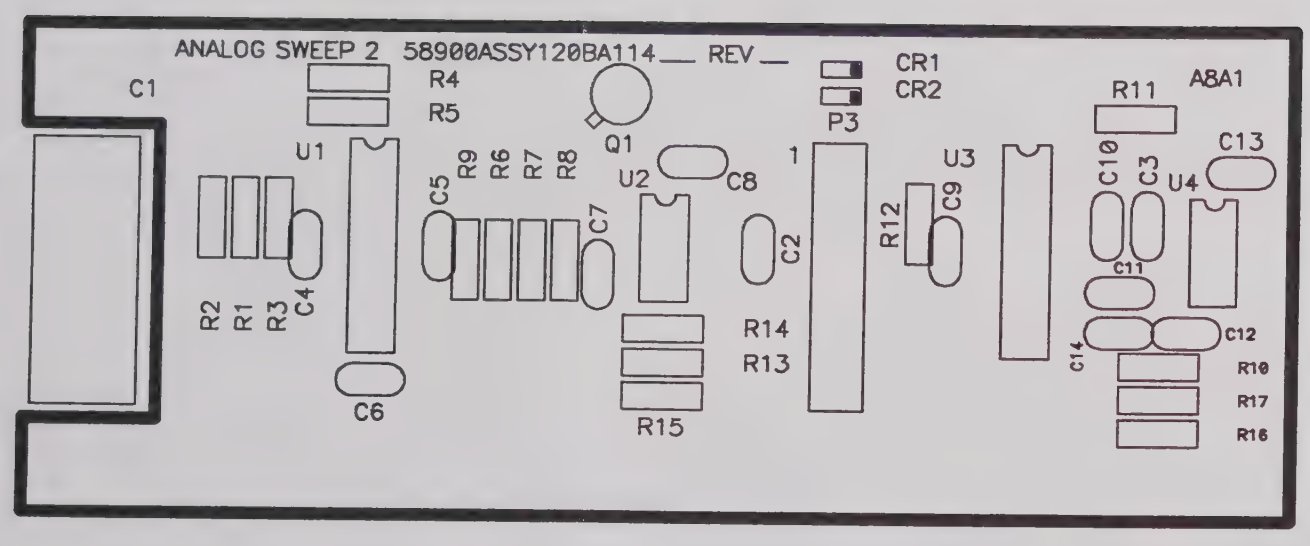

J2
BA3
BA4
BA5
BA6
BA2
BA1
BA7
BASN
BUR/WN
BD13
BD12
BD7
BD15
BD3
BD5
BD0
BD1
BD8
BD6
BD9
BD10
BD14
BD11
BD2
BD4
SELN96
R30 10K
+15V
C69 .01uF
10V RAMP
R29 10K
U19:A AD708
R31 10K
R33 10K
TP1
R32 9.09K
U19:B AD708
C70 .01uF
-15V
+5V
C72 .01uF
R26 2K
R27 2K
R28 2K
B1
B2
B3
BAND1V
BAND2V
U18:A IH5053
C73 .01uF
B1SEL
B2SEL
C71 .01uF
BAND3V
U18:B IH5053
B3SEL
(STARTN)
CSN8
CSN9
(CONTN)
RM2:G 10K
U16:C 74LS09
U24:A 74HC123
C21 .01uF
C82 .01uF
R40 20K
R63 1K
R64 1K
R39 1M
CR3 1N4148
U25:A NE5532
C20 .1uF
C81 .01uF
C22 .01uF
BA4
BA5
BA6
BA7
BASN
G1
G2
CSN0
CSN1
CSN2
CSN3
CSN4
CSN5
CSN6
CSN7
CSN8
CSN9
CSN10
CSN15
U26 74HC154
C83 .01uF
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
RATE1
RATE2
RATE3
RATE4
B1SEL
B2SEL
B3SEL
YIGDWN
CSN6
CLK
CLR
U27 74HC273
BD8
BD9
BD10
BD11
BD12
BD13
BD14
BD15
BD0 LSB
BD11 MSB
DB0 LSB
DB11 MSB
VREFA
VREFB
CSN4
CSN5
CSA
CSB
BUR/WN
WR




**Analog Sweep #1 (A8)**
**ASSY# 120BA09211 Rev A**
**Sheet 4 of 5**
**7-A8-4**



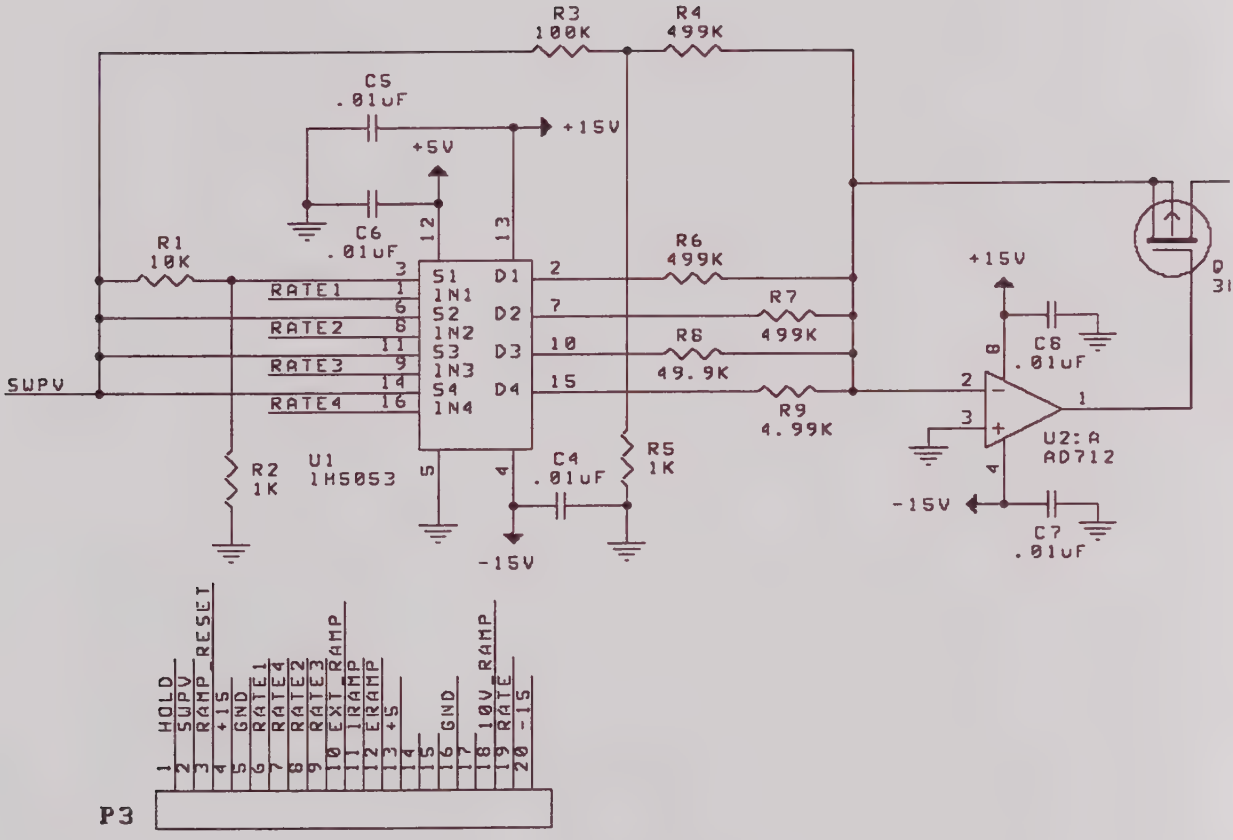

**Analog Sweep #1 (A8)**
**ASSY# 120BA09211 Rev A**
**Sheet 5 of 5**
**7-A8-5**




**ANALOG SWEEP #2 -- PC ASSY A8A1**

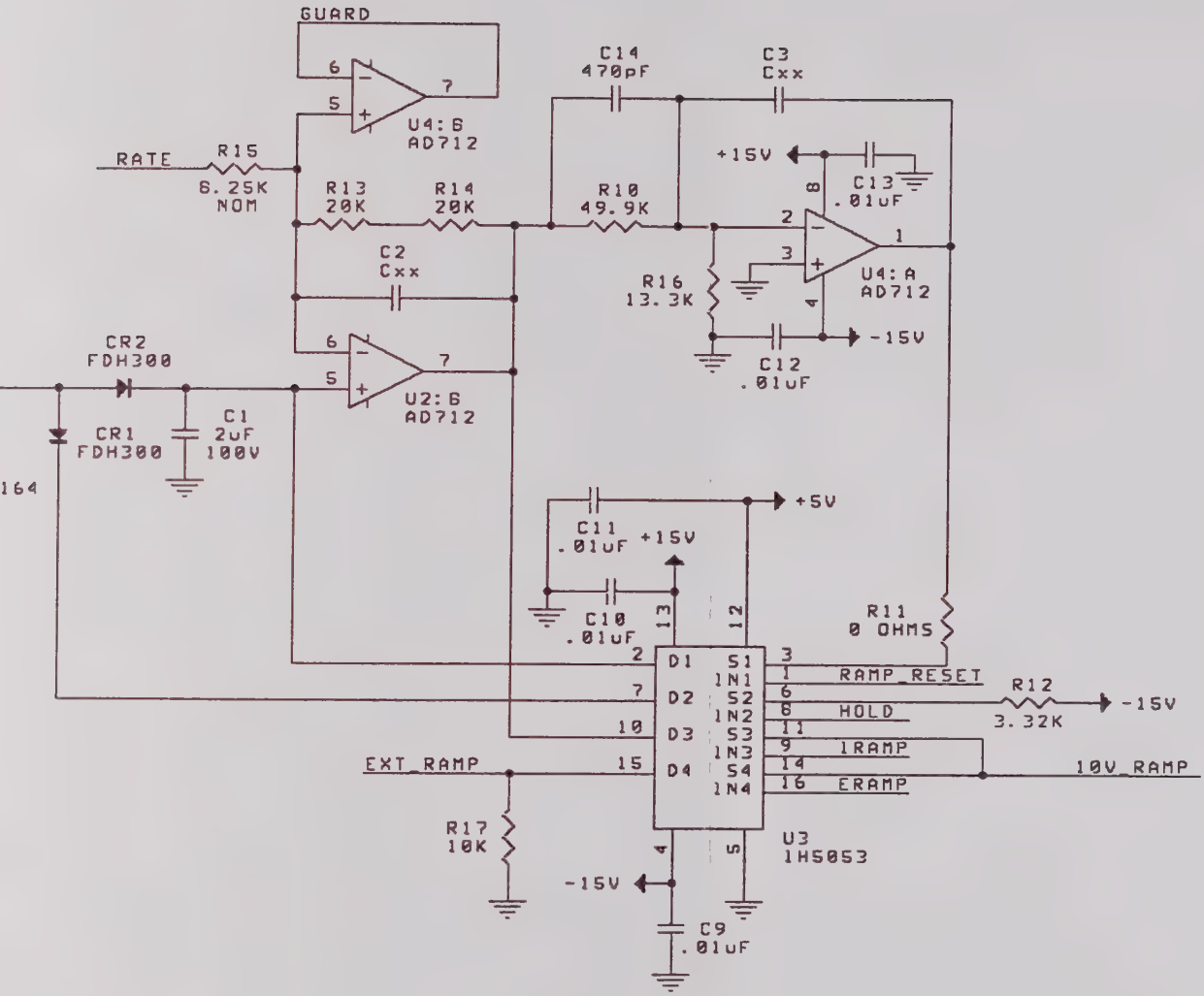
The main function of this board is to generate the various sweep rates.

A DC voltage SWPV is received from the A8 board whose magnitude varies according to the sweep rate selected. U1 switches resistors in parallel with R3 and R4 which gives decade changes in the rate by switching the current flow generated by the current source U2 A and Q1. The rates are controlled by the rate at which the cap C1 charges. The charging cap results in a ramp at U2-7 which can be fine tuned by the RATE voltage summed into U2 6. This 0-10V ramp or an external ramp can be selected by U3 as the 10V ramp output. U4 A is used for the purpose of resetting the rate ramp, when RAMP_RESET is selected at U3, by pulling U2-7 to 0V. When HOLD is selected CR1's cathode is pulled low, sinking current from the current source and biasing CR2 such that the voltage on C1 is held constant. This allows the ramp voltage to be held during band crossovers.

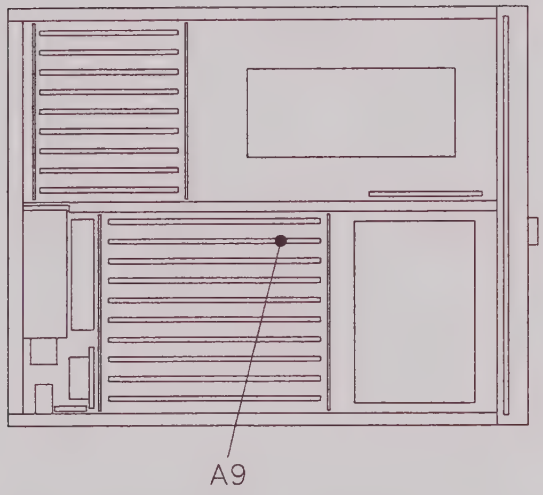



NOTES: UNLESS OTHERWISE SPECIFIED

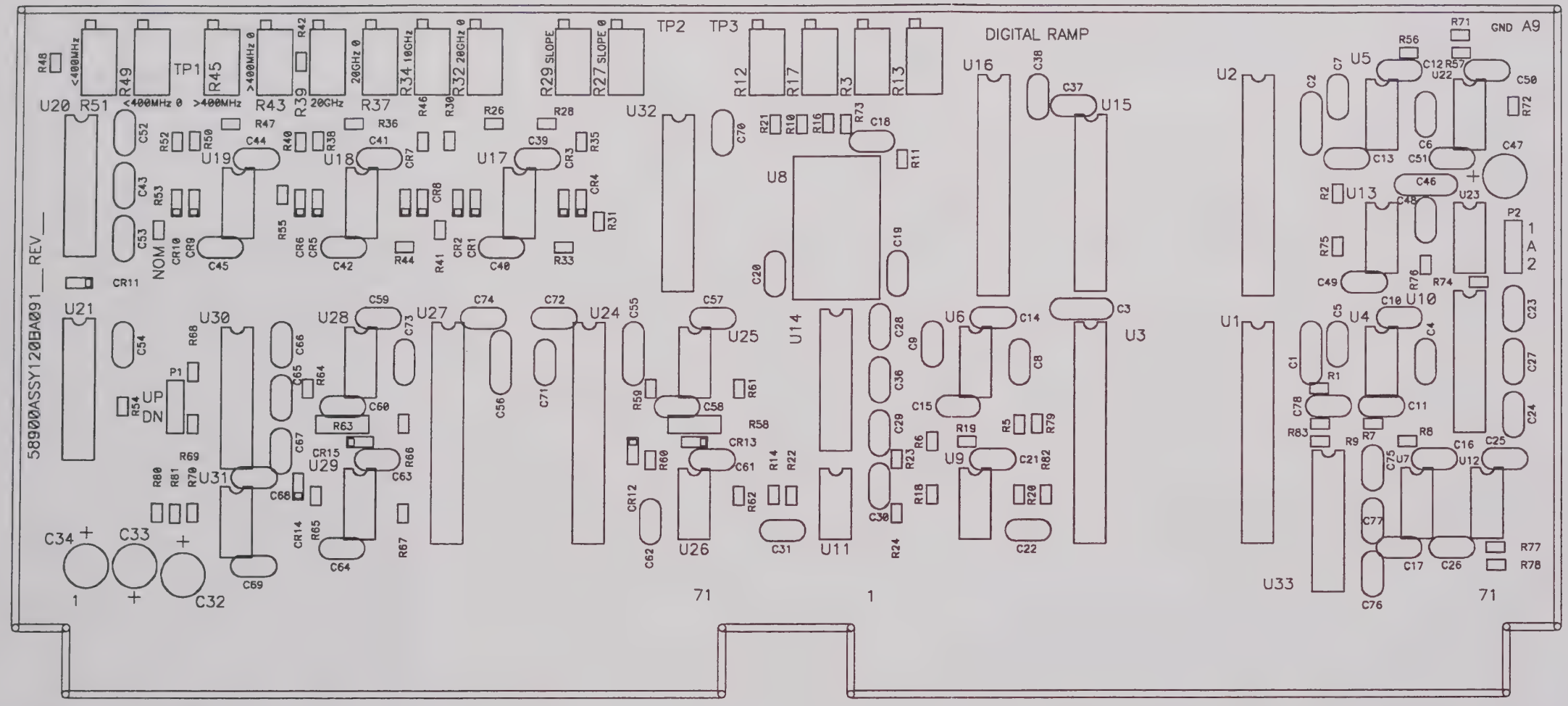
1) CAPACITOR VALUES ARE IN uF
2) RESISTOR VALUES ARE IN OHMS
3) RESISTORS ARE 1/4W, 1%




**Analog Sweep #2 (A8A1)**
**ASSY# 120BA11401 Rev A**
**Sheet 2 of 2**
**7-A8-7**




**Digital Ramp (A9)**
**ASSY# 120BA09100 Rev G**
**Sheet 1 of 4**
**7-A9-1**




**DIGITAL RAMP PCA -- PC ASSY A9**

The Digital Ramp PCA circuitry includes circuitry which generates voltage ramps required for both analog and digital sweep modes. It also provides level correction and frequency correction data required during analog sweep.

The DAC U1 section generates a 0 to 10V digital frequency ramp available at the output of U4 B. U10 B is used to switch either this digital frequency ramp or a 10 Volt ramp from the analog sweep board which is supplied to U12 B which provides the ramp output voltage to the front panel. The output of U10 B switch is also provided to U22 B which inverts the ramp. The frequency ramp or the negative frequency ramp is selected by U33 B depending on the direction of the sweep. The ramp selected is the input to the B section of DAC U1 which multiplies the ramp by some factor resulting in a ramp output at U4 A which is proportional to the delta or width of the sweep. DAC U2 section A provides a DC output voltage at U5 B which is proportional to the start frequency of the sweep. This start frequency voltage and the voltage ramp are summed together at U7 A resulting in a -.5 Volt per GHz ramp. This signal and an inverted form of the same signal (U7-7) are used by the level correction circuitry. The .5 V/GHz signal is also buffered by U12 A for output to the Rear Panel.

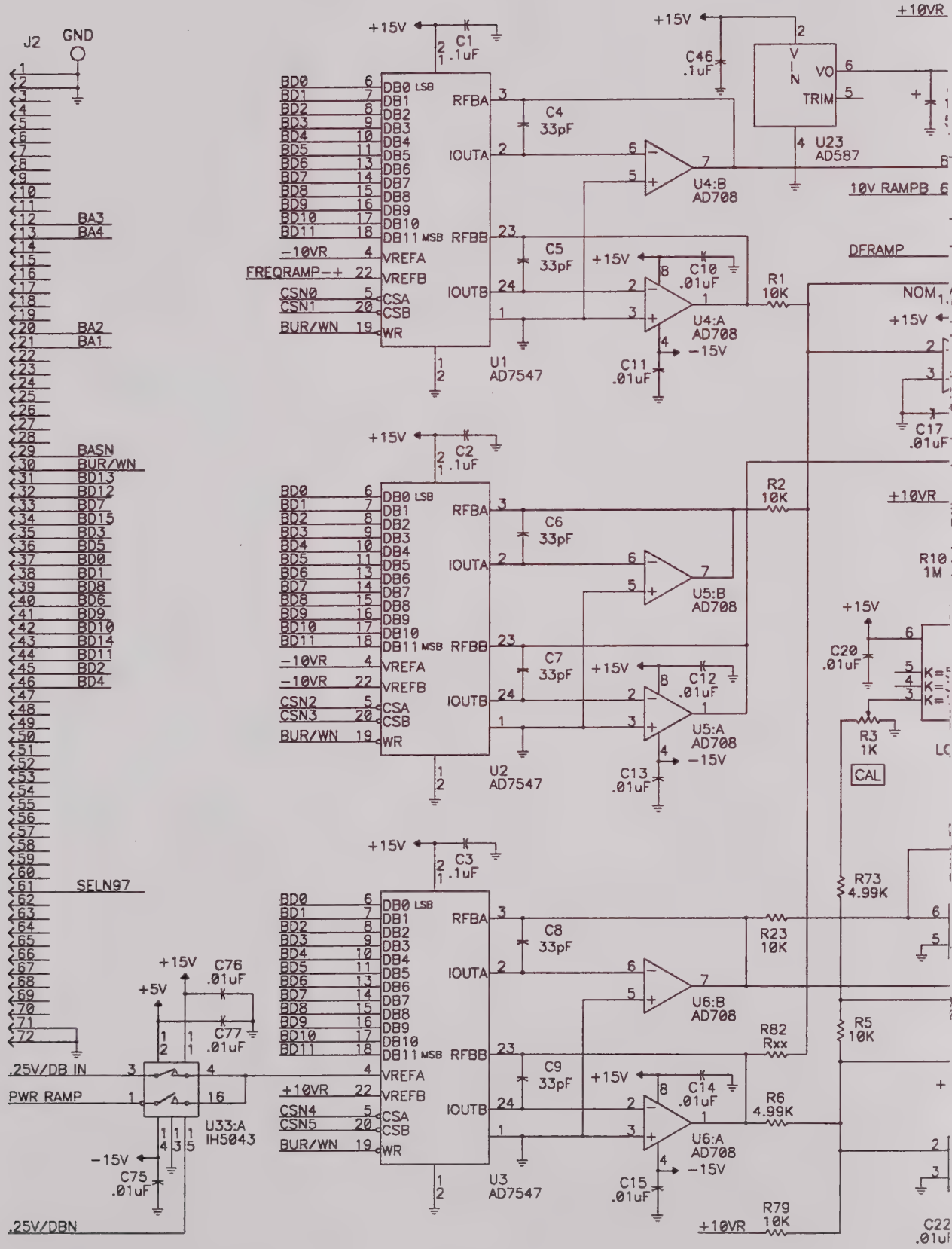
Section B of U2 generates a 0 to 10 Volt digital power ramp available at U5-1. This ramp or a 10 Volt ramp from the analog sweep board is selected by U10 A to be buffered by U13 A for optional Power Ramp to the rear panel, and to be fed back to U33 A. U33 A is used to switch the power ramp or a .5V/DB input (optional) from the rear panel, to the input of DAC U3 section A which multiplies the ramp by some factor resulting in a ramp output at U6-7 which is proportional to the delta or width of the power sweep. This delta power ramp or its inverse (U11 B) is selected by switch U14 A. It is inverted again at U9 B and summed at U9 A with a voltage proportional to the start power. This voltage is generated by DAC U3 and U6 A, resulting in a signal out at U9-1 which is .1V/ DB an optional rear panel output. The delta power ramp amplitude can also be calibrated by R3 before it is anti-logged by U8. U8 output is shifted and offset appropriately (R13 and R12) so that at the output of U11 A the delta power ramp is linear in dB. Either this signal or the straight delta power ramp (calibrated at R17) is selected at U14 B providing a power sweep voltage, linear in voltage or in dB, to the level control board.

The level correction circuitry requires the +.5V/GHz and - .5V/GHz ramp inputs as well as a + and - 10V reference. U17 B and U18 A along with their corresponding pots allow the ramp signal to be modified by 2 different slopes. The pots R32 and R37 allow the different slopes (controlled by R34 and R39) to start at different places corresponding to different frequencies. The resulting modified ramp is selected by U20 A to be used for frequencies greater than 2 GHz. There are two slope adjustments, U18 B and U19 A and corresponding pots, which can be selected to be used at frequencies less than 2GHz. To these slopes, specific to > or < 2GHz frequency bands, is added an additional universal slope, created by U17 A and its pots R27 and R29. This addition takes place at U19 B where yet another input may be selected by U20 B. This input is the amplitude marker input, which when enabled, pulses the instrument's output level at a frequency set by the marker. The final level correction voltage is available at U19-7 and is summed into the level board A10.

U13 B input is the marker signal which is amplified by U13 B to provide an optional rear panel output MKR_GATE which is provided for the purpose of gating an external counter.

U23 provides a +10 volt reference which is also inverted by U22 A giving a -10 volt reference as well. U32 and U15 provide the necessary buffering for interfacing with the computer bus. U16 decodes chip select lines.

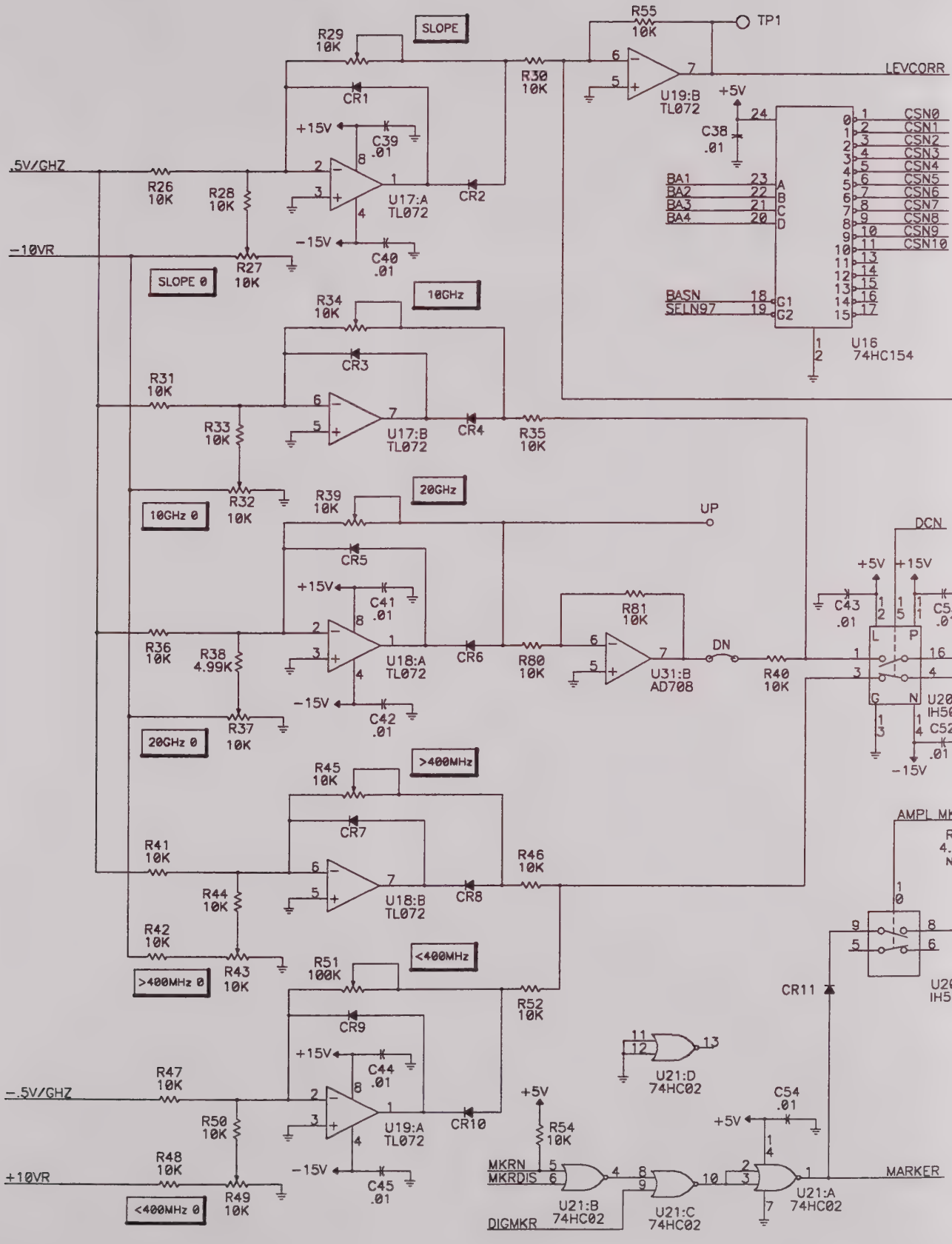
U24 and U27 digitally generate a similar slope correction as is created by the level correction circuitry. U24 DAC section A provides a DC offset voltage at U25-1 which controls what frequency (or voltage) the slope (in this case generated by -.5V/GHz ramp) summed into U26 A, begins having an effect. The steepness of this slope is then adjusted by the DAC when the signal is fed back into section B. The result is an output at U25-7 which has some specific slope starting at some specific frequency. This slope or its inverse is selected (U30 A) and summed together with another similar slope signal (generated by U27, U28 and U29). The result is a frequency correction signal at U31-1, which is summed with the YIG ramp on the A8 board, to keep the frequency correct during analog sweep.

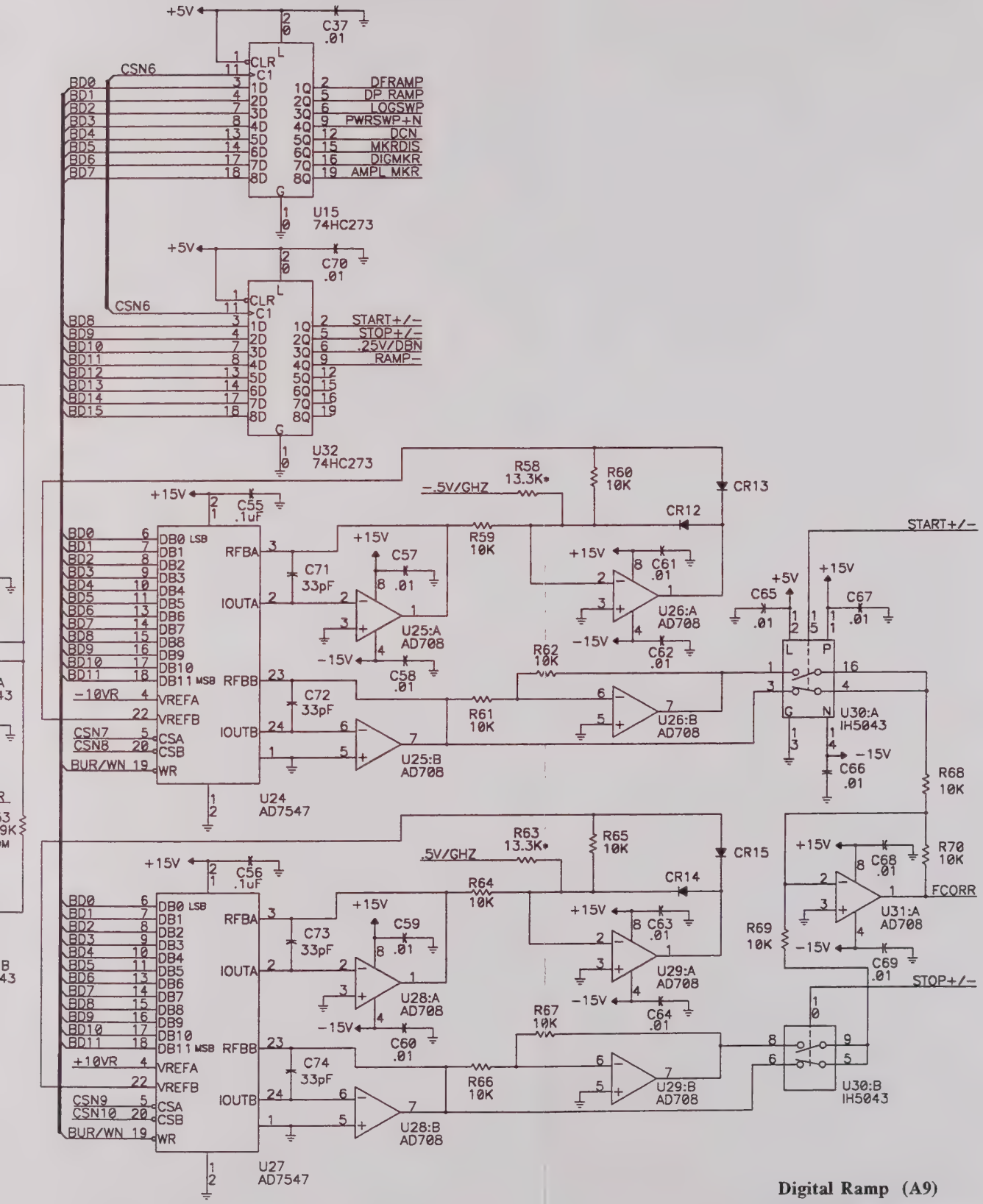

J2
GND
BA3
BA4
BA2
BA1
BASN
BUR/WN
BD13
BD12
BD7
BD15
BD3
BD5
BD0
BD1
BD8
BD6
BD9
BD10
BD14
BD11
BD2
BD4
SELN97
+15V
C1
.1uF
C2
C3
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
BD8
BD9
BD10
BD11
DB0 LSB
DB11 MSB
RFBA
IOUTA
RFBB
IOUTB
−10VR
FREQRAMP−+
CSN0
CSN1
CSN2
CSN3
CSN4
CSN5
CSA
CSB
WR
VREFA
VREFB
+10VR
U1
AD7547
U2
AD7547
U3
AD7547
C4
33pF
C5
33pF
C6
33pF
C7
33pF
C8
33pF
C9
33pF
U4:B
AD708
U4:A
AD708
U5:B
AD708
U5:A
AD708
U6:B
AD708
U6:A
AD708
C10
.01uF
C11
.01uF
C12
.01uF
C13
.01uF
C14
.01uF
C15
.01uF
−15V
C46
.1uF
U23
AD587
VIN
VO
TRIM
10V RAMPB
DFRAMP
NOM
C17
.01uF
R1
10K
R2
10K
R23
10K
R82
Rxx
R6
4.99K
R73
4.99K
R5
10K
R79
10K
R10
1M
C20
.01uF
R3
1K
CAL
C76
.01uF
C77
.01uF
+5V
.25V/DB IN
PWR RAMP
U33:A
IH5043
C75
.01uF
.25V/DBN
C22
.01uF

NOTES: UNLESS OTHERWISE SPECIFIED

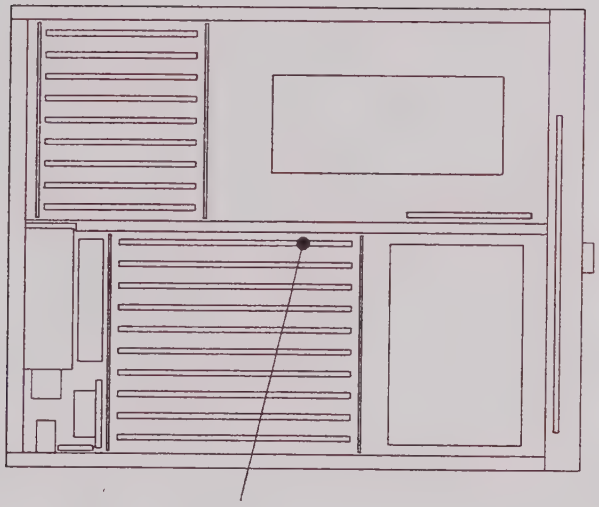
1. CAPACITOR VALUES ARE IN uF
2. RESISTOR VALUES ARE IN OHMS
3. RESISTORS ARE 1/5W, 1%
4. * INDICATES 1/4W, 1% RESISTORS
5. DIODES ARE 1N4148

**Digital Ramp (A9)**
**ASSY# 120BA09100 Rev G**
**Sheet 3 of 4**
**7-A9-3**

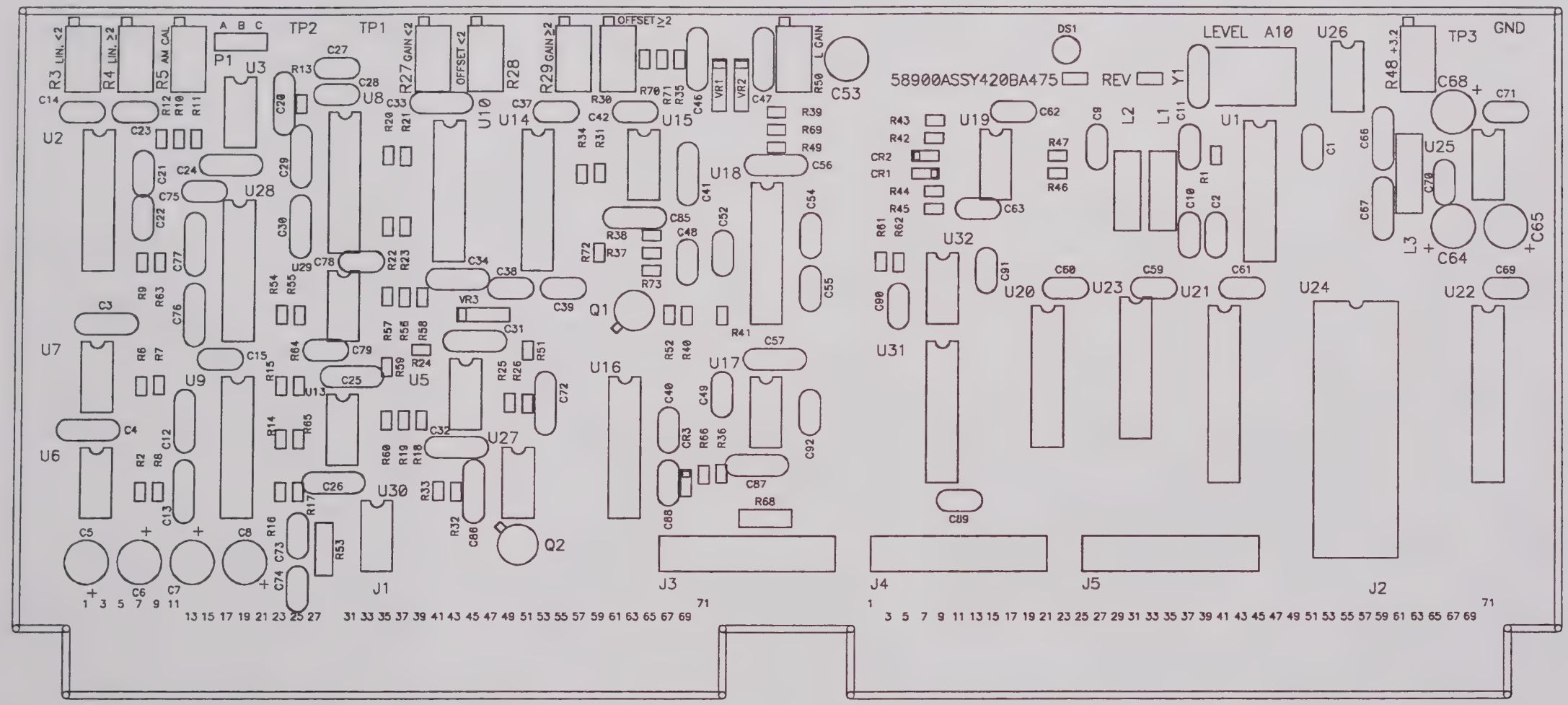

SLOPE
R29 10K
CR1
R30 10K
R55 10K
TP1
LEVCORR
U19:B TL072
+5V
C38 .01
.5V/GHZ
R26 10K
R28 10K
+15V
C39 .01
U17:A TL072
CR2
-15V
C40 .01
-10VR
R27 10K
SLOPE 0
10GHz
R34 10K
CR3
R31 10K
R33 10K
U17:B TL072
CR4
R35 10K
R32 10K
10GHz 0
20GHz
R39 10K
UP
CR5
C41 .01
R36 10K
R38 4.99K
U18:A TL072
CR6
R80 10K
R81 10K
U31:B AD708
DN
R40 10K
20GHz 0
R37 10K
DCN
C43 .01
>400MHz
R45 10K
CR7
R41 10K
R44 10K
U18:B TL072
CR8
R46 10K
R42 10K
>400MHz 0
R43 10K
<400MHz
R51 100K
R52 10K
CR9
CR11
U21:D 74HC02
-.5V/GHZ
R47 10K
C44 .01
R50 10K
U19:A TL072
CR10
R54 10K
C54 .01
+10VR
R48 10K
C45 .01
R49 10K
<400MHz 0
MKRN
MKRDIS
DIGMKR
U21:B 74HC02
U21:C 74HC02
U21:A 74HC02
MARKER
BA1
BA2
BA3
BA4
BASN
SELN97
CSN0
CSN1
CSN2
CSN3
CSN4
CSN5
CSN6
CSN7
CSN8
CSN9
CSN10
U16 74HC154




**Digital Ramp (A9)**
**ASSY# 120BA09100 Rev G**
**Sheet 4 of 4**
**7-A9-4**




**Level (A10)**
**ASSY# 420BA47500 Rev A**
**Sheet 1 of 5**
**7-A10-1**




**LEVEL – PC ASSY A10**

The leveling scheme used in the 7000 series can be compared to a Phase Locked Loop. The similarities are that the leveling loop has a reference and a variable input which are compared, and the loop action adjusts the variable input (which is proportional to the actual unit output level) until the two inputs are balanced. The comparison is made at the summing junction of an op amp integrator; the output of the integrator is used to control PIN leveling diodes which adjust the RF power level. This power level is detected and amplified as required and is returned as the variable input to the integrator.

On this board U17 A is the op amp integrator whose summing junction at pin 2 is comparing a reference input and the detected RF input. The reference input is the REFX20 input from the detector buffer module A200 which is amplified by U15. The gain is adjustable via pots R27 (GAIN ≤2 for downconverter frequencies) and R29 (GAIN >2 for frequencies >2GHz) and is switched by U14 A and B depending on the instrument's output frequency. The variable input to the U17 summing junction is the actual RF detector voltage which has been amplified at the detector buffer module A200. Q2 samples this signal (DETX20) when the unit is pulse modulated. When the unit is not pulse modulated, Q2 is turned on and the detector voltage, buffered by U30, can be inverted by U27, depending on whether the detector voltage is negative or positive. This inversion is controlled by switch U16 A and B. In addition to these two inputs to the summing junction of U17, offset voltages are summed in as well. Two different adjustable offsets (R28 and R30) are available and are switched by U14 A and B depending on whether the output frequency is > or ≤2 GHz. Q1 samples the signals at this summing point when in pulse modulation mode or, if pulse is turned off, Q1 is turned on all of the time. The summing integrator U17 A has variable feedback paths available. U18 A & B are switched in as appropriate for different leveling modes. The output of the amplifier is fed to U19 via CR1 and CR2; this serves as a window detector to detect when the leveling loop is unleveled. When the loop is unleveled U19-7 goes low, lighting DS1 and sending a low logic signal to the computer. The output of the U17 A amplifier is also amplified by U17 B, whose gain is adjustable via the R50 (LGAIN) pot. The output of U17 B is the level voltage which goes to the level driver board (A10A1) which ultimately drives the PIN leveling diodes.

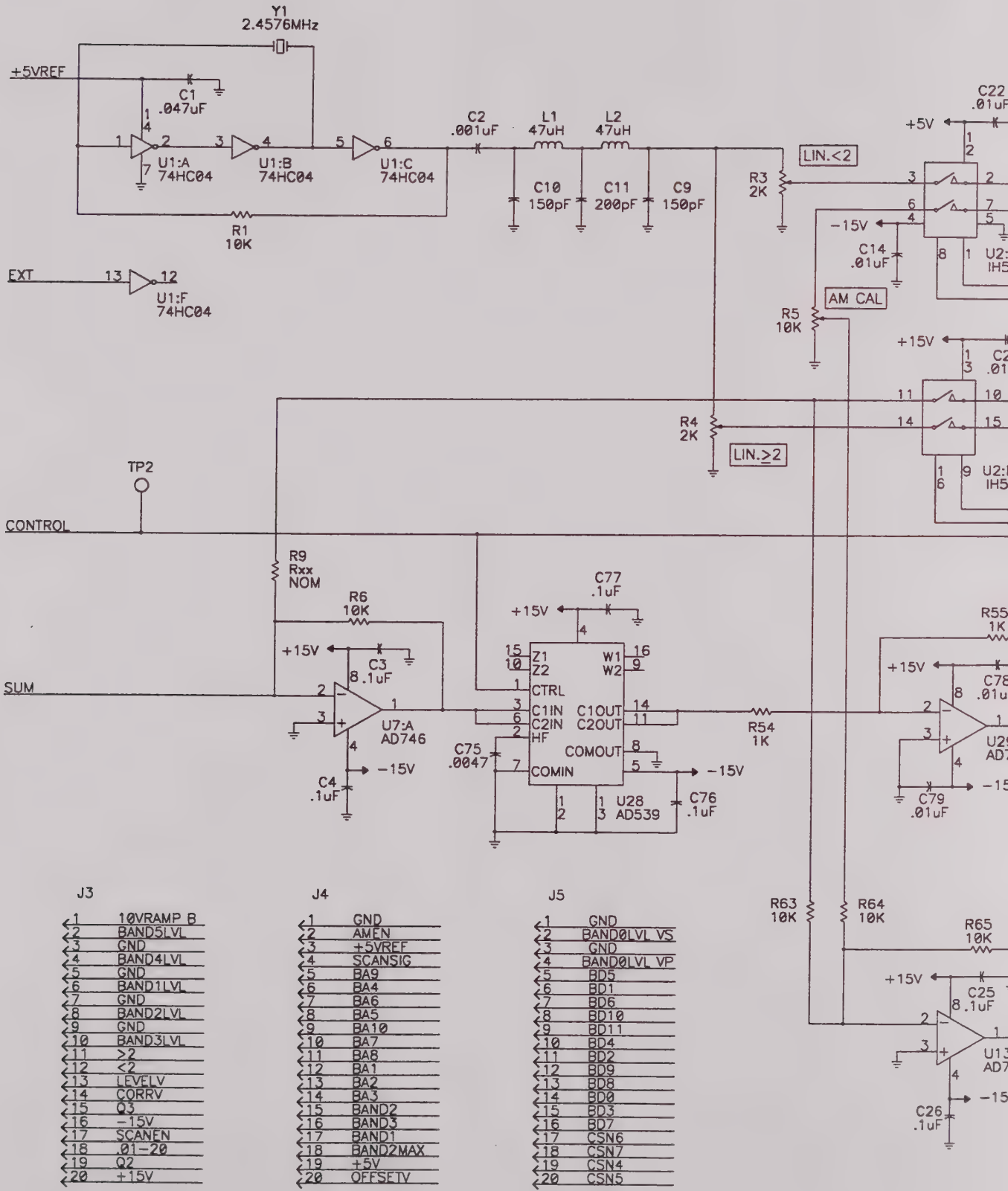
The reference signal is generated on this board. The 2.4596 MHz oscillator is composed of U1 A, B, C and Y1; its square wave output is then turned into a sine wave via filter L1, L2, C10, C11 and C9. The R3 and R4 pots allow a variable amplitude of this signal to be tapped off and amplified. U2 A and B switch in the appropriate pot depending on whether the frequency selected is > or ≤ 2 GHz. The signal is amplified and fed to a modulator U8 (which functions as a variable attenuator and is controlled by a voltage which may be a composite of different signals). The output of the modulator is sent via U10 to the Detector Buffer module to be amplified and returned to the leveling board as REFX20.

The main control voltage for the modulator IC's (U8, U28 and U9) is generated by the DAC U24. This voltage changes as the power level changes and is used to control the gain of U28. U28 adjusts the level correction voltage which is switched in by U16 A and amplified by U7 A. The amplitude of this signal is adjusted by the modulator U28 according to the power level the instrument is set to. U29 A amplifies the modulator output and sums it with the standard main control voltage at U29 B. The output of U29 B is inverted at U13 B and is used to control the modulator U9 which adjusts the amplitude of the AM signal when enabled by U2 A. R5 calibrates the AM signal which is then translated into a differential signal by U6 B and U7 B and applied to the modulator U9 input. The outputs of U9 are summed together by U6 A and this AM signal's amplitude has been adjusted according to the control voltage. The result is that the AM signal level is correctly calibrated for any power level. This AM signal is then summed together with its control voltage at U5 A and inverted at U5 B forming a composite signal used for appropriately modulating the reference signal at U8. VR3 and R51 are set to limit the control voltage so that it does not over drive the modulator.

U31 is a DAC programmed by the computer to give an output voltage at U32 B. This voltage is the appropriate offset required for the PIN leveling diode drivers on the A10A1 level driver board.

The U26 Reference provides a 5 volt reference which is filtered by L3 and C66 and C67. This filtered 5 volt reference is also amplified by U32 A to give a 10 volt reference. The 5 volt reference is also divided down by pot R48 to give a 3.2 v reference.

U20 provides decoding for the chip select lines. U21, U22 and U23 provide the necessary buffers for the bus interface lines.




J3

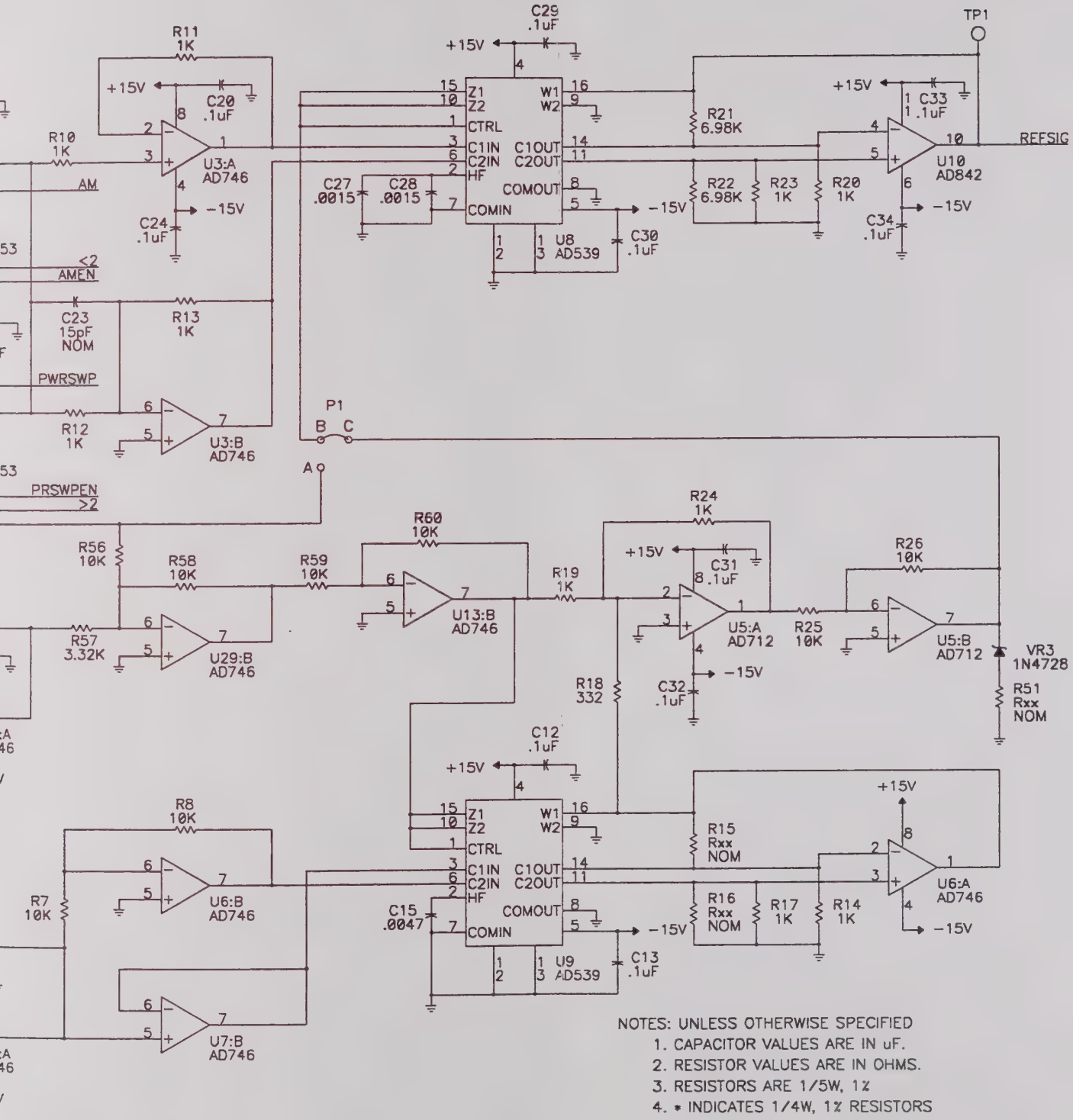
| | |
|---|---|
| 1 | 10VRAMP B |
| 2 | BAND5LVL |
| 3 | GND |
| 4 | BAND4LVL |
| 5 | GND |
| 6 | BAND1LVL |
| 7 | GND |
| 8 | BAND2LVL |
| 9 | GND |
| 10 | BAND3LVL |
| 11 | >2 |
| 12 | <2 |
| 13 | LEVELV |
| 14 | CORRV |
| 15 | Q3 |
| 16 | -15V |
| 17 | SCANEN |
| 18 | .01-20 |
| 19 | Q2 |
| 20 | +15V |

J4

| | |
|---|---|
| 1 | GND |
| 2 | AMEN |
| 3 | +5VREF |
| 4 | SCANSIG |
| 5 | BA9 |
| 6 | BA4 |
| 7 | BA6 |
| 8 | BA5 |
| 9 | BA10 |
| 10 | BA7 |
| 11 | BA8 |
| 12 | BA1 |
| 13 | BA2 |
| 14 | BA3 |
| 15 | BAND2 |
| 16 | BAND3 |
| 17 | BAND1 |
| 18 | BAND2MAX |
| 19 | +5V |
| 20 | OFFSETV |

J5

| | |
|---|---|
| 1 | GND |
| 2 | BAND0LVL VS |
| 3 | GND |
| 4 | BAND0LVL VP |
| 5 | BD5 |
| 6 | BD1 |
| 7 | BD6 |
| 8 | BD10 |
| 9 | BD11 |
| 10 | BD4 |
| 11 | BD2 |
| 12 | BD9 |
| 13 | BD8 |
| 14 | BD0 |
| 15 | BD3 |
| 16 | BD7 |
| 17 | CSN6 |
| 18 | CSN7 |
| 19 | CSN4 |
| 20 | CSN5 |




NOTES: UNLESS OTHERWISE SPECIFIED

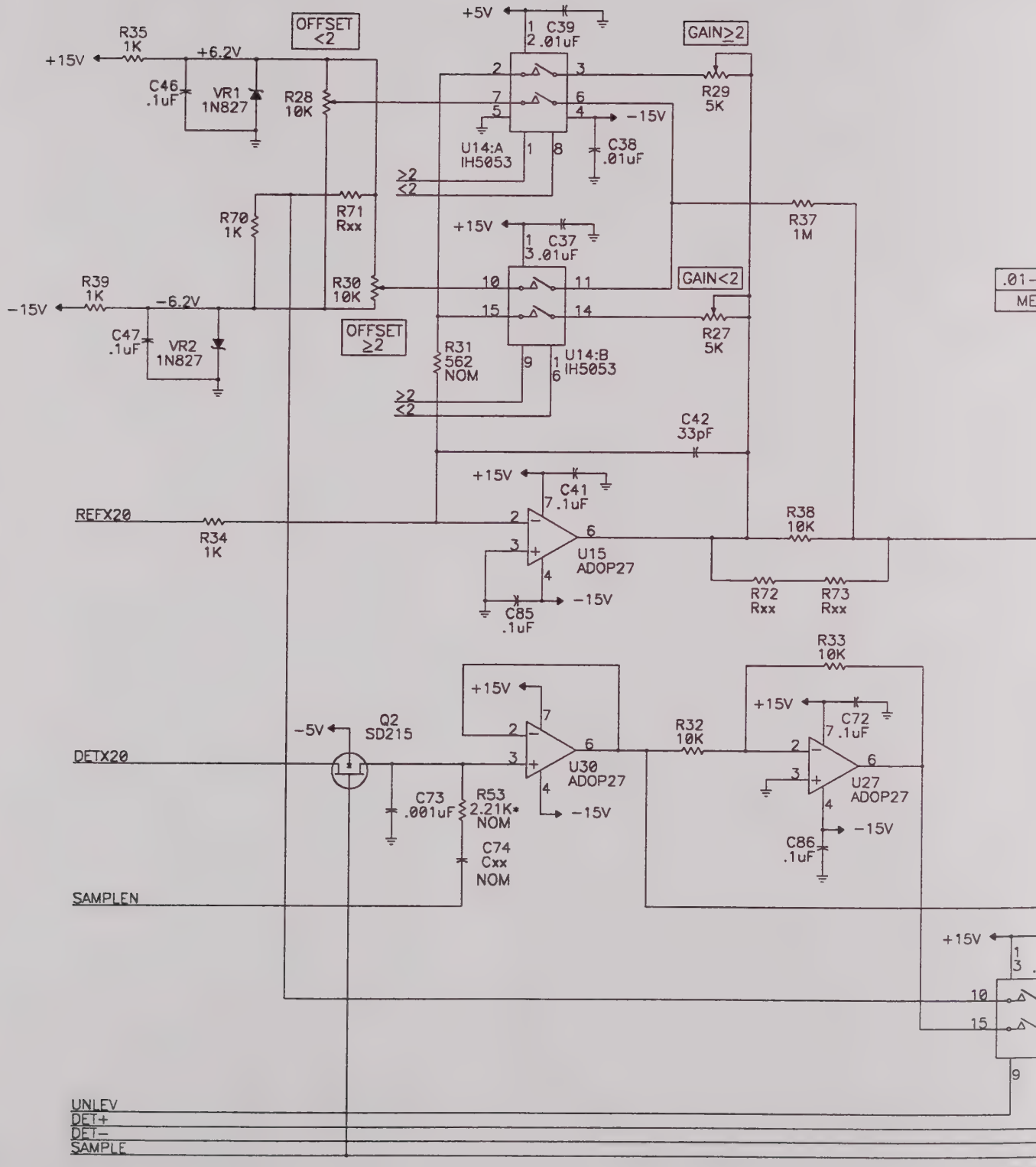
1. CAPACITOR VALUES ARE IN uF.
2. RESISTOR VALUES ARE IN OHMS.
3. RESISTORS ARE 1/5W, 1%
4. * INDICATES 1/4W, 1% RESISTORS

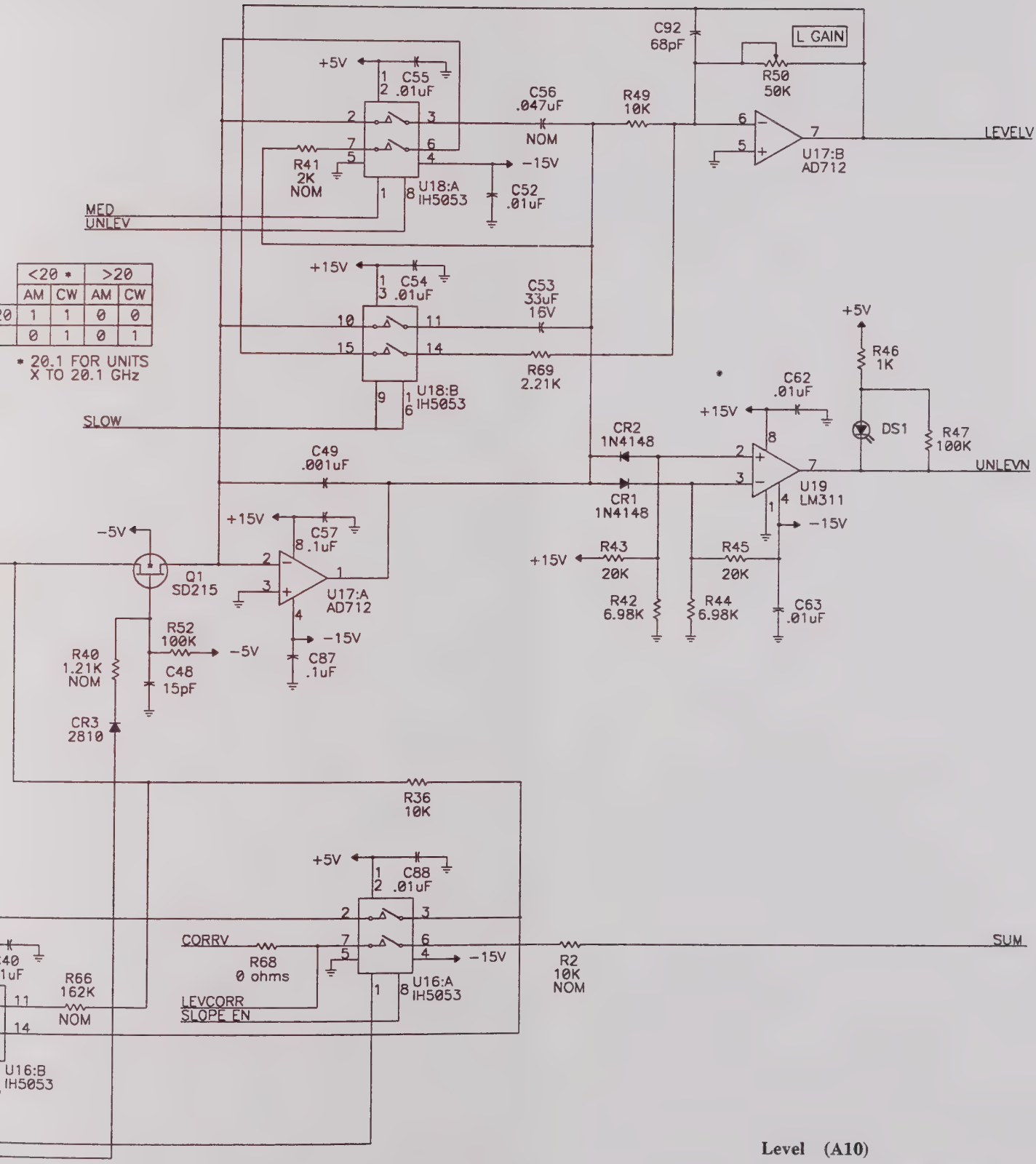
**Level (A10)**

**ASSY# 420BA47500 Rev A**

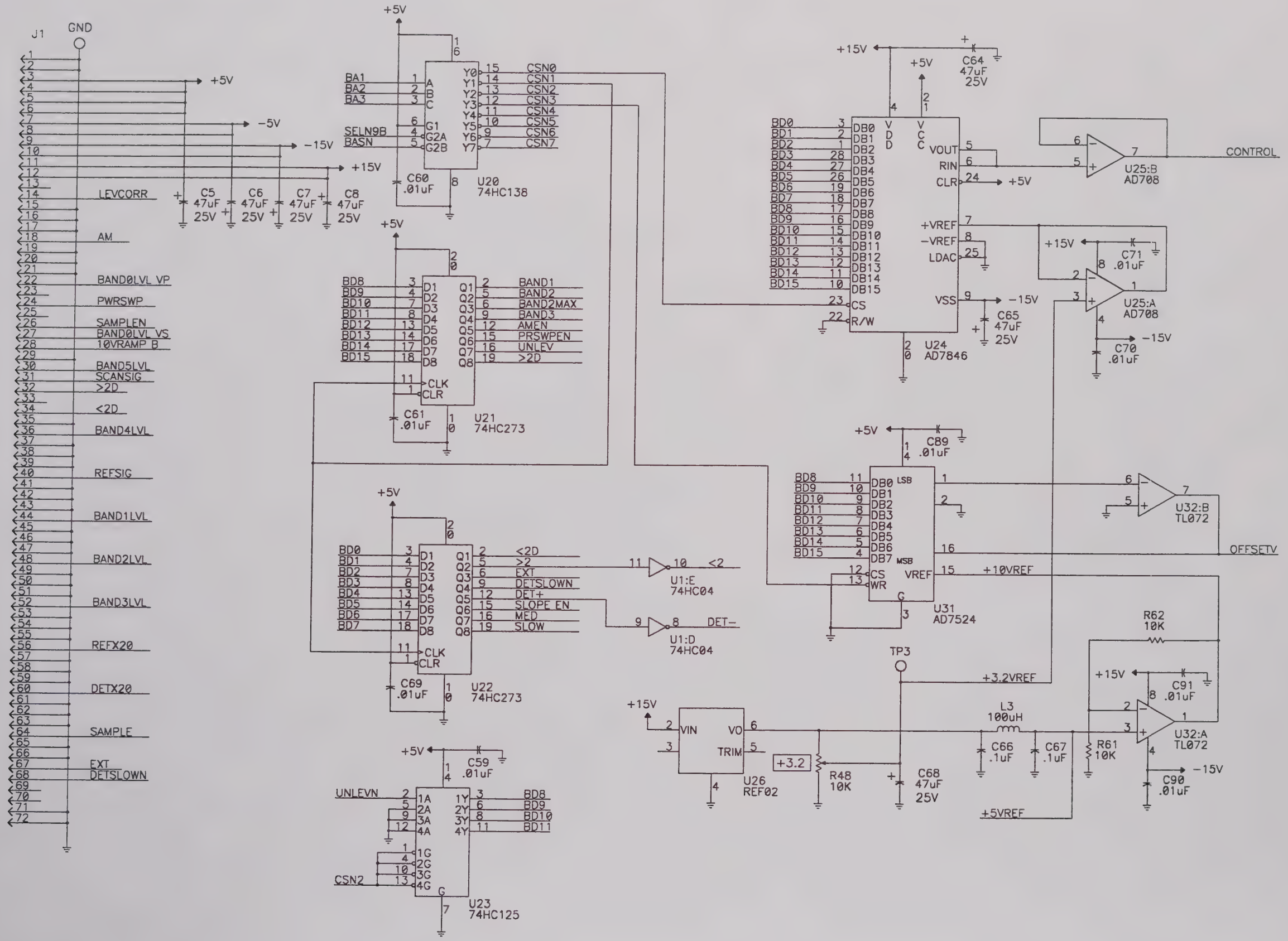
**Sheet 3 of 5**

**7-A10-3**

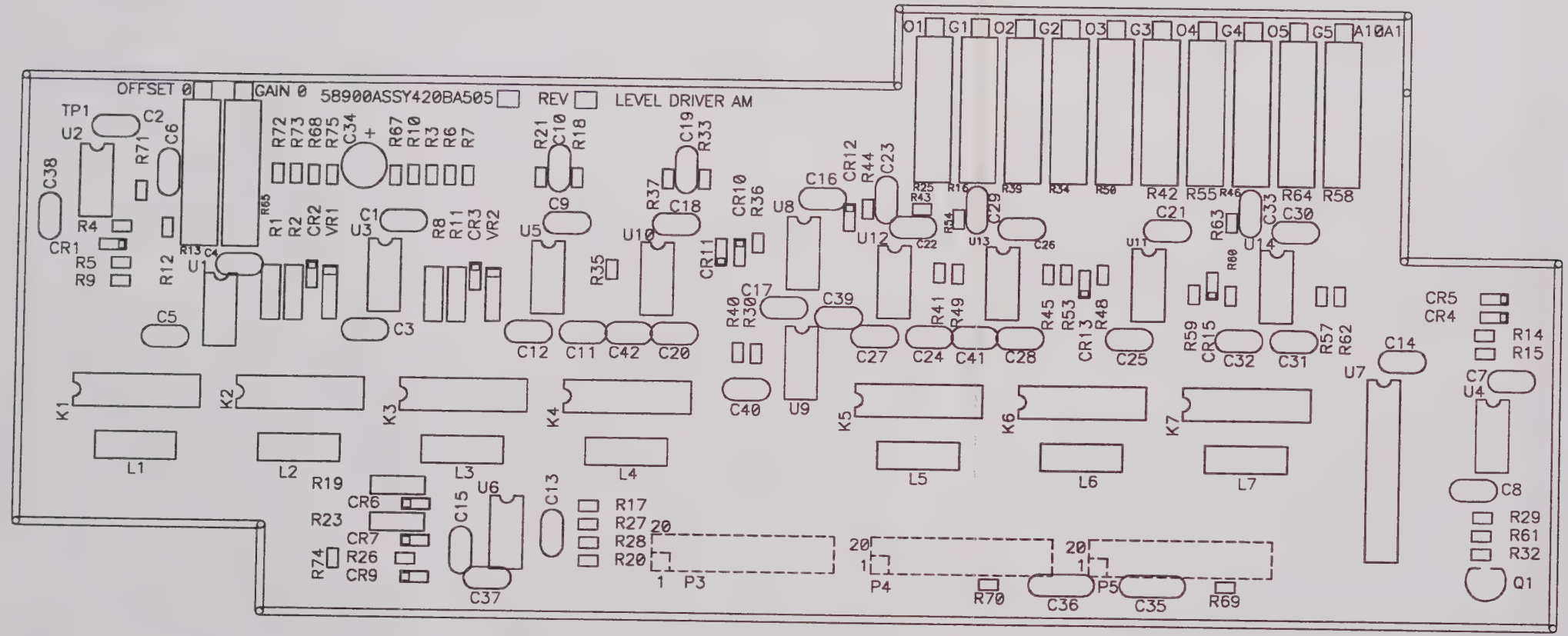

R35
1K
+15V
+6.2V
OFFSET
<2
C46
.1uF
VR1
1N827
R28
10K
+5V
1
C39
2.01uF
GAIN≥2
2
3
7
6
5
4
-15V
R29
5K
U14:A
IH5053
1
8
C38
.01uF
≥2
<2
R70
1K
R71
Rxx
+15V
1
C37
3.01uF
R37
1M
R39
1K
-15V
-6.2V
R30
10K
10
11
GAIN<2
15
14
R27
5K
C47
.1uF
VR2
1N827
OFFSET
≥2
R31
562
NOM
9
1
6
U14:B
IH5053
≥2
<2
C42
33pF
+15V
C41
7.1uF
REFX20
R34
1K
2
3
6
4
U15
ADOP27
R38
10K
-15V
C85
.1uF
R72
Rxx
R73
Rxx
R33
10K
+15V
-5V
Q2
SD215
7
2
3
6
4
U30
ADOP27
R32
10K
+15V
C72
7.1uF
2
3
6
4
U27
ADOP27
DETX20
C73
.001uF
R53
2.21K*
NOM
-15V
C74
Cxx
NOM
-15V
C86
.1uF
SAMPLEN
+15V
1
3
10
15
9
UNLEV
DET+
DET-
SAMPLE




**Level (A10)**
**ASSY# 420BA47500 Rev A**
**Sheet 4 of 5**
**7-A10-4**




**Level (A10)**
**ASSY# 420BA47500 Rev A**
**Sheet 5 of 5**
**7-A10-5**




**LEVEL DRIVER -- PC ASSY A10A1**

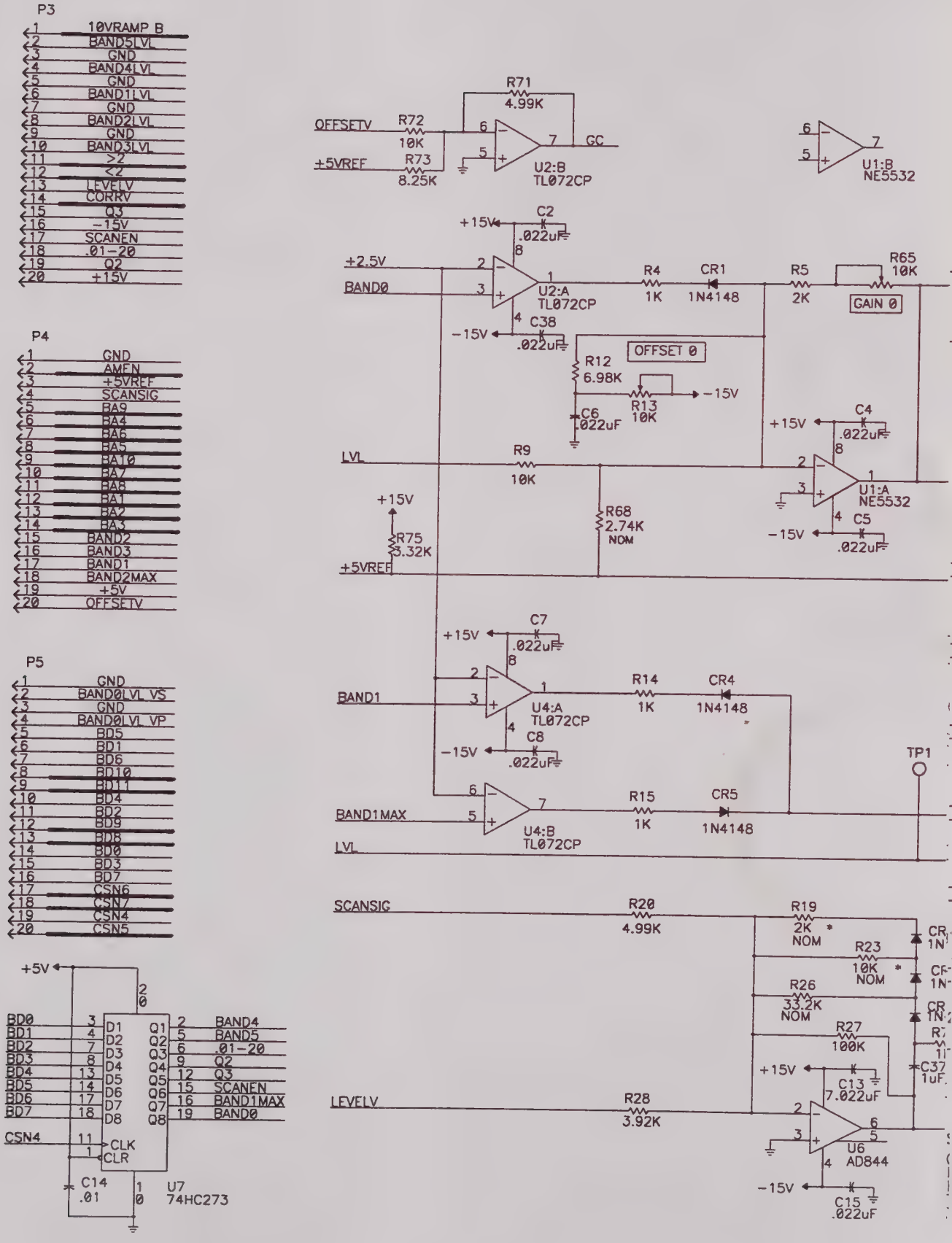
The level driver contains amplifiers and filters which drive the levelers (variable attenuator circuits) in the microwave module.

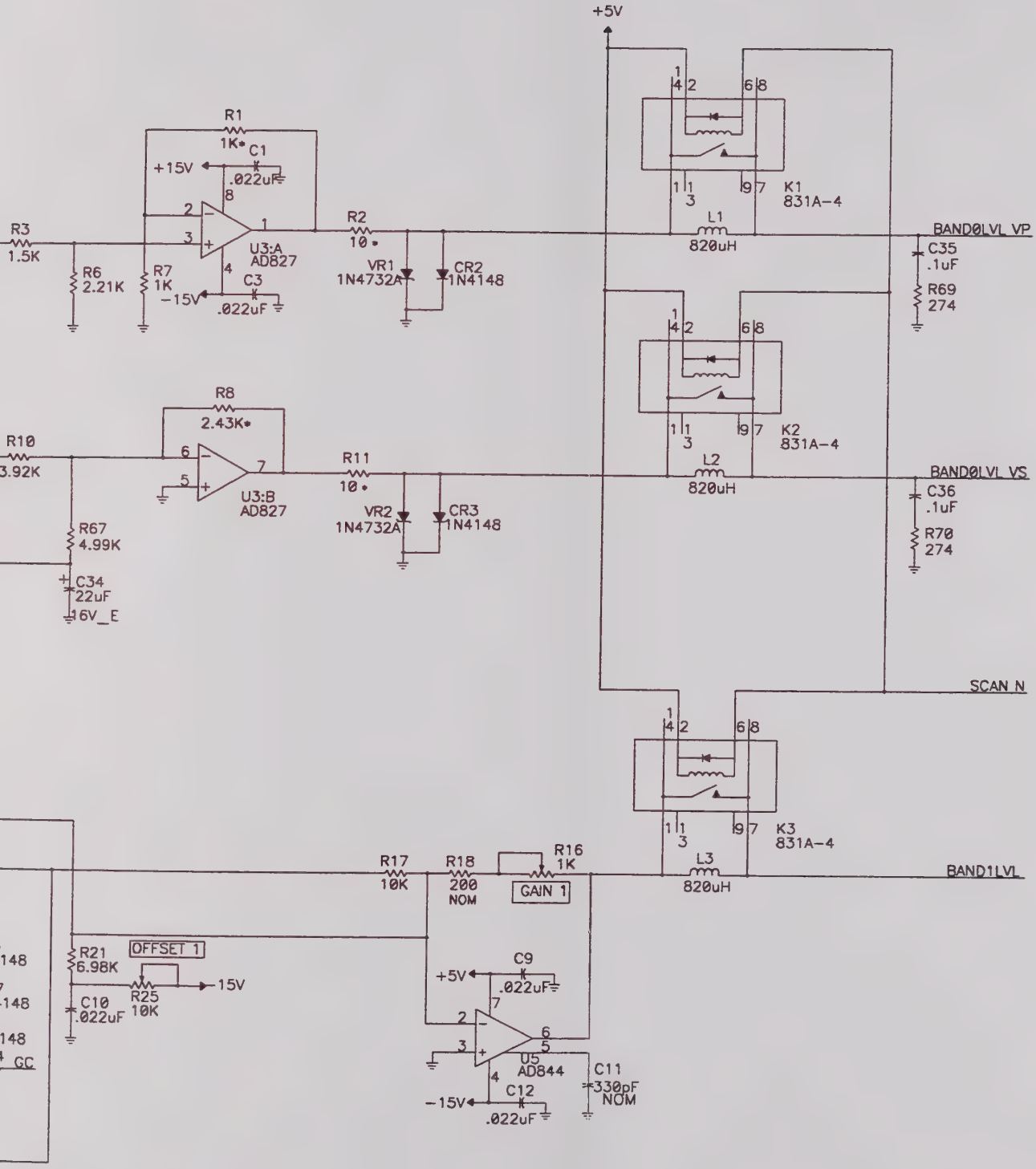
'LEVELV', the output of the Level PC board (A10), is amplified by the circuit which includes U6. This amplifier circuit has four different levels of AC gain, activated (in order of decreasing gain) as the AC input level increases and switches on the diodes CR9, CR7, and CR6. The 'SCANSIG' input is not used in this instrument. The amplifier output at U6-6 ('LVL') is supplied to the level drivers associated with particular bands.

Inside the microwave module, the leveler for Band 0 (the downconverted range, below 2 GHz) consists of a pair of FETs which act as variable attenuators; separate driver outputs are required to control the 'series' FET and the 'shunt' FET. For Band 0, therefore, the 'LVL' signal is converted by a differential amplifier (consisting of U1A, U3-A, and U3-B) into two outputs (the output labeled 'BAND0LVL VP' is applied to the series FET and the output labeled 'BAND0LVL VS' is applied to the shunt fet. Both outputs are transmitted through low-pass filter elements (see L1 and L2) to the microwave module; relays K1 and K2 are used to bypass these filters during AM operation (the control input labeled 'SCAN N' is actually on only during amplitude modulation, not scan modulation).

Higher frequency bands are level-controlled by PIN diode attenuator circuits in the microwave module, and these attenuators do not require differential control inputs. For Band 1 (2-8 GHz), the level driver is the circuit which includes U5. The filter associated with this band (see L3) is bypassed through relay K3 during AM operation. For Band 2 (8-20 GHz), the level driver is the circuit which includes U10. The filter associated with this band (see L4) is bypassed through relay K4 during AM operation.

The remaining level drivers are unused in this design.

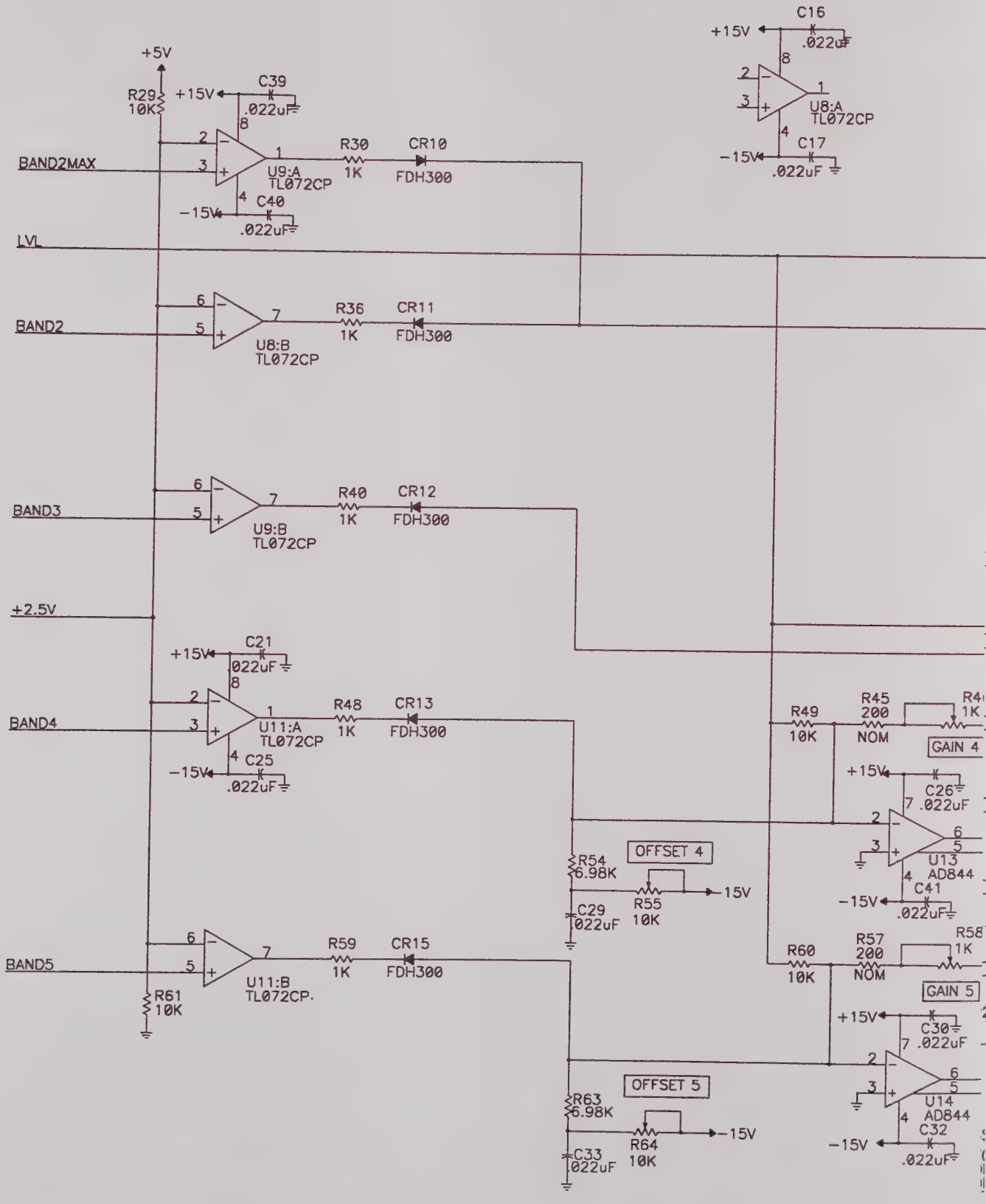

P3
1 10VRAMP B
2 BAND5LVL
3 GND
4 BAND4LVL
5 GND
6 BAND1LVL
7 GND
8 BAND2LVL
9 GND
10 BAND3LVL
11 >2
12 <2
13 LEVELV
14 CORRV
15 Q3
16 -15V
17 SCANEN
18 .01-20
19 Q2
20 +15V
P4
1 GND
2 AMEN
3 +5VREF
4 SCANSIG
5 BA9
6 BA4
7 BA6
8 BA5
9 BA10
10 BA7
11 BA8
12 BA1
13 BA2
14 BA3
15 BAND2
16 BAND3
17 BAND1
18 BAND2MAX
19 +5V
20 OFFSETV
P5
1 GND
2 BAND0LVL_VS
3 GND
4 BAND0LVL_VP
5 BD5
6 BD1
7 BD6
8 BD10
9 BD11
10 BD4
11 BD2
12 BD9
13 BD8
14 BD0
15 BD3
16 BD7
17 CSN6
18 CSN7
19 CSN4
20 CSN5
+5V
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
CSN4
D1
D2
D3
D4
D5
D6
D7
D8
CLK
CLR
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
BAND4
BAND5
.01-20
Q2
Q3
SCANEN
BAND1MAX
BAND0
C14
.01
U7
74HC273
OFFSETV
R72
10K
+5VREF
R73
8.25K
R71
4.99K
GC
U2:B
TL072CP
U1:B
NE5532
+15V
C2
.022uF
+2.5V
BAND0
U2:A
TL072CP
R4
1K
CR1
1N4148
R5
2K
R65
10K
GAIN 0
C38
.022uF
OFFSET 0
R12
6.98K
R13
10K
C6
.022uF
LVL
R9
10K
R68
2.74K
NOM
R75
3.32K
C4
.022uF
U1:A
NE5532
C5
.022uF
C7
.022uF
BAND1
U4:A
TL072CP
R14
1K
CR4
1N4148
C8
.022uF
TP1
BAND1MAX
U4:B
TL072CP
R15
1K
CR5
1N4148
SCANSIG
R20
4.99K
R19
2K
NOM
R23
10K
NOM
R26
33.2K
NOM
R27
100K
C13
7.022uF
C37
1uF
LEVELV
R28
3.92K
U6
AD844
C15
.022uF

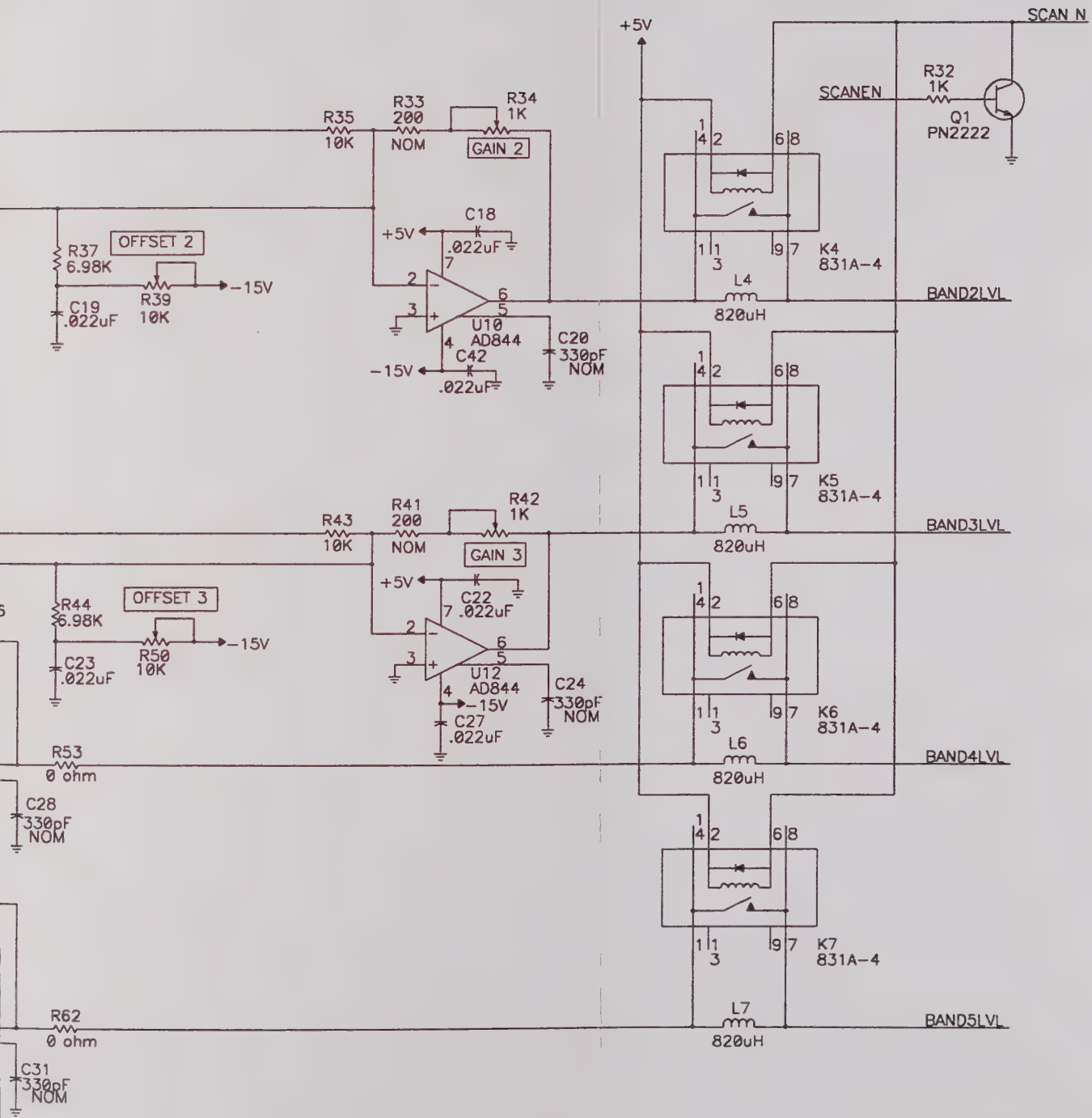



NOTES: UNLESS OTHERWISE SPECIFIED

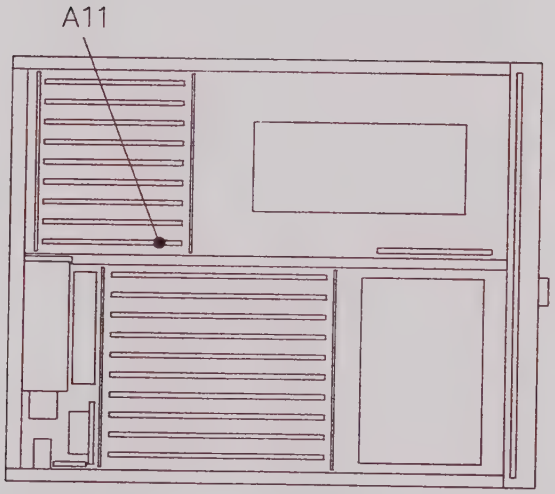
1. CAPACITOR VALUES ARE IN uF.
2. RESISTOR VALUES ARE IN OHMS.
3. * INDICATES 1/4W, 1% RESISTORS.

**Level Driver (A10A1)**
**ASSY# 420BA50500 Rev A**
**Sheet 2 of 3**
**7-A10-7**

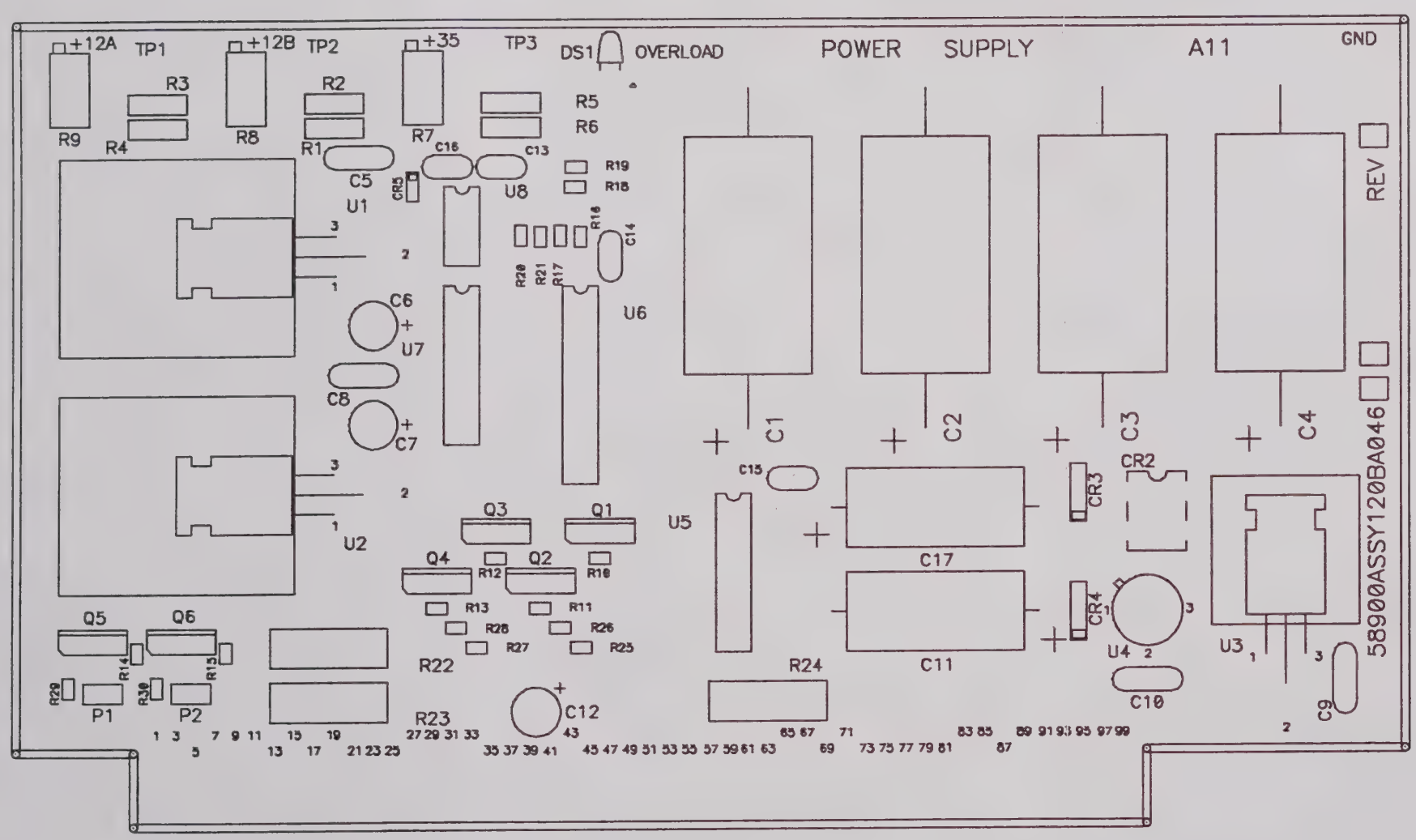

+5V
R29
10K
+15V
C39
.022uF
BAND2MAX
U9:A
TL072CP
R30
1K
CR10
FDH300
-15V
C40
.022uF
LVL
BAND2
U8:B
TL072CP
R36
1K
CR11
FDH300
BAND3
U9:B
TL072CP
R40
1K
CR12
FDH300
+2.5V
C21
022uF
BAND4
U11:A
TL072CP
R48
1K
CR13
FDH300
C25
.022uF
BAND5
U11:B
TL072CP.
R59
1K
CR15
FDH300
R61
10K
C16
.022uF
U8:A
TL072CP
C17
.022uF
R49
10K
R45
200
NOM
GAIN 4
C26
.022uF
U13
AD844
C41
.022uF
R54
6.98K
OFFSET 4
R55
10K
C29
022uF
15V
R60
10K
R57
200
NOM
GAIN 5
C30
.022uF
U14
AD844
C32
.022uF
OFFSET 5
R63
6.98K
R64
10K
C33
022uF
-15V




**Level Driver (A10A1)**
**ASSY# 420BA50500 Rev A**
**Sheet 3 of 3**
**7-A10-8**




**Power Supply (A11)**
**ASSY# 120BA04650 Rev A**
**Sheet 1 of 3**
**7-A11-1**



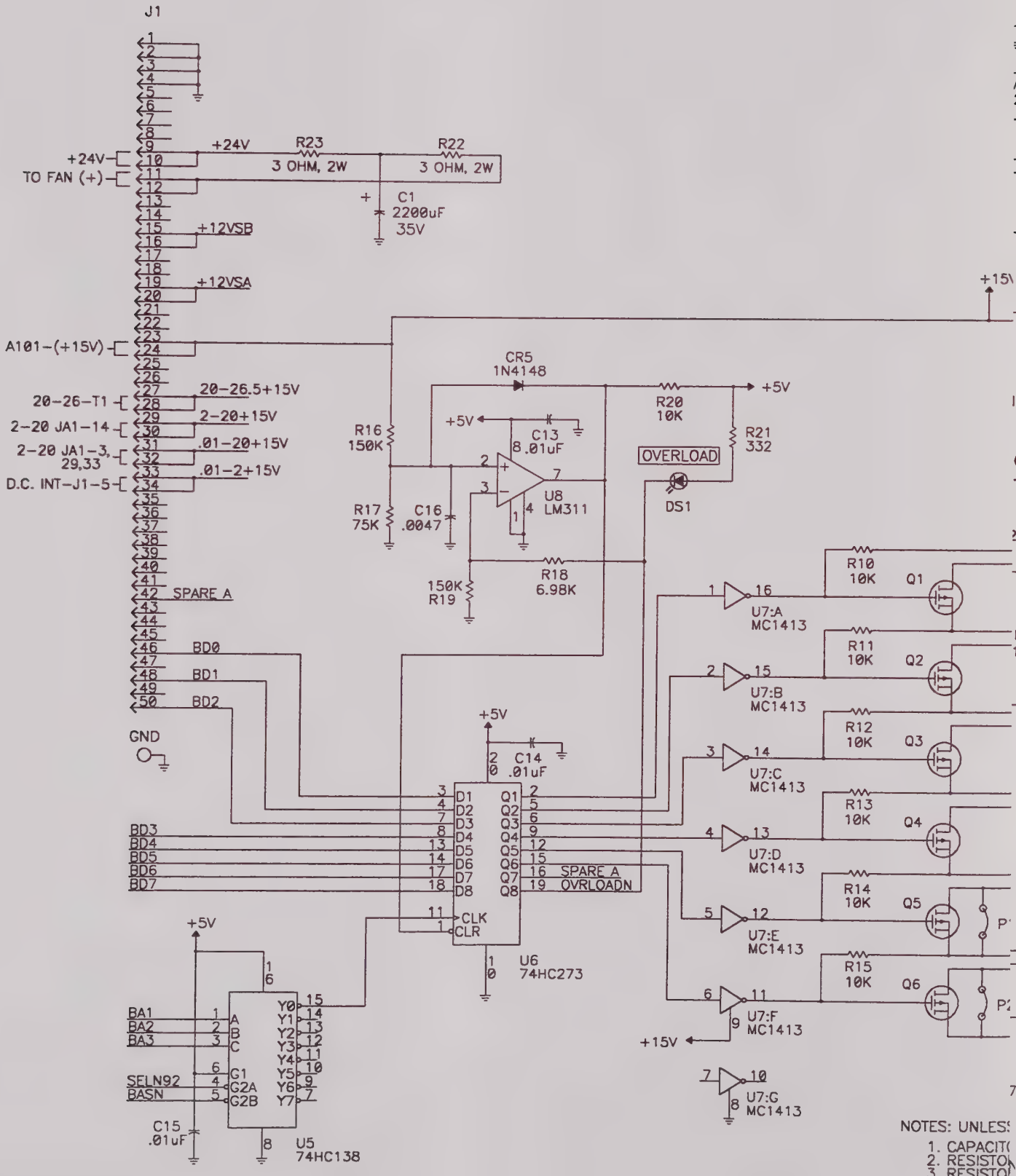

**POWER SUPPLY -- PC ASSY A11**

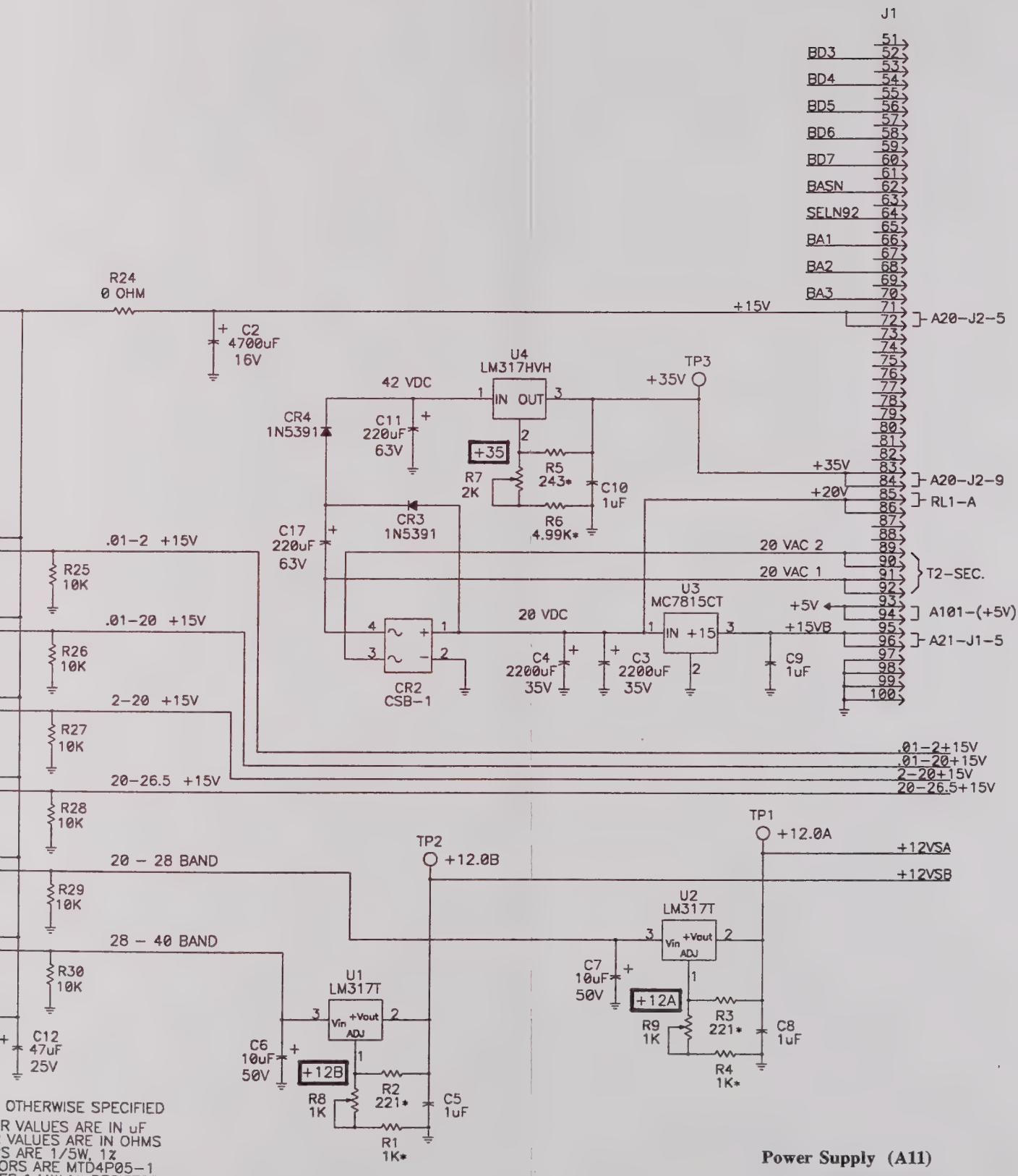
Most of the instrument's power supplies are furnished directly from the switching power supply assembly to the circuits that require them. However, some supplies require further conditioning, or are independent of the switching PS assembly, and for those supplies, the A11 Power Supply PC board provides such functions as rectification, regulation, filtering, and switching.

The circuit consisting of R22, R23, and C1 is used to filter the +24V supply in order to eliminate fan-generated noise.

The +15V input at J1-23 is furnished to the front panel display drivers, and also (through power FETs Q1 through Q6) to various band-related sections of the microwave module. In order to minimize power dissipation in this module, each FET is switched on only when the associated frequency band is in use. The FETs are switched by gates U7-A through U7-F, which are in turn switched by the computer by way of the latch (U6) and the latch strobe (U5). The supplies for the frequency doublers in the 20-28 band (Q5) and the 28-40 band (Q6) are re-regulated down to +12 V by U2 and U1. The +15V supply is also applied to an overload detection circuit (see U8), which is needed to protect the power FETs. If the '+15V' input falls below an acceptable voltage level, the latch is cleared, the FETs are turned off, and the 'OVERLOAD' LED is lit.

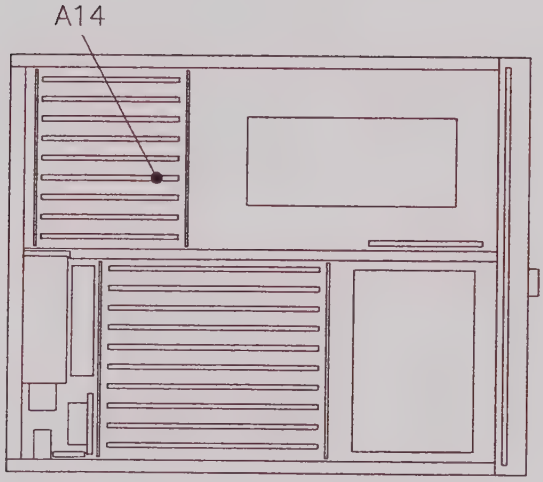
Standby power (including a heater voltage for the timebase oscillator's crystal oven) is supplied through a small transformer located near the cooling fan. The 20 VAC inputs from the transformer are rectified by CR2 and regulated by U3 to make a +15V heater voltage for the timebase. The rectified 20 VAC input is used to drive the line power relay, and is also doubled by CR3 and CR4, and regulated by U4, to make a +35 VDC output for the front panel fluorescent displays.


J1
+24V
TO FAN (+)
+24V
R23
3 OHM, 2W
R22
3 OHM, 2W
C1
2200uF
35V
+12VSB
+12VSA
A101-(+15V)
20-26-T1
20-26.5+15V
2-20 JA1-14
2-20+15V
2-20 JA1-3, 29,33
.01-20+15V
D.C. INT-J1-5
.01-2+15V
SPARE A
BD0
BD1
BD2
GND
CR5
1N4148
R16
150K
R17
75K
C16
.0047
C13
.01uF
U8
LM311
R20
10K
R21
332
OVERLOAD
DS1
R18
6.98K
150K
R19
C14
.01uF
U6
74HC273
D1
D2
D3
D4
D5
D6
D7
D8
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
CLK
CLR
SPARE A
OVRLOADN
BD3
BD4
BD5
BD6
BD7
BA1
BA2
BA3
SELN92
BASN
C15
.01uF
U5
74HC138
U7:A
MC1413
U7:B
MC1413
U7:C
MC1413
U7:D
MC1413
U7:E
MC1413
U7:F
MC1413
U7:G
MC1413
R10
10K
Q1
R11
10K
Q2
R12
10K
Q3
R13
10K
Q4
R14
10K
Q5
R15
10K
Q6
+15V
+5V
NOTES: UNLES
1. CAPACIT
2. RESISTO
3. RESISTO
4. TRANSIS
5. * INDICA

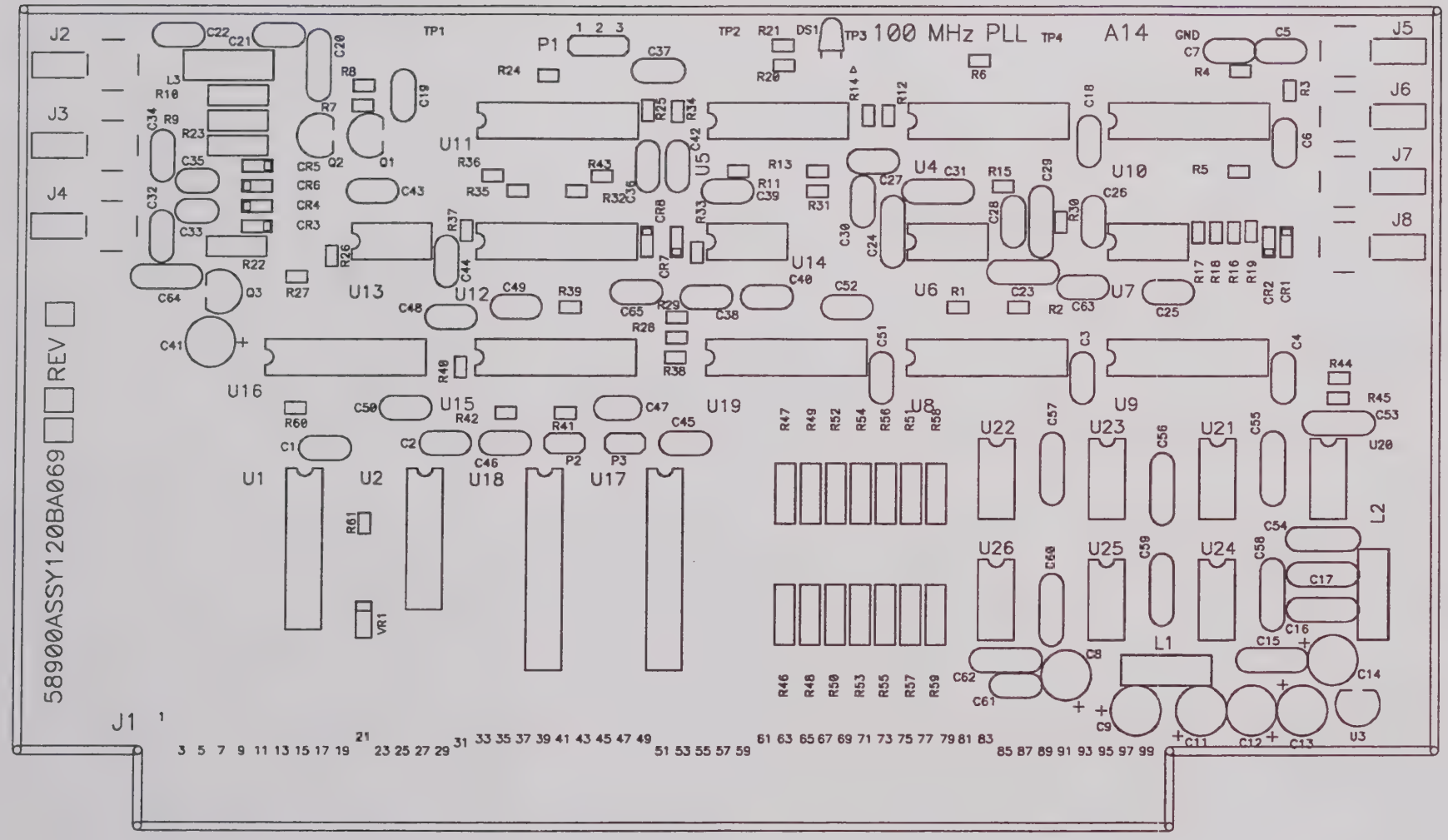



OTHERWISE SPECIFIED
R VALUES ARE IN uF
VALUES ARE IN OHMS
S ARE 1/5W, 1%
ORS ARE MTD4P05-1
ES 1/4W,1% RESISTORS

**Power Supply (A11)**
**ASSY# 120BA04650 Rev A**
**Sheet 3 of 3**
**7-A11-3**




**100 MHz Ref PLL (A14)**
**ASSY# 120BA06950 Rev A**
**Sheet 1 of 4**
**7-A14-1**



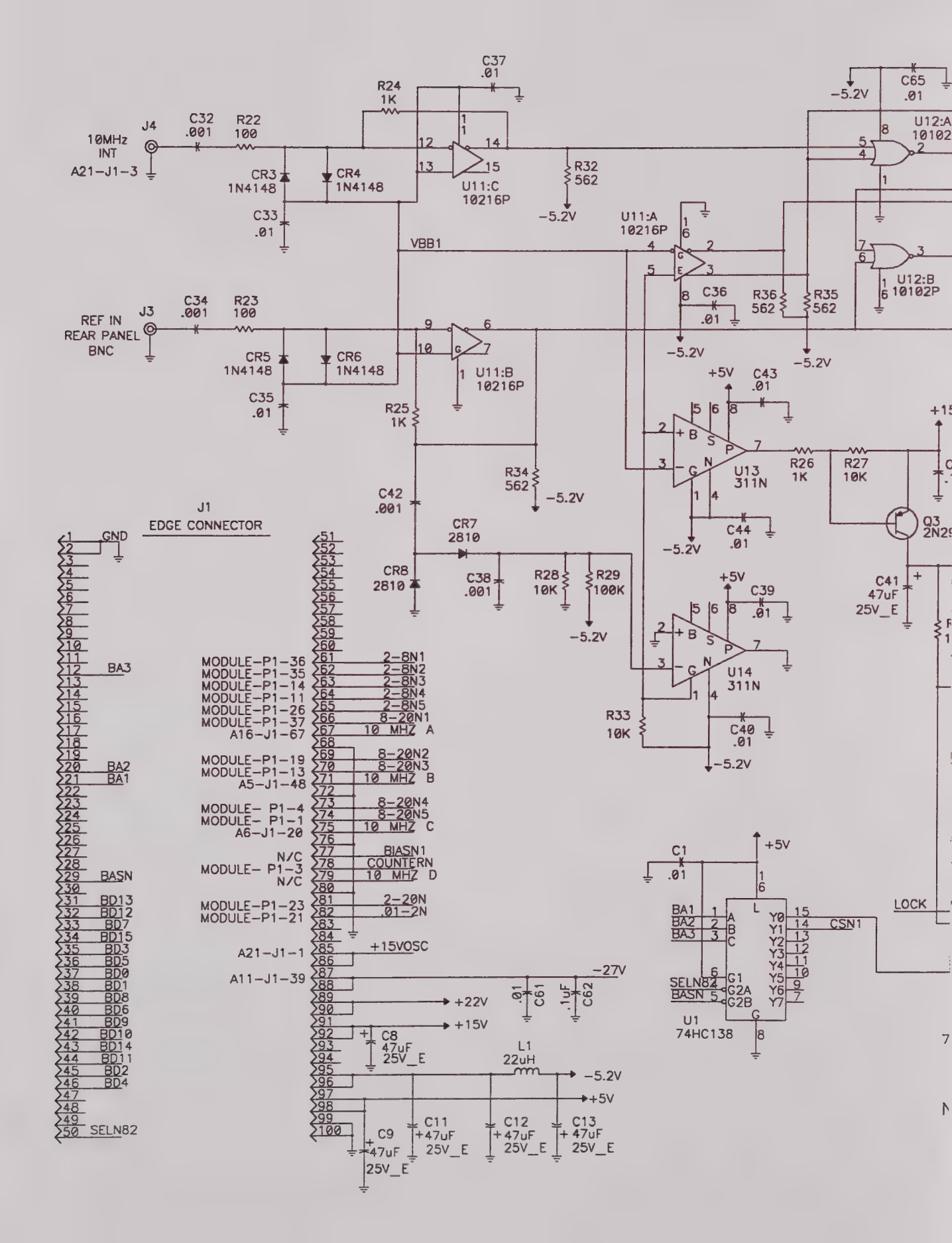

**100 MHZ REFERENCE PHASE LOCKED LOOP -- PC ASSY A14**

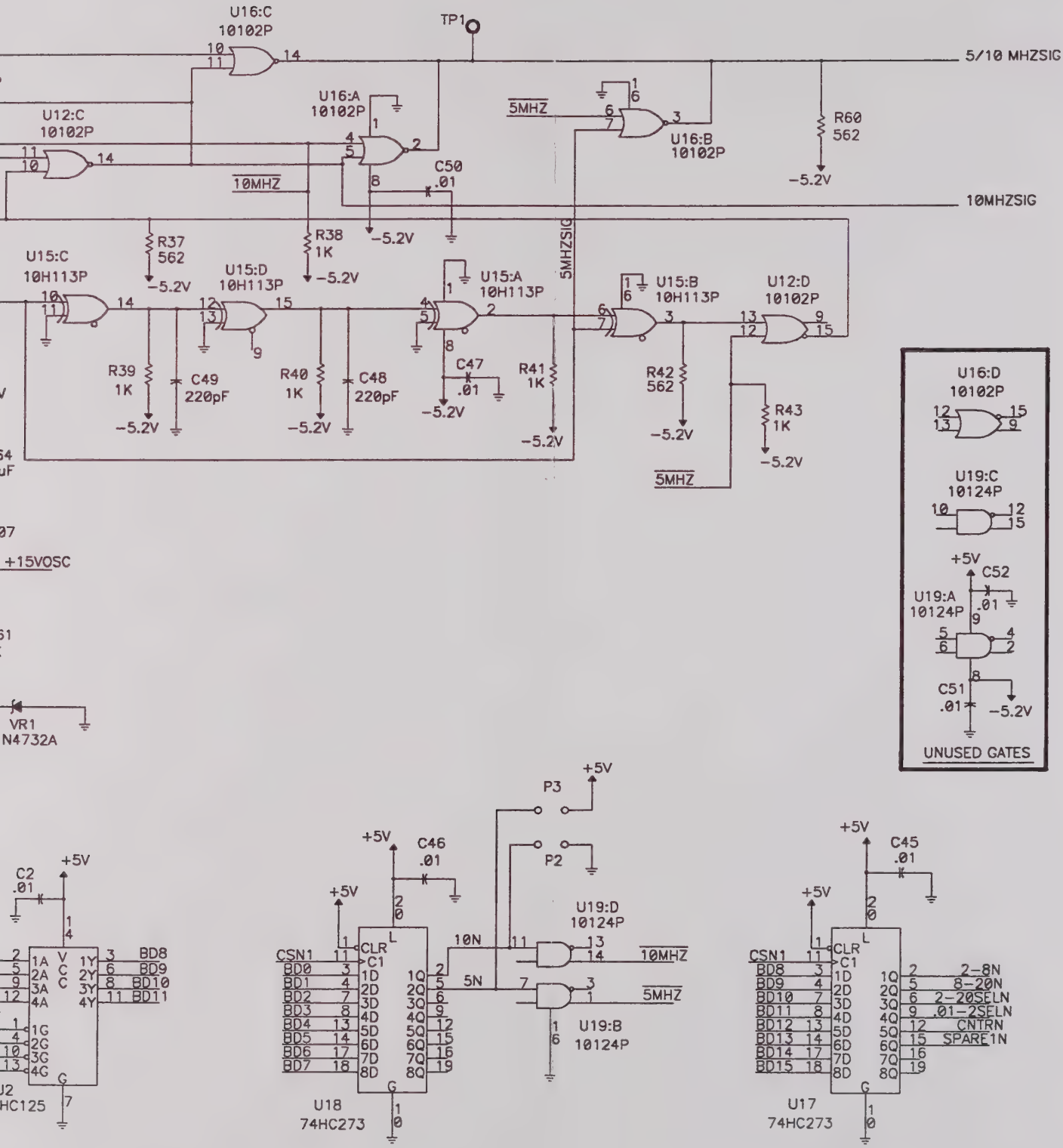
This circuit is used to phase lock the 100 MHz oscillator (A201) to the internal 10 MHz timebase or to an external timebase; in addition to the loop output it produces a lock indicator signal and a set of buffered 10 MHz outputs to be used for references for other loops in the instrument.

The 100 MHz input at J5 is buffered by U10 B before being divided down to 10 MHz by U4. This 10 MHz is then buffered by U8 A, B, C and U9 A, B and C so that it can be used by other circuits in the unit which require a 10 MHz reference. The signal is also applied to the variable input of the phase detector U5-9.

The reference input to the phase detector U5-6 comes from a switching circuit, which selects either an internal or external 10 MHz reference. When no external reference is present at J3 the internal 10 MHz reference at J4, buffered by U11 A, is allowed to propagate through U12 C and on to the phase detector (U5-6). When an external 10 MHz signal is present at J3 it is buffered by U11 A and allowed to propagate through U12 A to the phase detector. The presence of an external 10 MHz reference is detected when a charge is built up on C38 causing the switching circuit (comparator U14) to switch to a high state, in turn causing U13 output to go high which ultimately turns off the supply to the internal 10MHz reference. In addition, the switching circuit enables the external reference path at U12 A and disables the internal reference at U12 C. The selected reference is then available through Q1 and Q2 as the 10 MHz reference output on the rear panel.

The phase comparator U5 compares the 10MHz reference with the output of the divider U4 and determines which signal leads or lags the other. The output pulses at U5-12 and 3 are integrated or filtered by U6 B resulting in a tuning or correction voltage at J6 which will steer the 100 MHz VCXO oscillator in the proper direction (a more positive voltage increases frequency) to acquire and sustain a locked condition. When the loop is phase locked (the reference and variable input frequency and phase are equal) the output pulses of the phase detector will be extremely narrow at a 10 MHz rate. U7, CR1 and CR2 along with other components serve as a window detector which detects the tuning voltage and detects unlocked conditions. When the loop unlocks U7-7 goes low, lighting DS1 and sending the unlock logic level to the computer via U2, a tri-state buffer which serves as the interface to the bus. U1 is a 3 to 8 decoder which is used for decoding chip selects.

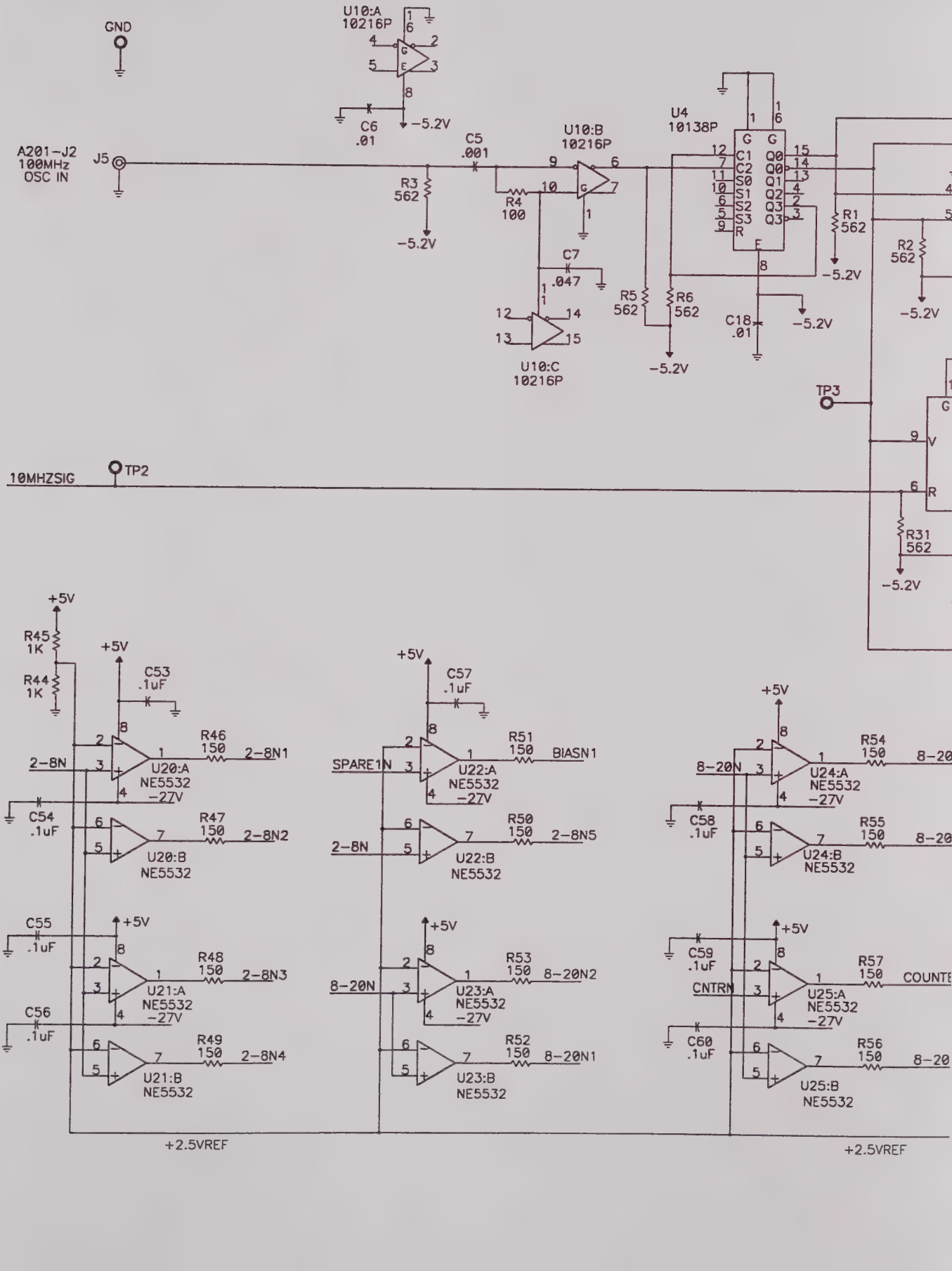

10MHz INT
A21-J1-3
J4
C32 .001
R22 100
CR3 1N4148
CR4 1N4148
C33 .01
C37 .01
R24 1K
U11:C 10216P
R32 562
-5.2V
C65 .01
U12:A 10102
U11:A 10216P
VBB1
R36 562
R35 562
C36 .01
U12:B 10102P
REF IN REAR PANEL BNC
J3
C34 .001
R23 100
CR5 1N4148
CR6 1N4148
C35 .01
U11:B 10216P
R25 1K
R34 562
C42 .001
+5V
C43 .01
U13 311N
R26 1K
R27 10K
C44 .01
Q3 2N29
CR7 2810
CR8 2810
C38 .001
R28 10K
R29 100K
C39 .01
U14 311N
R33 10K
C40 .01
C41 47uF 25V_E
J1
EDGE CONNECTOR
GND
BA3
BA2
BA1
BASN
BD13
BD12
BD7
BD15
BD3
BD5
BD0
BD1
BD8
BD6
BD9
BD10
BD14
BD11
BD2
BD4
SELN82
MODULE-P1-36
MODULE-P1-35
MODULE-P1-14
MODULE-P1-11
MODULE-P1-26
MODULE-P1-37
A16-J1-67
2-8N1
2-8N2
2-8N3
2-8N4
2-8N5
8-20N1
10 MHZ A
MODULE-P1-19
MODULE-P1-13
A5-J1-48
8-20N2
8-20N3
10 MHZ B
MODULE- P1-4
MODULE- P1-1
A6-J1-20
8-20N4
8-20N5
10 MHZ C
N/C
MODULE- P1-3
N/C
BIASN1
COUNTERN
10 MHZ D
MODULE-P1-23
MODULE-P1-21
2-20N
.01-2N
A21-J1-1
+15VOSC
A11-J1-39
-27V
+22V
+15V
C8 47uF 25V_E
L1 22uH
-5.2V
+5V
C9 47uF 25V_E
C11 +47uF 25V_E
C12 +47uF 25V_E
C13 +47uF 25V_E
C1 .01
BA1
BA2
BA3
SELN82
BASN
G1
G2A
G2B
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
CSN1
LOCK
U1 74HC138

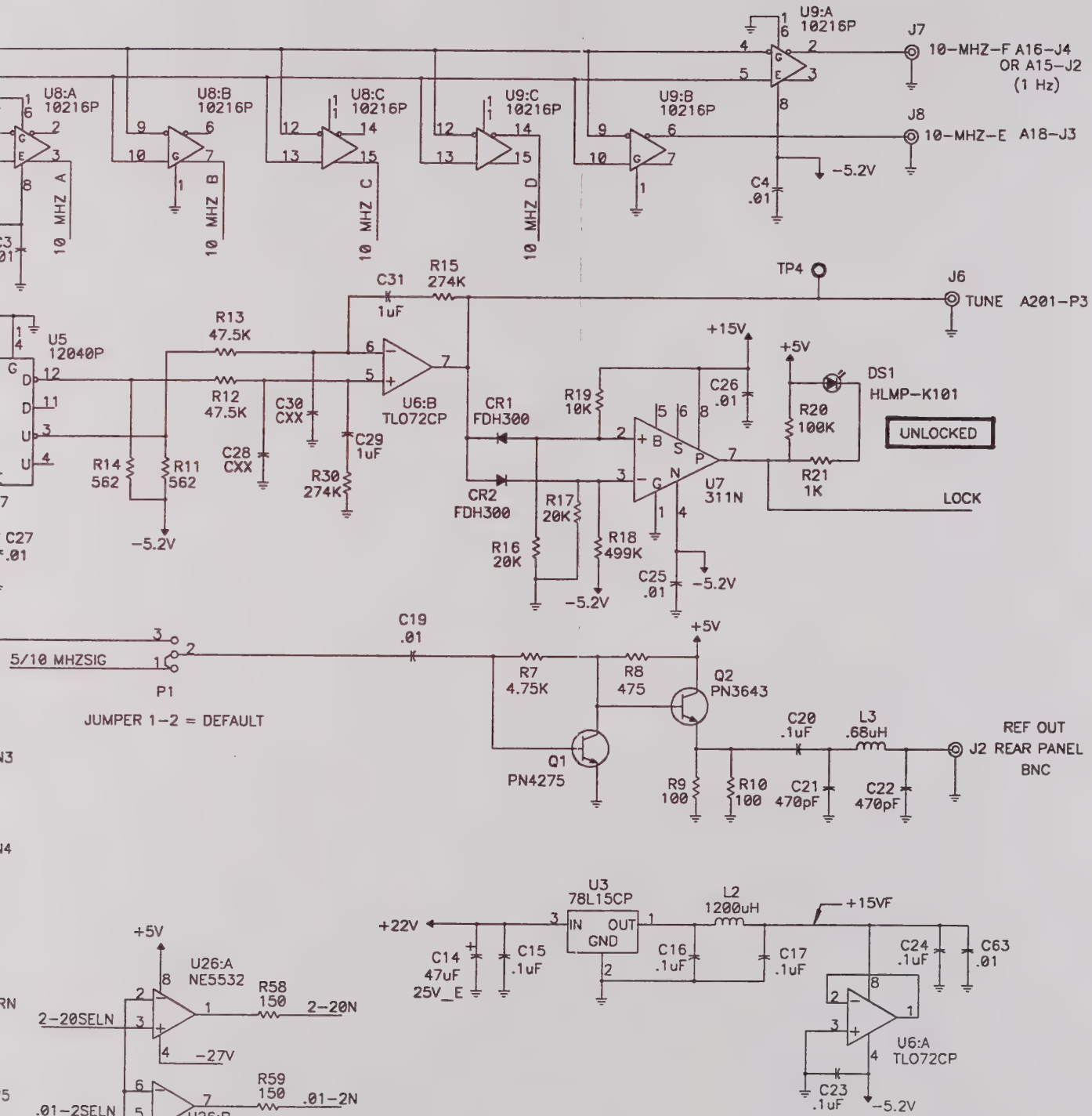



NOTES: UNLESS OTHERWISE SPECIFIED

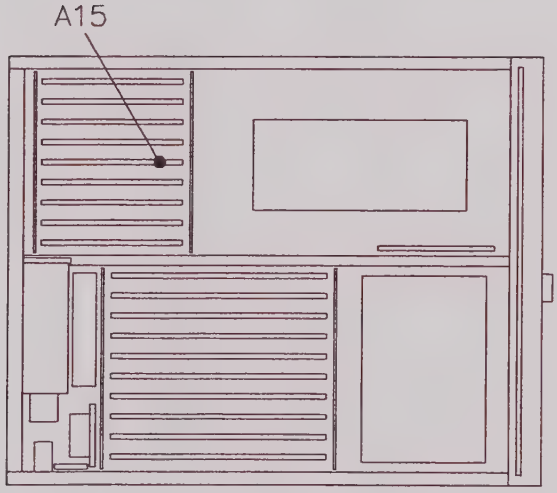
1.) RESISTORS ARE IN OHMS.
2.) RESISTORS ARE 1\5W,1%.
3.) * INDICATES 1\4W RESISTORS.
4.) CAPACITOR VALUES ARE IN uF.

**100 MHz Ref PLL (A14)**
**ASSY# 120BA06950 Rev A**
**Sheet 3 of 4**
**7-A14-3**

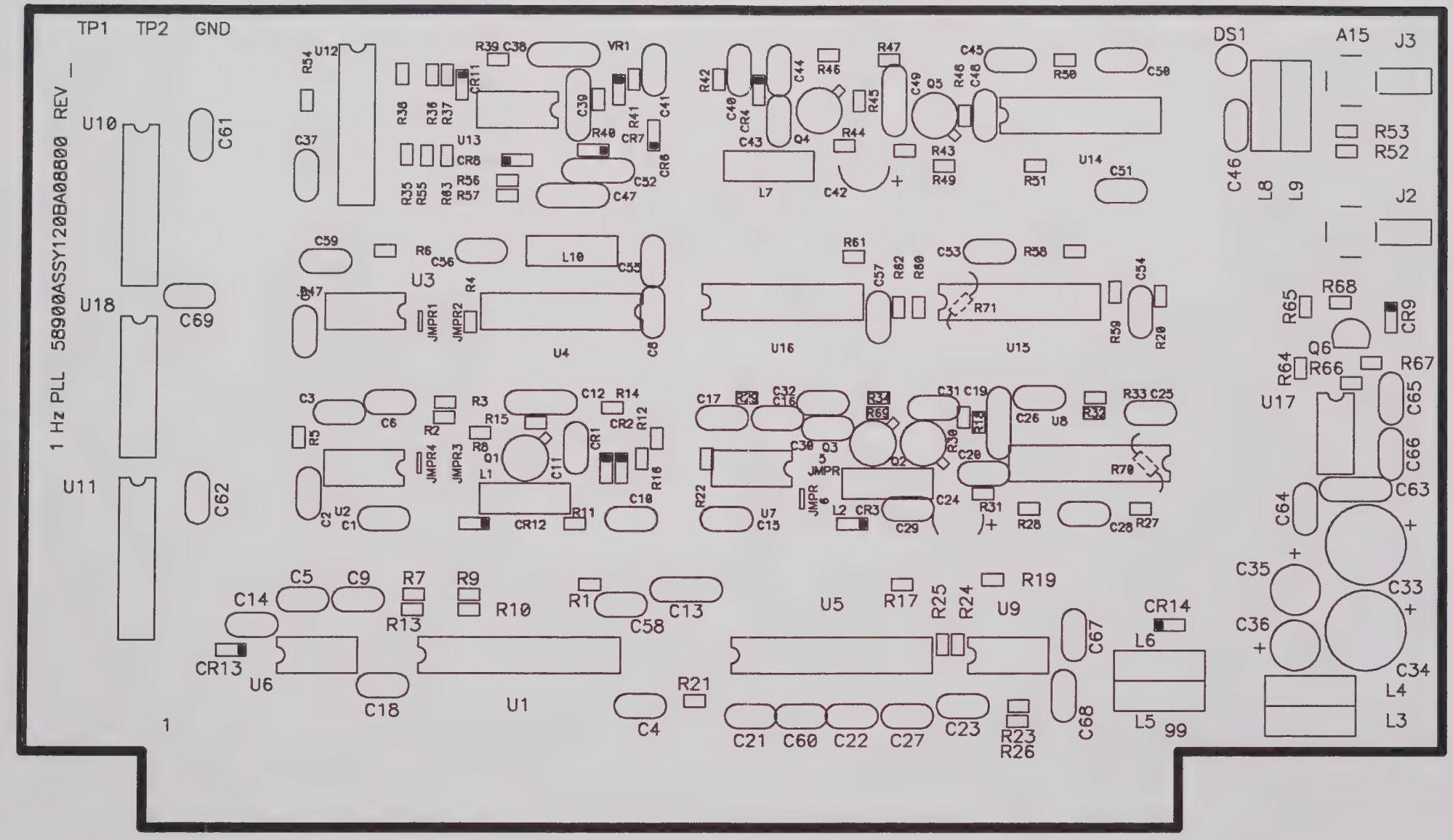

GND
U10:A
10216P
C6
.01
-5.2V
A201-J2
100MHz
OSC IN
J5
C5
.001
U10:B
10216P
R3
562
R4
100
C7
.047
U10:C
10216P
U4
10138P
R1
562
R2
562
R5
562
R6
562
C18
.01
TP3
10MHZSIG
TP2
+5V
R45
1K
R44
1K
C53
.1uF
2-8N
U20:A
NE5532
R46
150
2-8N1
C54
.1uF
U20:B
NE5532
R47
150
2-8N2
C55
.1uF
U21:A
NE5532
R48
150
2-8N3
C56
.1uF
U21:B
NE5532
R49
150
2-8N4
+2.5VREF
C57
.1uF
SPARE1N
U22:A
NE5532
R51
150
BIASN1
U22:B
NE5532
R50
150
2-8N5
8-20N
U23:A
NE5532
R53
150
8-20N2
U23:B
NE5532
R52
150
8-20N1
C58
.1uF
U24:A
NE5532
R54
150
C59
.1uF
U24:B
NE5532
R55
150
CNTRN
U25:A
NE5532
R57
150
C60
.1uF
U25:B
NE5532
R56
150




**100 MHz Ref PLL (A14)**
**ASSY# 120BA06950 Rev A**
**Sheet 4 of 4**
**7-A14-4**




**1 Hz Phase Locked Loop (A15)**
**ASSY# 120BA08800 Rev H**




**1 Hz PHASE LOCKED LOOP -- PC ASSY A15**

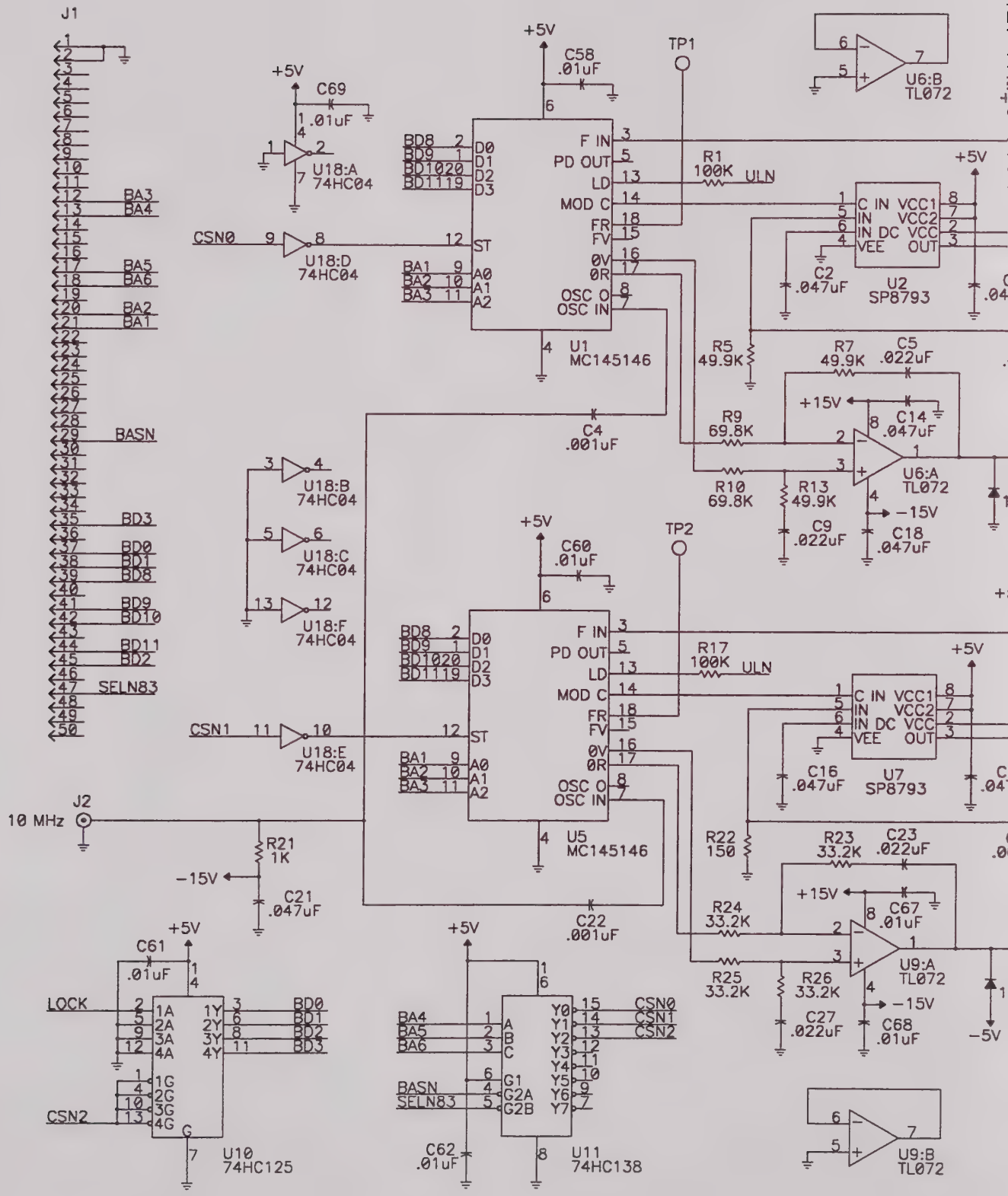
This circuit synthesizes a reference frequency programmable in fine increments. This reference is substituted for the standard timebase signal used by the reference phase lock loop. By setting the reference output from this circuit, the computer is able to specify RF frequency in 1 Hz increments. The output at J3 has a range of 10-12 MHz and a resolution of 2 Hz; when divided in half at the reference PLL input, the result is a 5-6 MHz reference programmable in 1 Hz steps.

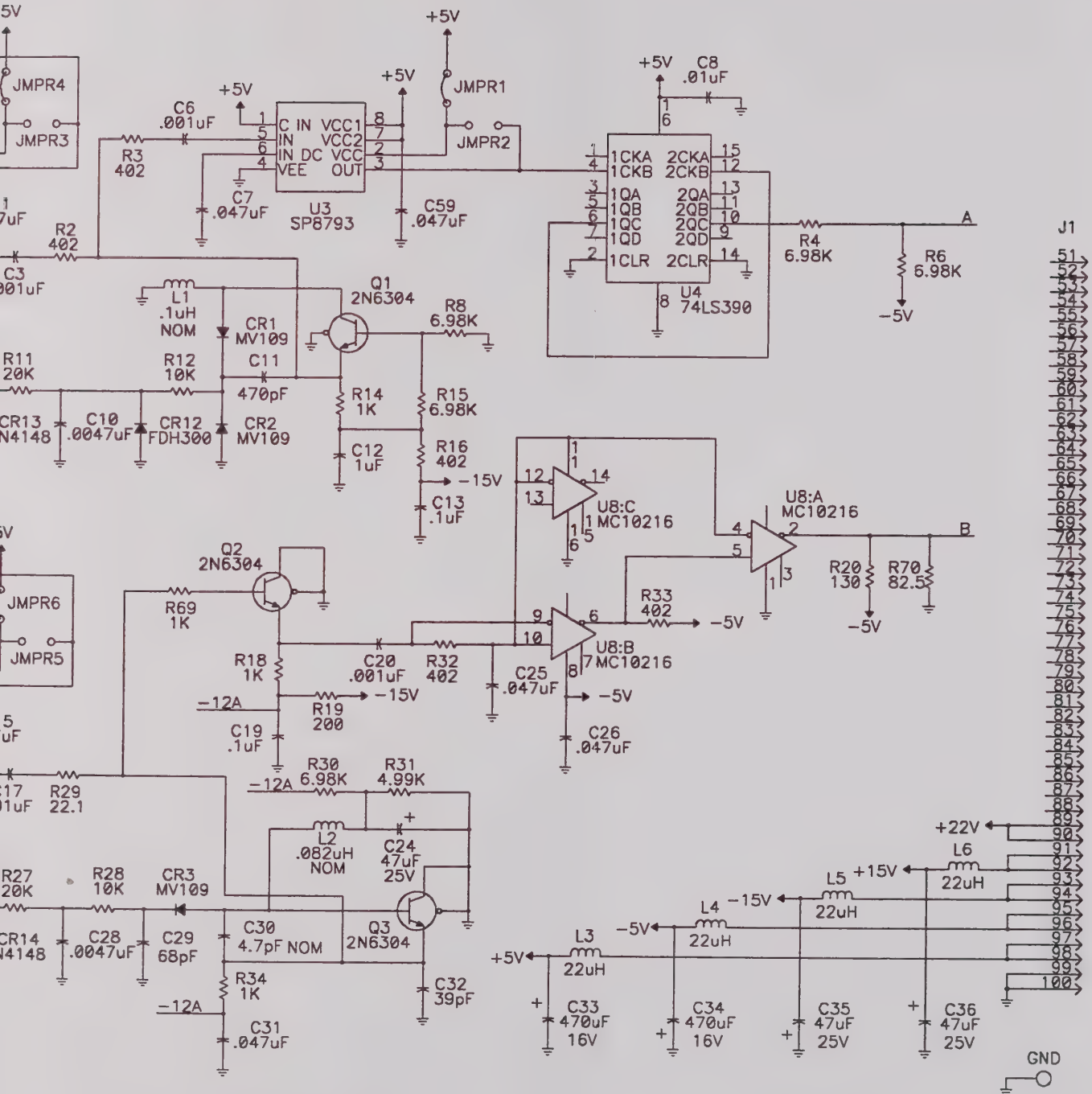
A 100-120 MHz voltage controlled oscillator (Q3) is controlled by U5. U5 is a synthesizer chip containing several programmable frequency dividers and a phase comparator, used in conjunction with an external prescaler (U7 which is programmed by U5 to divide by 40 or 41). U5 compares the prescaled feedback input from the VCO (U5-3) to the timebase input (U5-7) and produces pulsed outputs at U5-17 or U5-16 depending on which input is leading. A filter/amplifier circuit (U9 A) averages these pulses to produce a tuning input to the VCO. By programming the dividers in U5, the computer sets the VCO frequency in 50 kHz increments. The VCO frequency is buffered (Q2, U8 A and B) and applied to a mixer circuit consisting of the flip flops of U16.

The second frequency input to the U16 mixer circuit is produced by a second VCO (Q4) having the same range (100-120 MHz) but programmed in finer increments (20 Hz). This VCO is controlled by a PLL circuit consisting of a phase comparator (U12) and a filter/amplifier circuit (U13 A). The inputs to the phase comparator consist of feedback from the mixer circuit (U16-15) and a reference input from a third VCO circuit (Q1) divided down (by U3 and U4) to 100-150 kHz, giving 20 Hz increments. The PLL circuit phase locks the VCO to this reference. The circuit consisting of U13 B and U17 B performs as a window detector; when the PLL circuit is out of its normal control range, U17-7 goes high, illuminating the LED "unlock" indicator and pulling the 'LOCK' line low. The VCO output (from Q4) is divided by 10 (U14) yielding an output at J1 with a frequency range of 10-12 MHz and a resolution of 2 Hz.

The third VCO (Q1) has a frequency range of 100-150 MHz, programmed in 20 kHz increments, but dividers U3 and U4 reduce this frequency to 100-150 kHz so that it can be used as a reference input by phase comparator U12. U1 is the same type of synthesizer chip as U5, and its prescaler chip U2 also divides by 40 or 41. Filter/amplifier circuit U6 A converts the phase comparator outputs of U1 into a tuning voltage for the VCO. U11 is a decoder chip used for decoding chip selects. U10 is a tri-state buffer for outputting board outputs to the bus.

**1 Hz Phase Locked Loop (A15)**
**ASSY# 120BA08800 Rev H**
**Sheet 2 of 4**

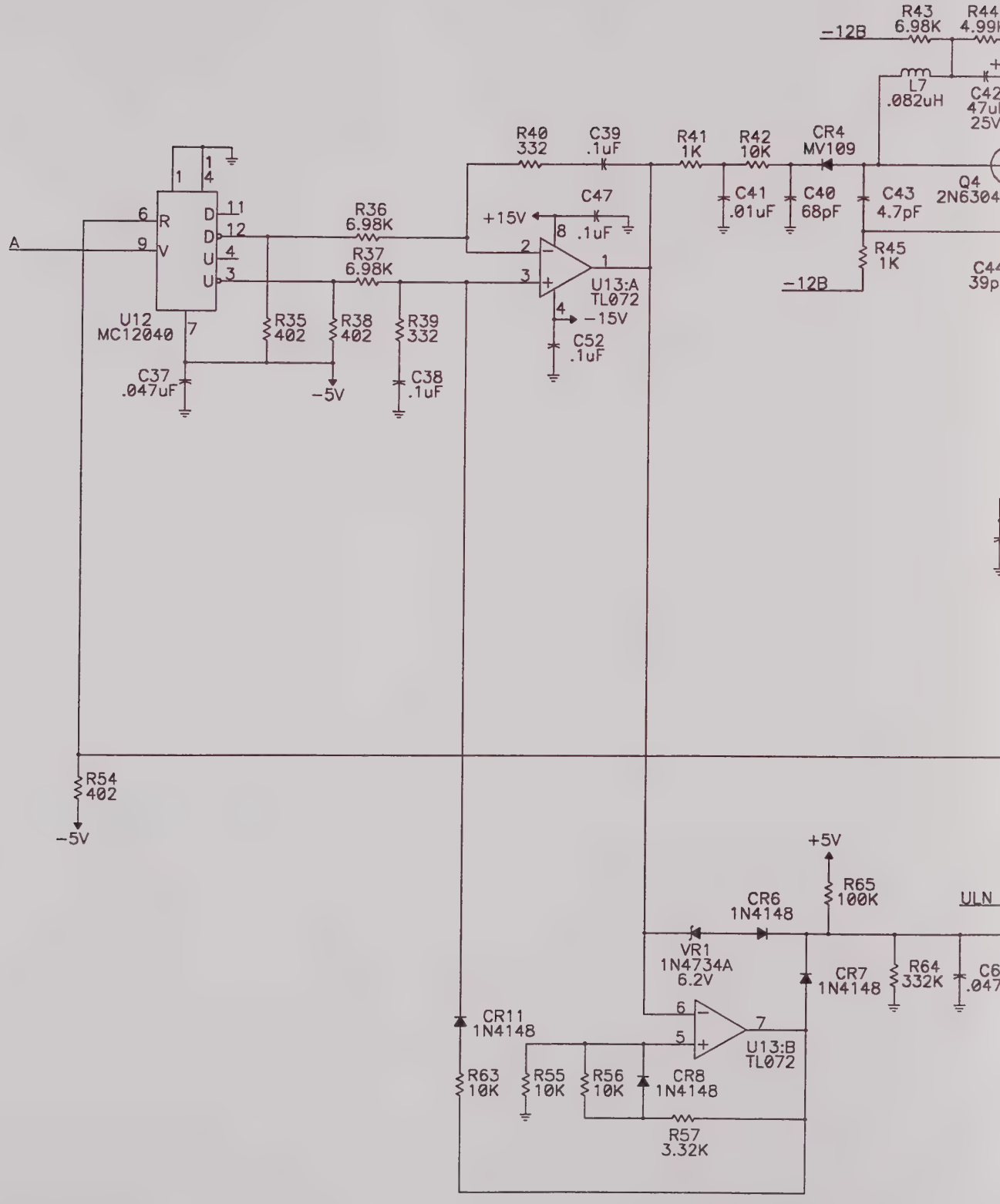

J1
BA3
BA4
BA5
BA6
BA2
BA1
BASN
BD3
BD0
BD1
BD8
BD9
BD10
BD11
BD2
SELN83
+5V
C69
.01uF
U18:A
74HC04
CSN0
U18:D
74HC04
BD8
BD9
BD1020
BD1119
BA1
BA2
BA3
D0
D1
D2
D3
ST
A0
A1
A2
F IN
PD OUT
LD
MOD C
FR
FV
0V
0R
OSC O
OSC IN
U1
MC145146
C58
.01uF
TP1
R1
100K
ULN
U6:B
TL072
C IN
IN
IN DC
VEE
VCC1
VCC2
VCC
OUT
U2
SP8793
C2
.047uF
R5
49.9K
R7
49.9K
C5
.022uF
+15V
C14
.047uF
R9
69.8K
U6:A
TL072
R10
69.8K
R13
49.9K
C9
.022uF
-15V
C18
.047uF
C4
.001uF
U18:B
74HC04
U18:C
74HC04
U18:F
74HC04
C60
.01uF
TP2
R17
100K
ULN
U7
SP8793
C16
.047uF
CSN1
U18:E
74HC04
J2
10 MHz
R21
1K
C21
.047uF
C22
.001uF
U5
MC145146
R22
150
R23
33.2K
C23
.022uF
R24
33.2K
U9:A
TL072
R25
33.2K
R26
33.2K
C27
.022uF
C67
.01uF
C68
.01uF
-5V
C61
.01uF
LOCK
CSN2
1A
2A
3A
4A
1Y
2Y
3Y
4Y
1G
2G
3G
4G
U10
74HC125
C62
.01uF
BA4
BA5
BA6
BASN
SELN83
A
B
C
G1
G2A
G2B
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
CSN0
CSN1
CSN2
U11
74HC138
U9:B
TL072

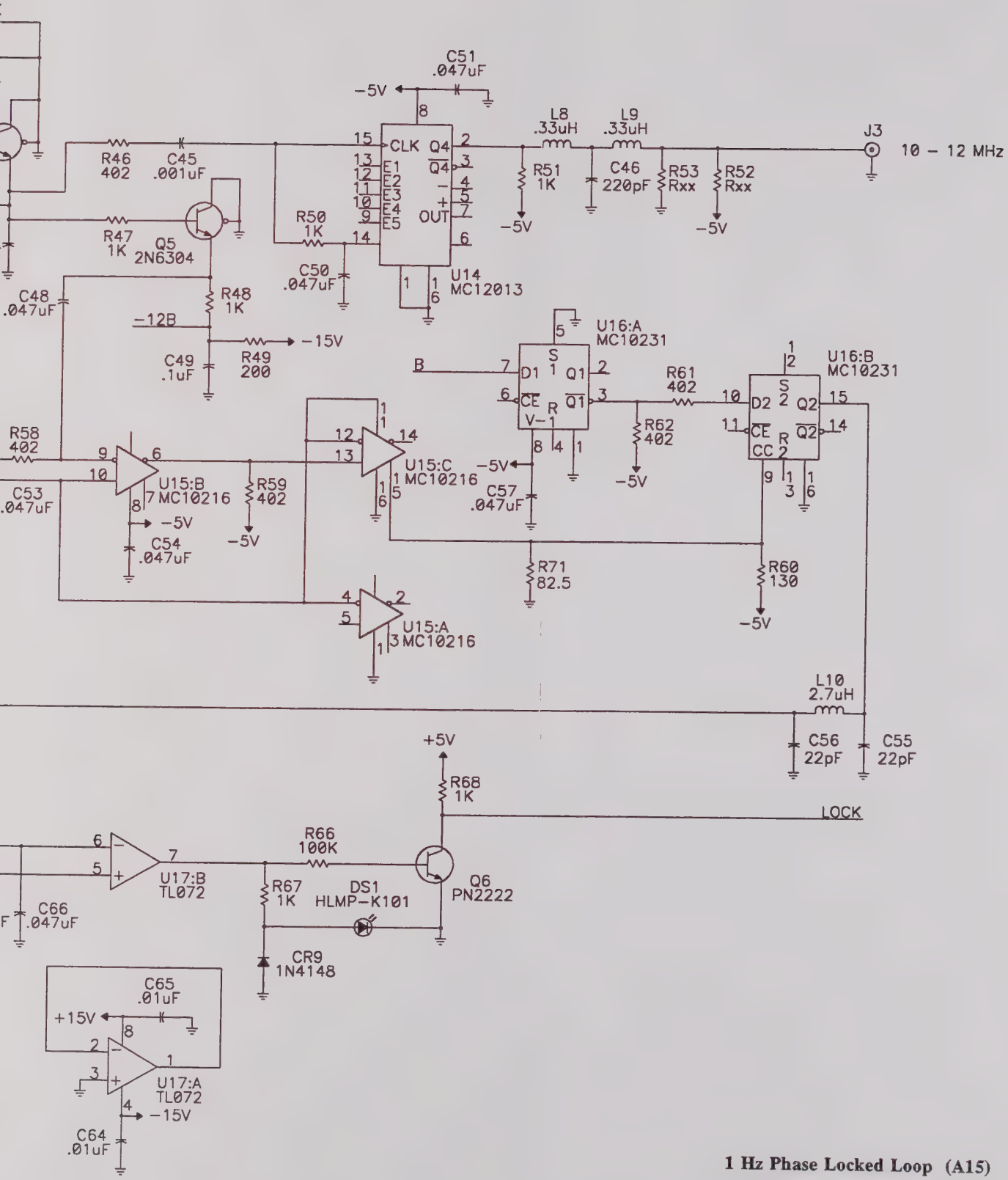



NOTES: UNLESS OTHERWISE SPECIFIED

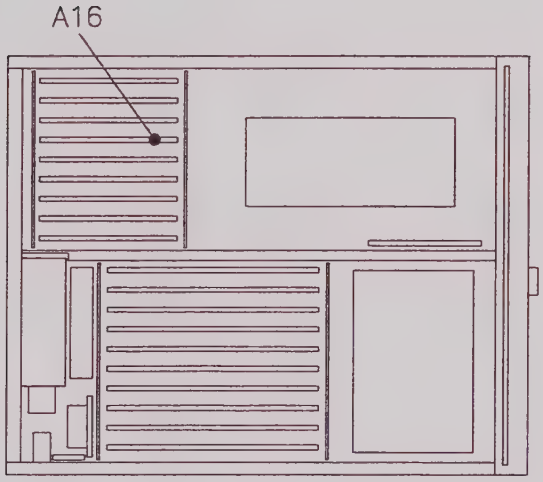
1. CAPACITOR VALUES ARE IN uF
2. RESISTOR VALUES ARE IN OHMS
3. RESISTORS ARE 1/5W, 1%

**1 Hz Phase Locked Loop (A15)**
**ASSY# 120BA08800 Rev H**

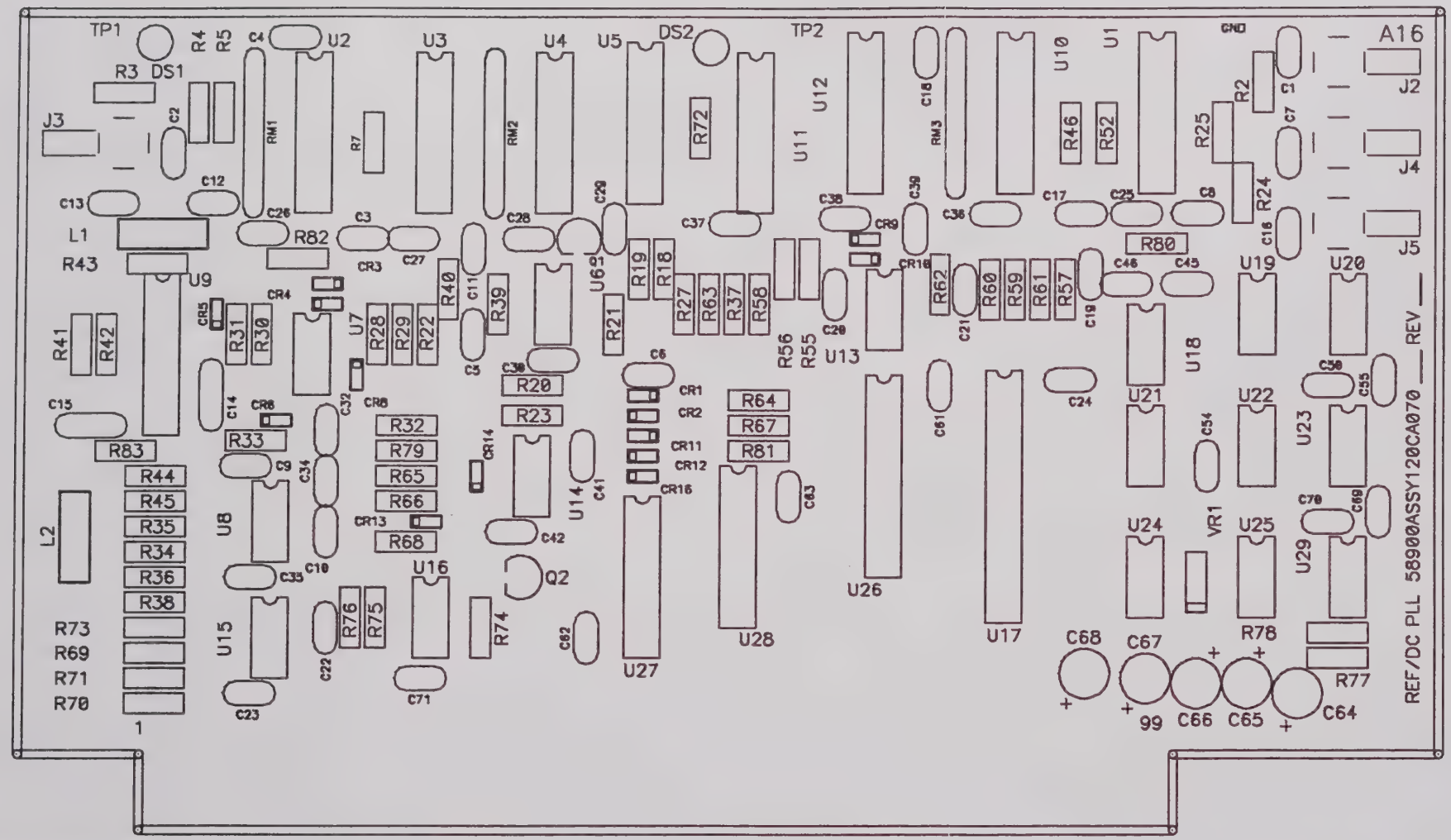

R43
6.98K
-12B
L7
.082uH
R40
332
C39
.1uF
R41
1K
R42
10K
CR4
MV109
C41
.01uF
C40
68pF
C43
4.7pF
Q4
2N6304
R45
1K
-12B
C47
+15V
.1uF
R36
6.98K
R37
6.98K
U13:A
TL072
-15V
C52
.1uF
A
U12
MC12040
R35
402
R38
402
R39
332
C37
.047uF
-5V
C38
.1uF
R54
402
-5V
+5V
R65
100K
CR6
1N4148
VR1
1N4734A
6.2V
CR7
1N4148
R64
332K
CR11
1N4148
U13:B
TL072
R63
10K
R55
10K
R56
10K
CR8
1N4148
R57
3.32K




**1 Hz Phase Locked Loop (A15)**
**ASSY# 120BA08800 Rev H**




**Ref/DC PLL (A16)**
**ASSY# 120BA07000 Rev E**




**REFERENCE/ DOWNCONVERTER PHASE LOCKED LOOPS -- PC ASSY A16**

This board holds the Reference PLL, and the Downconverter ( or Fixed LO) PLL circuitry as well as the logic and drivers for the Downconverter filters.

The REFERENCE PLL fine tunes the reference YIG oscillator in order to phase-lock it to a harmonic of the 100 MHz oscillator (see A201) and ultimately to the instruments timebase. The phase detector U5 compares two 5 MHz inputs, one from the reference sampler IF (J2), buffered by U1 C, and the other one from the internal or external input (J4 or J3 respectively). If the two 5 MHz inputs are out of phase, wide pulses will appear at one of U5's outputs (pins 3 or 12, depending on which input is leading). The filter/amplifiers (U6 A and B and associated components) convert these pulses into a correction voltage which is filtered by L1, C12 & C13 and then supplied to U9 which drives the fine tuning (or FM) coil of the reference YIG oscillator. The PLL circuit adjusts the frequency of the oscillator in whichever direction will reduce the phase difference between the two 5 MHz inputs. The PLL output goes more positive to increase frequency and more negative to decrease it.

The reference frequency is mixed with a 100 MHz comb line and should be 5 MHz **above** the 100 MHz multiple. If the reference frequency falls above the desired multiple, the output voltage at U6-1 will be higher than normal. The kicker circuit U7 A and associated components will detect this by comparing this voltage with a reference voltage set by R30, R31 and kick the output of U6 B high, resulting in the output of U6 A going low thus decreasing the oscillator frequency. On the contrary, if the output frequency is too low the kicker circuit U7 B and associated components will detect the output of U6 A being below a certain voltage level (set by R79, 32 and 33) and kick U6 such that the output at pin 1 will go high thereby increasing the output frequency.

Whenever the kicker circuits (U7) kick, C10 or C9 are charged up such that the lock detector U8 pulls the REF_LOCK signal low thereby illuminating the lock LED DS1.

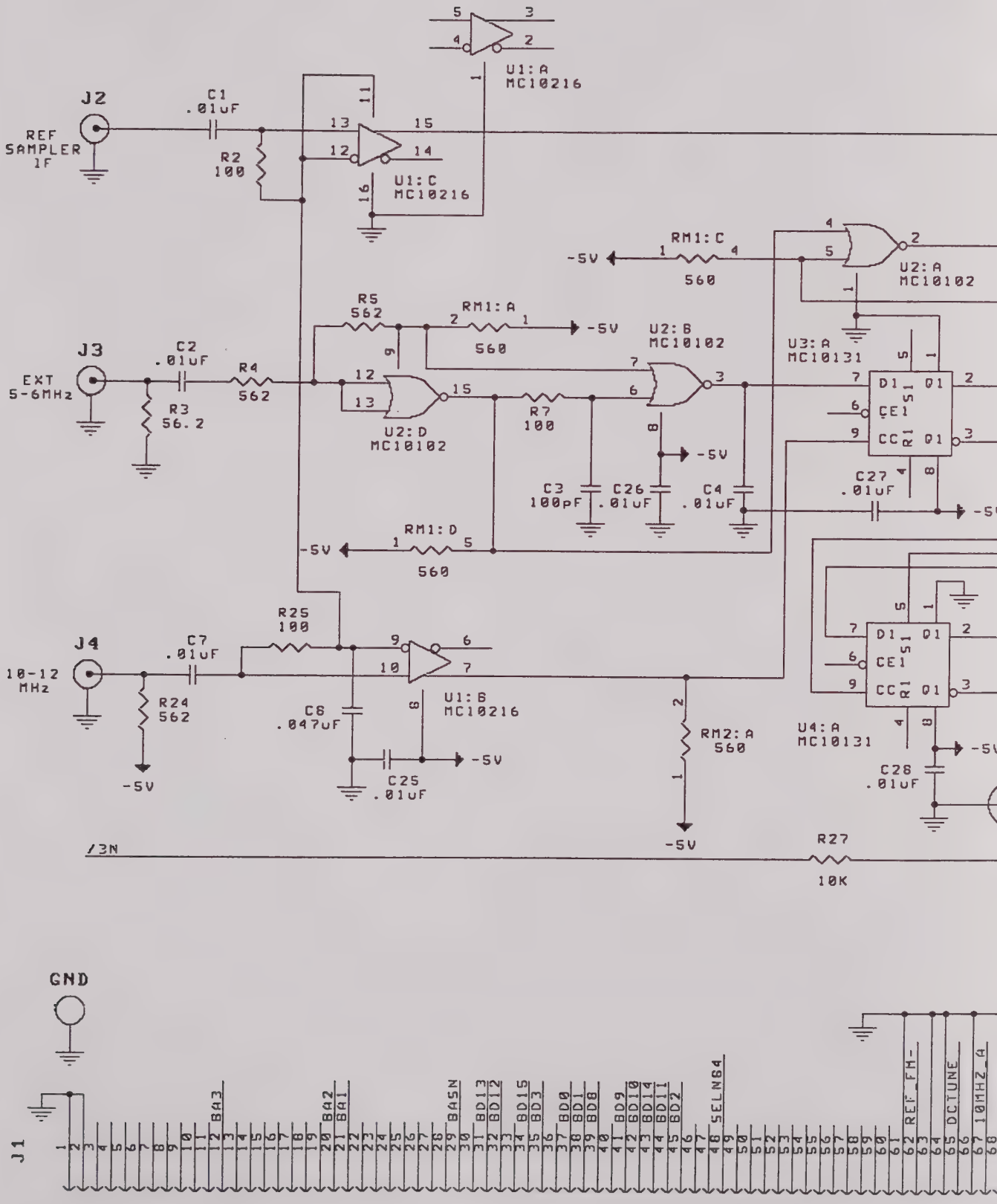
The 5 MHz input to the phase detector is derived either from the 10 MHz input at J4 or from the 5-6 MHz input at J3. The 5-6MHz input, if present must be detected so that the 10 MHz path will be disabled. This is achieved by delaying one input to U2 B using R7 an C3. This causes U2-3 output to be low thus disabling the 10 MHz from propagating thru U3 A. Instead the 5-6 MHz input propagates thru to the phase detector U5. When no 5-6 MHz input is present the 10 MHz propagates thru U3 A and B, being divided by two, and then on thru U2 C to the phase detector input.

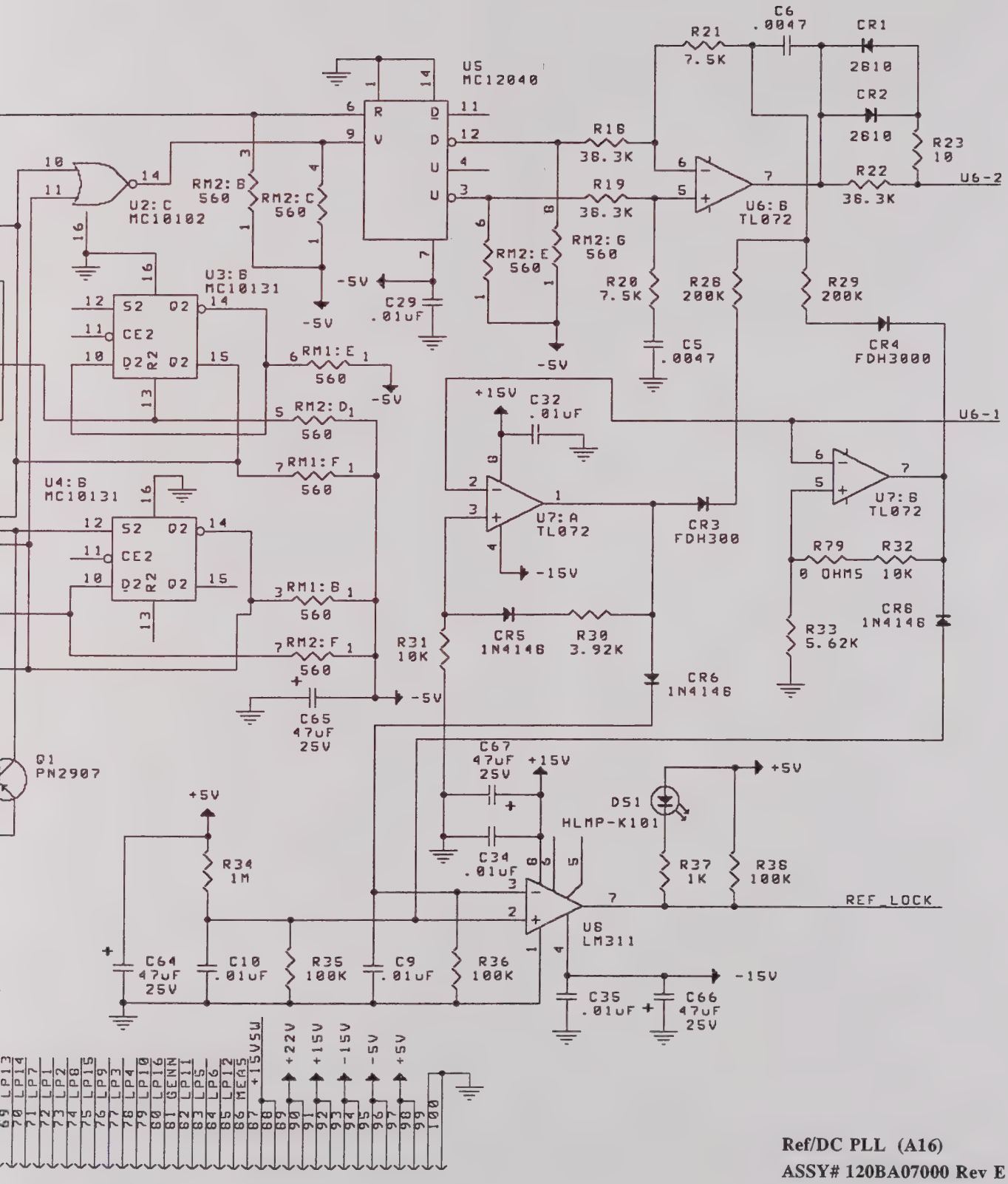
At some output frequencies the sampler IF is 1.667 MHz rather than 5 MHz; in that situation the control input at Q1 causes the flip flop U4 to be activated which removes two pulses out of every three coming from either U2-2 or U3-15. This effectively divides the 5 MHz by three which yields the desired 1.667 MHz signal.

The DOWNCONVERTER PLL (or Fixed LO PLL) circuitry functions basically identical to the Reference PLL. One difference is that there is only one set of inputs to the phase detector U11, the 10 MHz and the DC sampler IF. When the loop is locked the DC sampler IF should be 5 MHz, the flip flop U12 divides the 10 MHz reference by two yielding 5 MHz. The other difference is that this loop is turned off by U16 and Q2 when the unit is not operating in the downconverter range. This reduces spurs and noise which can be added by this circuitry when it is not locked.

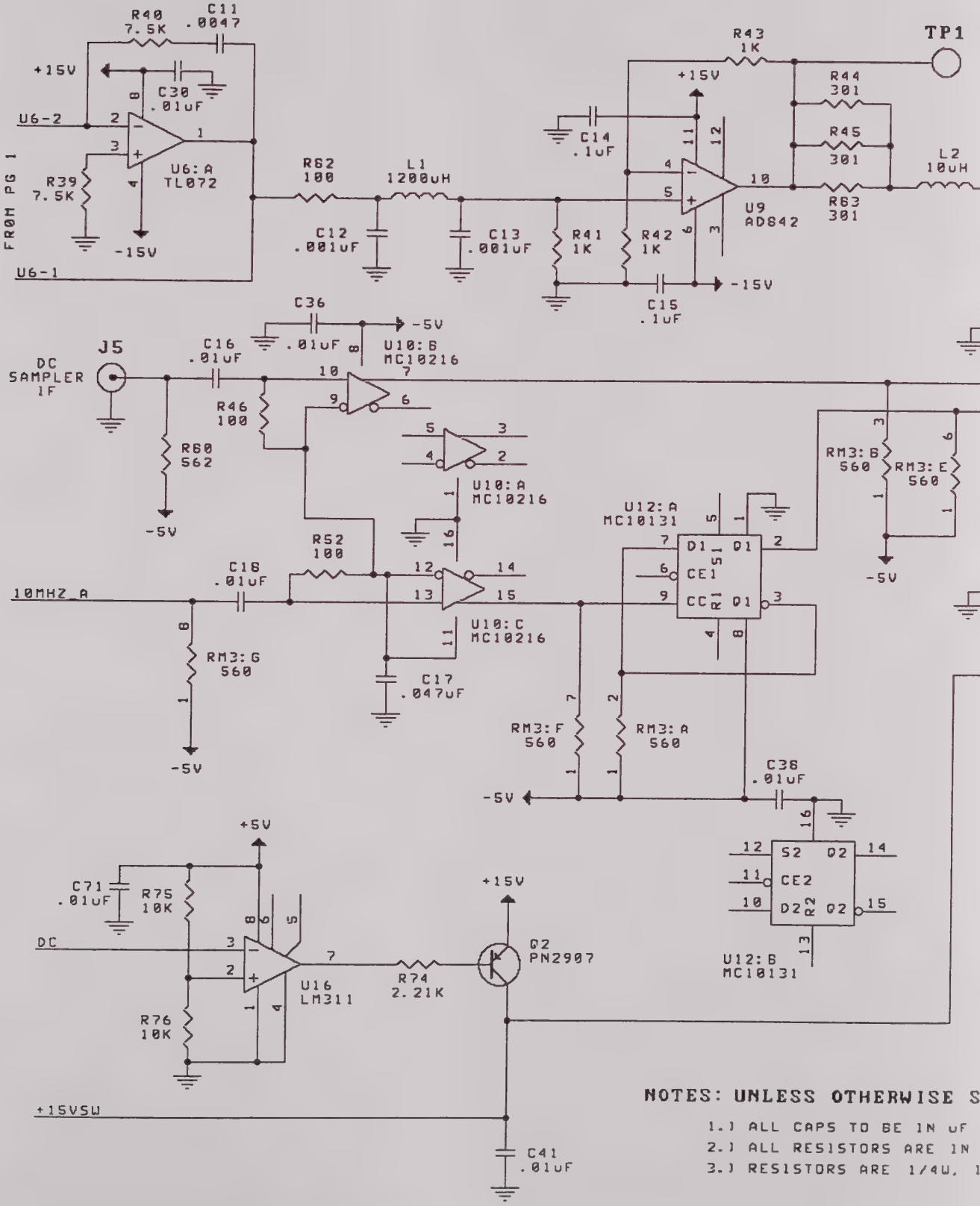
This board also provides downconverter filter drive logic. U17 is a 4 to 16 decoder which decodes logic from the computer there by selecting each of the downconverter filters as appropriate via their drive circuitry U18 thru U25. The GENN and MEAS logic drives for the computer are provided by U29.

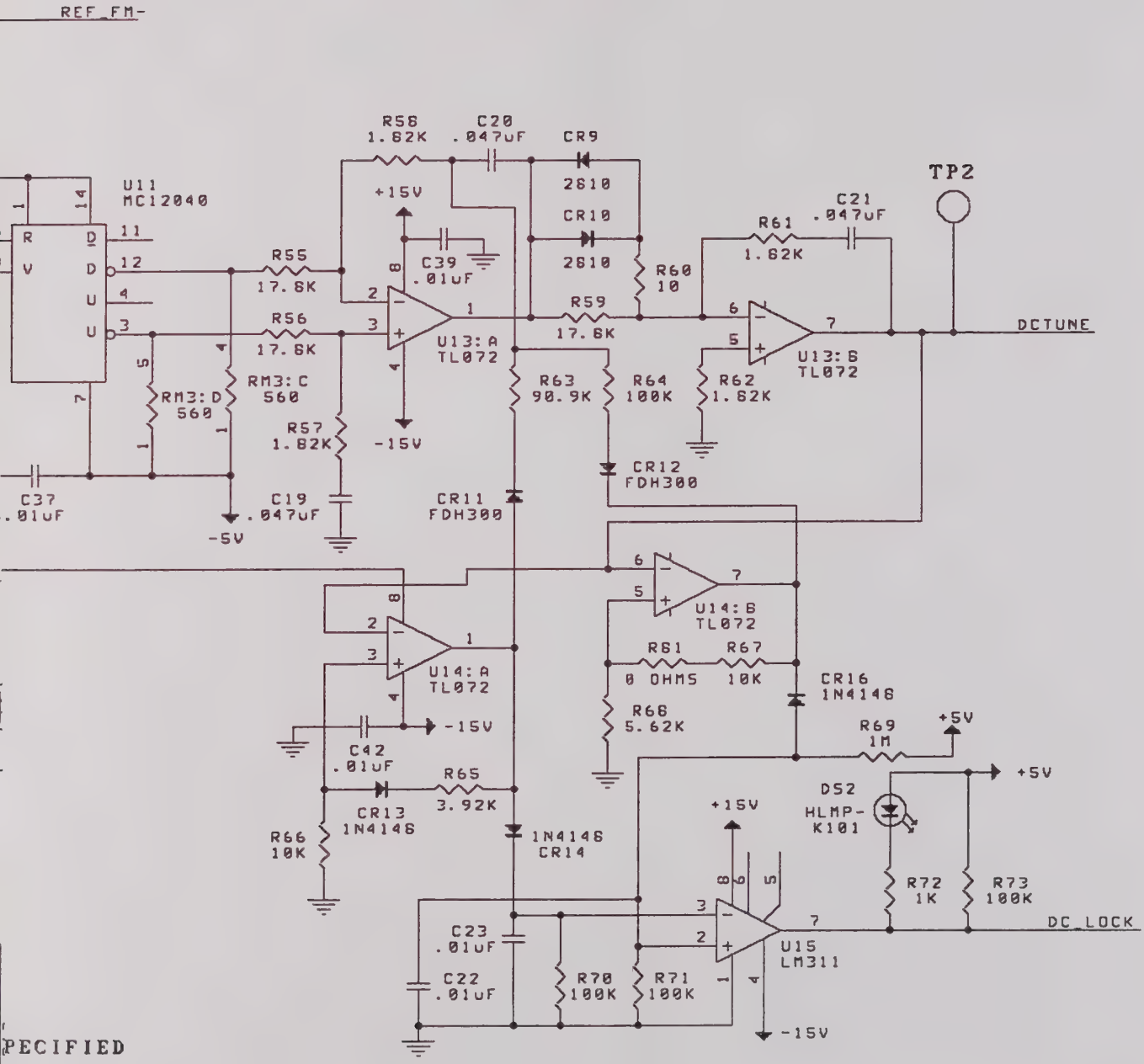
U27 provides chip selects for various IC's on the board and U26 and U28 serve as buffers required for computer bus interface.


J2
REF SAMPLER IF
C1 .01uF
R2 100
U1:A MC10216
U1:C MC10216
J3
EXT 5-6MHz
C2 .01uF
R3 56.2
R4 562
R5 562
RM1:A 560
-5V
U2:B MC10102
U2:D MC10102
R7 100
C3 100pF
C26 .01uF
C4 .01uF
RM1:C 560
U2:A MC10102
U3:A MC10131
C27 .01uF
RM1:D 560
J4
10-12 MHz
C7 .01uF
R24 562
R25 100
C8 .047uF
C25 .01uF
U1:B MC10216
RM2:A 560
U4:A MC10131
C28 .01uF
/3N
R27 10K
GND
J1
BA3
BA2
BA1
BASN
BD13
BD12
BD15
BD3
BD0
BD1
BD8
BD9
BD10
BD14
BD11
BD2
SELN84
REF_FM-
DCTUNE
10MHZ_4

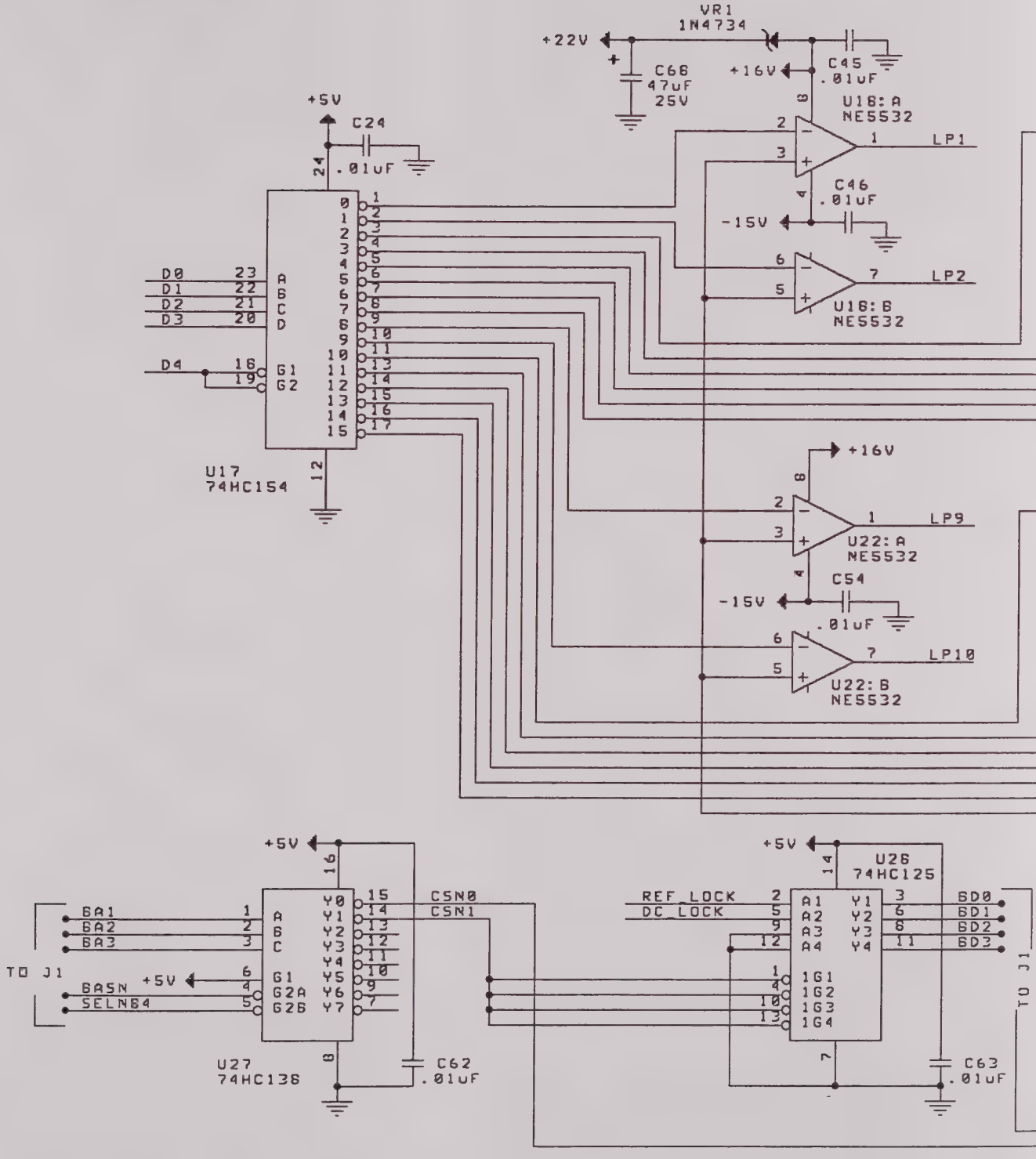


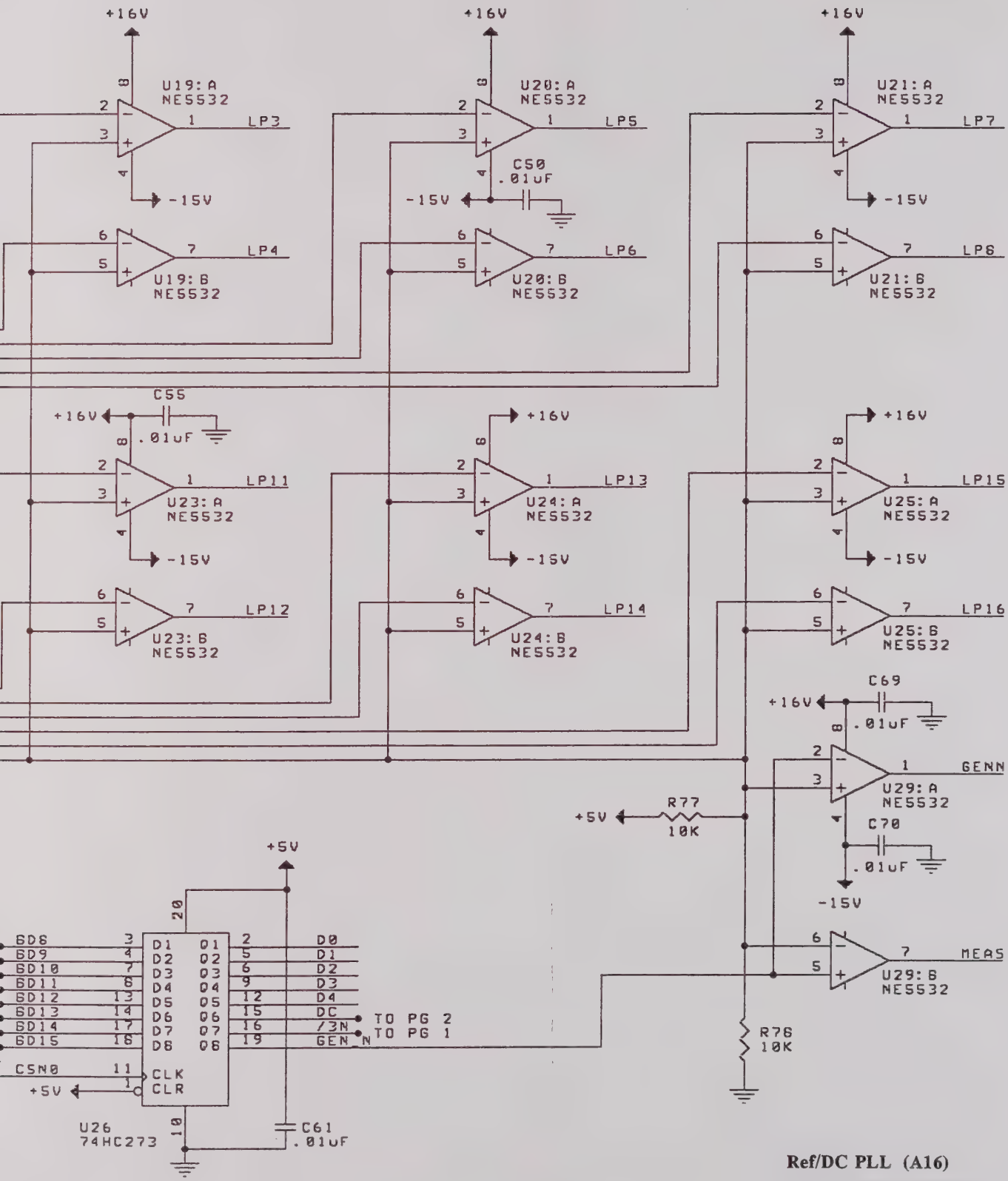

**Ref/DC PLL (A16)**
**ASSY# 120BA07000 Rev E**
**Sheet 3 of 5**
**7-A16-3**


R40
7.5K
C11
.0047
+15V
C30
.01uF
U6-2
U6-1
R39
7.5K
U6:A
TL072
-15V
FROM PG 1
R62
100
L1
1200uH
C12
.001uF
C13
.001uF
R41
1K
R42
1K
C14
.1uF
C15
.1uF
R43
1K
TP1
R44
301
R45
301
R63
301
L2
10uH
U9
AD842
C36
.01uF
-5V
U10:B
MC10216
J5
DC
SAMPLER
1F
C16
.01uF
R46
100
R60
562
U10:A
MC10216
R52
100
C18
.01uF
10MHZ_A
U10:C
MC10216
C17
.047uF
RM3:G
560
U12:A
MC10131
RM3:B
560
RM3:E
560
RM3:F
560
RM3:A
560
C38
.01uF
U12:B
MC10131
+5V
C71
.01uF
R75
10K
DC
R76
10K
U16
LM311
R74
2.21K
Q2
PN2907
+15VSW
C41
.01uF
NOTES: UNLESS OTHERWISE S
1.) ALL CAPS TO BE IN uF
2.) ALL RESISTORS ARE IN
3.) RESISTORS ARE 1/4W, 1

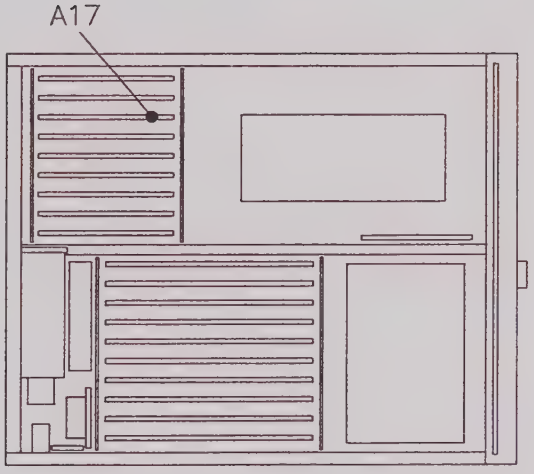



**Ref/DC PLL (A16)**
**ASSY# 120BA07000 Rev E**
**Sheet 4 of 5**
**7-A16-4**

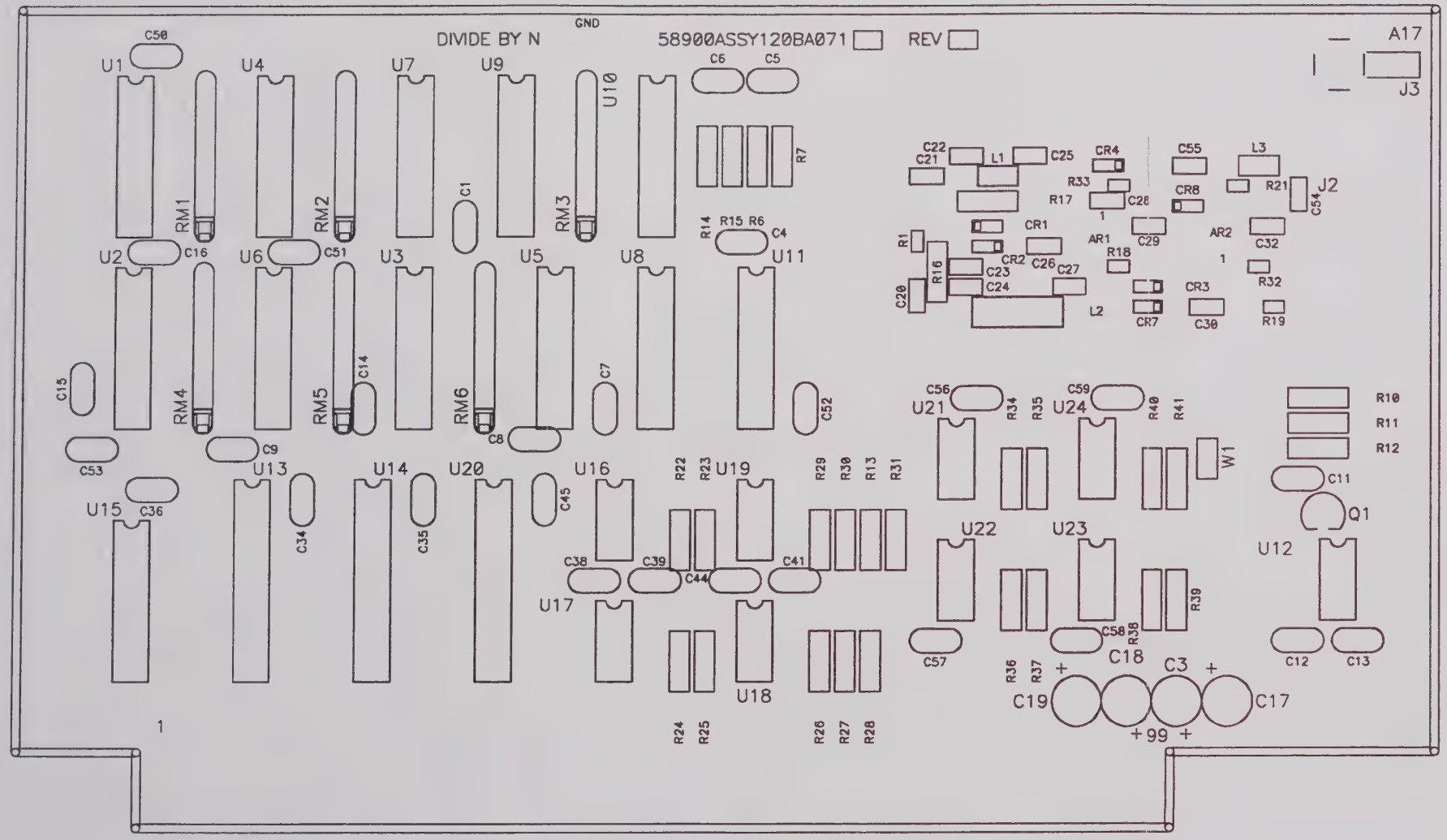

VR1
1N4734
+22V
C68
47uF
25V
+16V
C45
.01uF
U18:A
NE5532
LP1
C46
.01uF
-15V
U18:B
NE5532
LP2
+5V
C24
.01uF
U17
74HC154
D0
D1
D2
D3
D4
+16V
U22:A
NE5532
LP9
C54
-15V
.01uF
U22:B
NE5532
LP10
+5V
U27
74HC138
BA1
BA2
BA3
TO J1
BASN
SELNB4
CSN0
CSN1
C62
.01uF
+5V
U26
74HC125
REF_LOCK
DC_LOCK
BD0
BD1
BD2
BD3
C63
.01uF
TO J1




**Ref/DC PLL (A16)**
**ASSY# 120BA07000 Rev E**
**Sheet 5 of 5**
**7-A16-5**




**Divide By N (A17)**
**ASSY# 120BA07150 Rev A**
**Sheet 1 of 5**
**7-A17-1**




**DIVIDE BY N -- PC ASSY A17**

This circuit is a programmable frequency divider. It is set by the computer with a divisor between 95 and 395. Its frequency input is the 95 to 395 MHz I.F. from the reference mixer. The divided I.F. is supplied to the output phase lock loop and should be exactly 1 MHz when the output loop is locked. A 2 stage amplifier is used to provide enough gain throughout the operating frequency range to drive the Mod-8/9 counter (U11). AR1 and AR2 are amplifiers. CR1,2 and C23 detect the level of the signal at the output of AR1 and U12 A and Q1 provide bias to CR3, CR4, CR7 and CR8 to attenuate the signal as required, thereby providing a form of automatic level control. L2, C24 and C27 are required for power supply filtering. L3, C54, C55, and L1, C25, C22 are low pass filters for the IF signal.

In the discussion of the divider circuit, terms are defined as follows: "I.F. cycles" refers to the amplified I.F. from the reference mixer, which is used as a timing clock by the Mod 8/9 counter; "clock cycles" refers to the output of the Mod 8/9 counter, U11-2, which is used as a timing clock by the three-bit and six-bit counters; "division cycles" refers to the output signal, U9-14, which should have a rate of 1 MHz when the loop is locked. I.F. cycles are the fastest of the three; division cycles are the slowest.

The divisor, selected by the computer, is supplied as a nine-bit binary number at TTL levels to the 10124 translators (U1, 2 and 3), which convert the bits to ECL levels. Bits 0, 1 and 2 control the three-bit counter (U5) and bits 3 through 8 control the six-bit counter consisting of U4, 6 and 7. These two counters operate independently, but they use the same timing clock and they count down simultaneously.

The outputs of the three-bit counter U5, by way of gate U8, program the Mod- 8/9 counter U11 ; while U5 is counting down, U11 divides the I.F. by 8. In the case of most divisors, it is necessary for the I.F. to be divided by 9 for some portion of the division cycle; only when the three lowest bits are all zero is U11 programmed as a Mod-8 counter throughout the division cycle (a situation which can only occur if the divisor itself happens to be an even multiple of eight). Whenever it reaches zero, U5 stops counting until it is preset at the next division cycle.

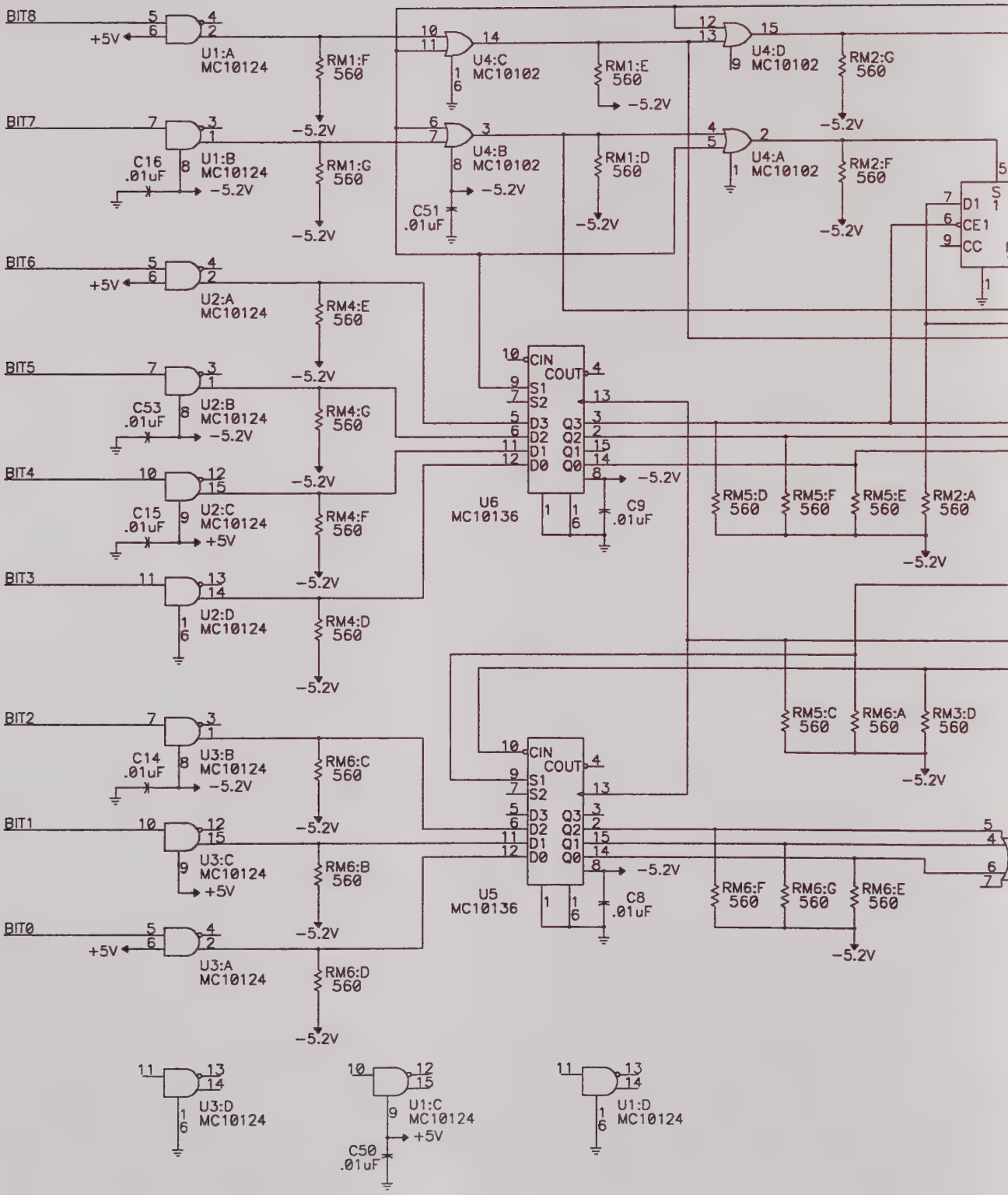
The six-bit counter (U6 and U7) continues counting down after U5 has reached zero and U11 has entered the Mod-8 phase of the division cycle. The lowest number it ever counts down from is 11, (binary 001011) whereas the highest number the three-bit counter ever counts down from is 7 (binary 111); therefore the three-bit counter always finishes first. When the six-bit counter has completed its count, gate U8-14 goes high; this line, applied to the 'D' input of U9, allows U9-14 to go low (this represents the falling edge of the output waveform) on the next clock transition; the output is also used to preset the six-bit counter. The three-bit counter is preset by U9-2; this transition occurs a half-cycle later than for the other counter because U9-2, unlike U9-15, is triggered by the complement of the divider circuit's clock (U11-3). The delays involved in driving the output low, presetting the counters, and triggering them to count down again result in the addition of two clock cycles to the division cycle--that is, U11 will perform two extra divisions by 8 before the next division cycle can begin. To compensate for this, U6's Q1 output is not connected to the OR gate U8-14; the six-bit counter counts down only to two, not to zero, before sending to U9 the high level that initiates the output transition and presets the counters. The duration of the output low pulse is one clock cycle, which is equal to eight I.F. cycles; because the I.F. is variable, the width of the low pulse varies (between about .02 and .08 microseconds).

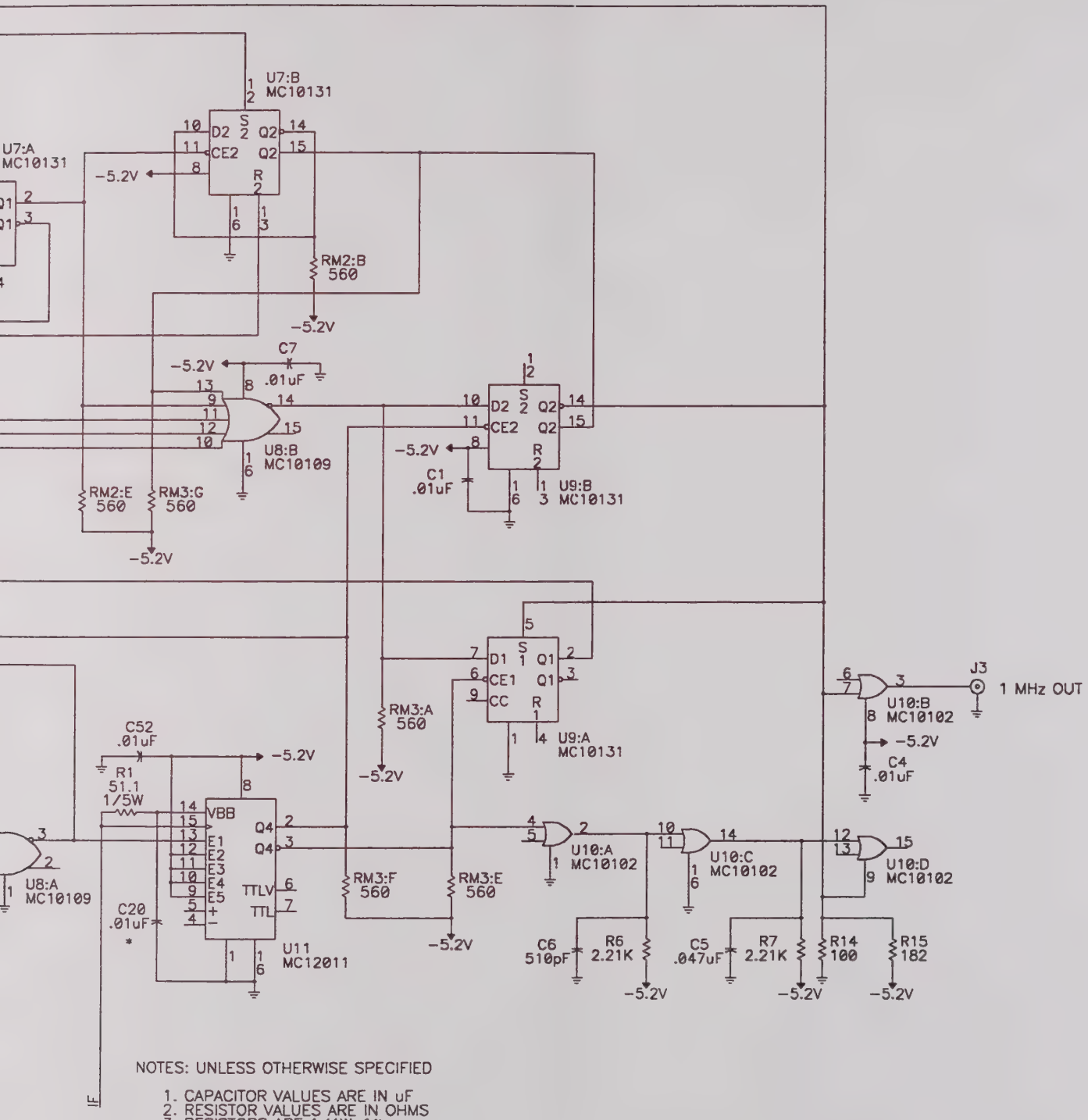
EXAMPLE: When the divisor is to be 195 (this occurs when the I.F. is 195 MHz), the translators are programmed with the binary equivalent of 195 (011000011). This breaks down as 3 for the three-bit counter (binary 011), and 24 for the six-bit counter (binary 011000). For the first three clock cycles U11 divides the I.F. by 9, for a total of 3 X 9 = 27 I.F. cycles. The three-bit counter then reaches zero and programs U11 to divide by 8 for the remaining clock cycles (21, since three of the six-bit counter's 24 cycles have already been counted simultaneously with the other counter). After 21 X 8 = 168 further I.F. cycles (bringing the total so far counted to 195) the low-going pulse of the output waveform occurs, the counters are preset and the division cycles recommences. Of course, to compensate for the cycles added by delay in presetting the counters, the six-bit counter actually stopped early by 2 clock cycles (2 X 8 = 16 I.F. cycles); the high level at U8-14 occurs two clock cycles before the beginning of the next division cycle because two clock pulses are needed to initiate that division cycle. Since 195 I.F. cycles occurred during one division cycle, the circuit has divided the input frequency by 195.

The OR gate U10 and four passive components are used to shut down the output of the circuit under conditions that would interfere with normal operation of the phase lock loop. Under normal conditions, with an I.F. input in the 95-395 range, the clock frequency applied to U10-4 will be above 10 MHz. The filter components between the three gates produce a low at U10-12, and the third gate does not interfere with the circuit output frequency. If the I.F. drops substantially below the normal range, however, and the clock frequency at U10-4 falls well below 10 MHz, the filter action will not be sufficient to have the same effect; U10-9 will go to an ECL high, preventing any waveform from reaching the phase lock loop. The reason for this precaution is that the Mod 8/9 counter responds erratically to frequencies below its intended range, and could prevent the PLL circuit from recovering phase lock when the output frequency is too low. When the output waveform has been shut down, the PLL circuit reacts by "kicking" the output frequency to a higher value; this forces the I.F. to a higher frequency within the range of the divider circuit. After the I.F. has been forced higher, the "kicker" circuit again allows the output frequency to reach the PLL.

U16, 17, 18, 19 and 20 provide drive for the REFerence COUPLER and the REFerence SWITCH filters. U18 B signal is used to switch the downconverter coupler port.

U15 is a decoder which provides decoding of chip selects. U13 and U14 are buffers required for interfacing with the computer bus.

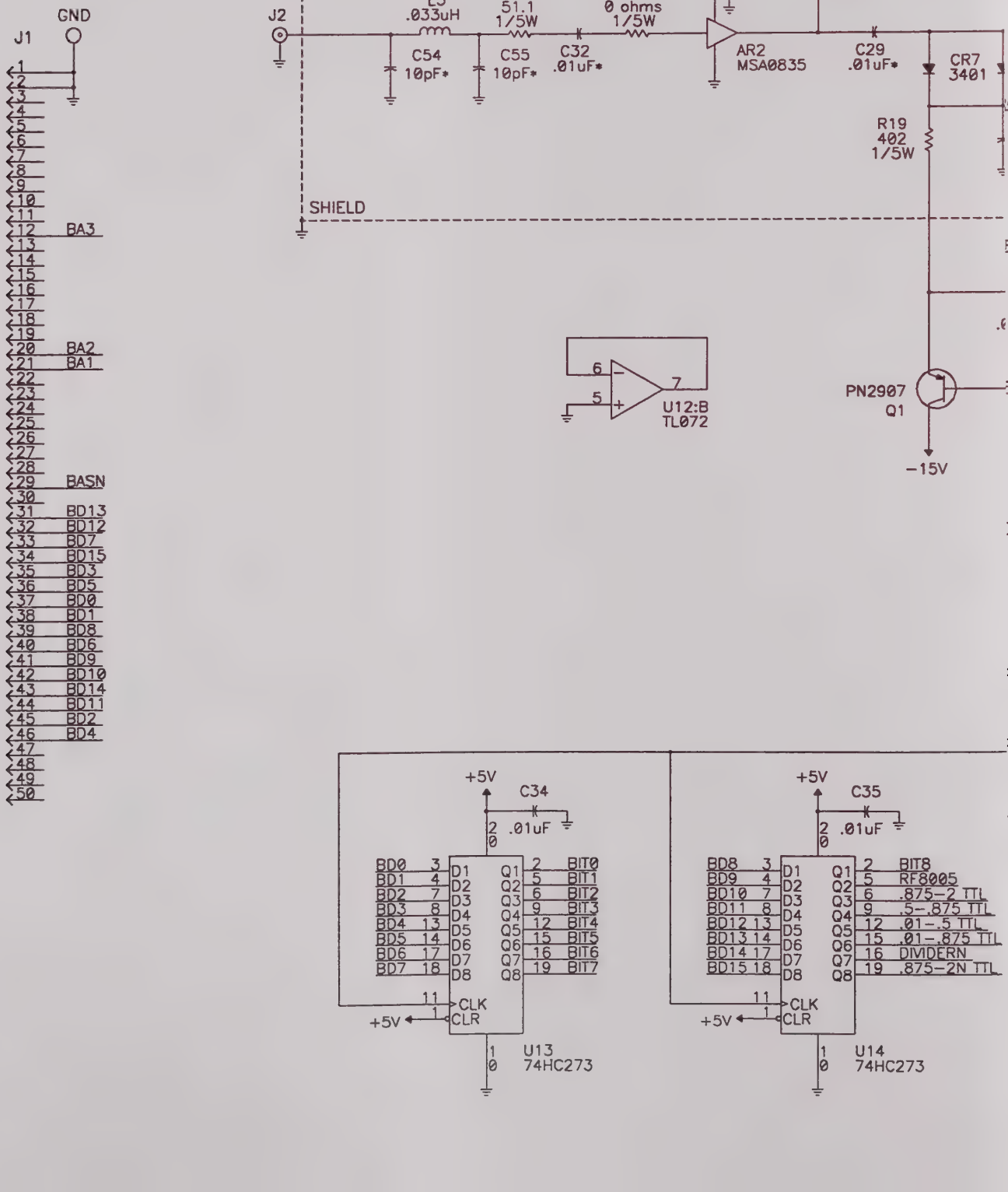

BIT8
BIT7
BIT6
BIT5
BIT4
BIT3
BIT2
BIT1
BIT0
+5V
-5.2V
U1:A MC10124
U1:B MC10124
U2:A MC10124
U2:B MC10124
U2:C MC10124
U2:D MC10124
U3:A MC10124
U3:B MC10124
U3:C MC10124
U3:D MC10124
U4:A MC10102
U4:B MC10102
U4:C MC10102
U4:D MC10102
U1:C MC10124
U1:D MC10124
C16 .01uF
C15 .01uF
C14 .01uF
C53 .01uF
C51 .01uF
C50 .01uF
C9 .01uF
C8 .01uF
U6 MC10136
U5 MC10136
CIN
COUT
S1
S2
D3
D2
D1
D0
Q3
Q2
Q1
Q0
RM1:F 560
RM1:G 560
RM1:E 560
RM1:D 560
RM2:G 560
RM2:F 560
RM2:A 560
RM4:E 560
RM4:G 560
RM4:F 560
RM4:D 560
RM5:D 560
RM5:F 560
RM5:E 560
RM5:C 560
RM6:A 560
RM3:D 560
RM6:C 560
RM6:B 560
RM6:D 560
RM6:F 560
RM6:G 560
RM6:E 560

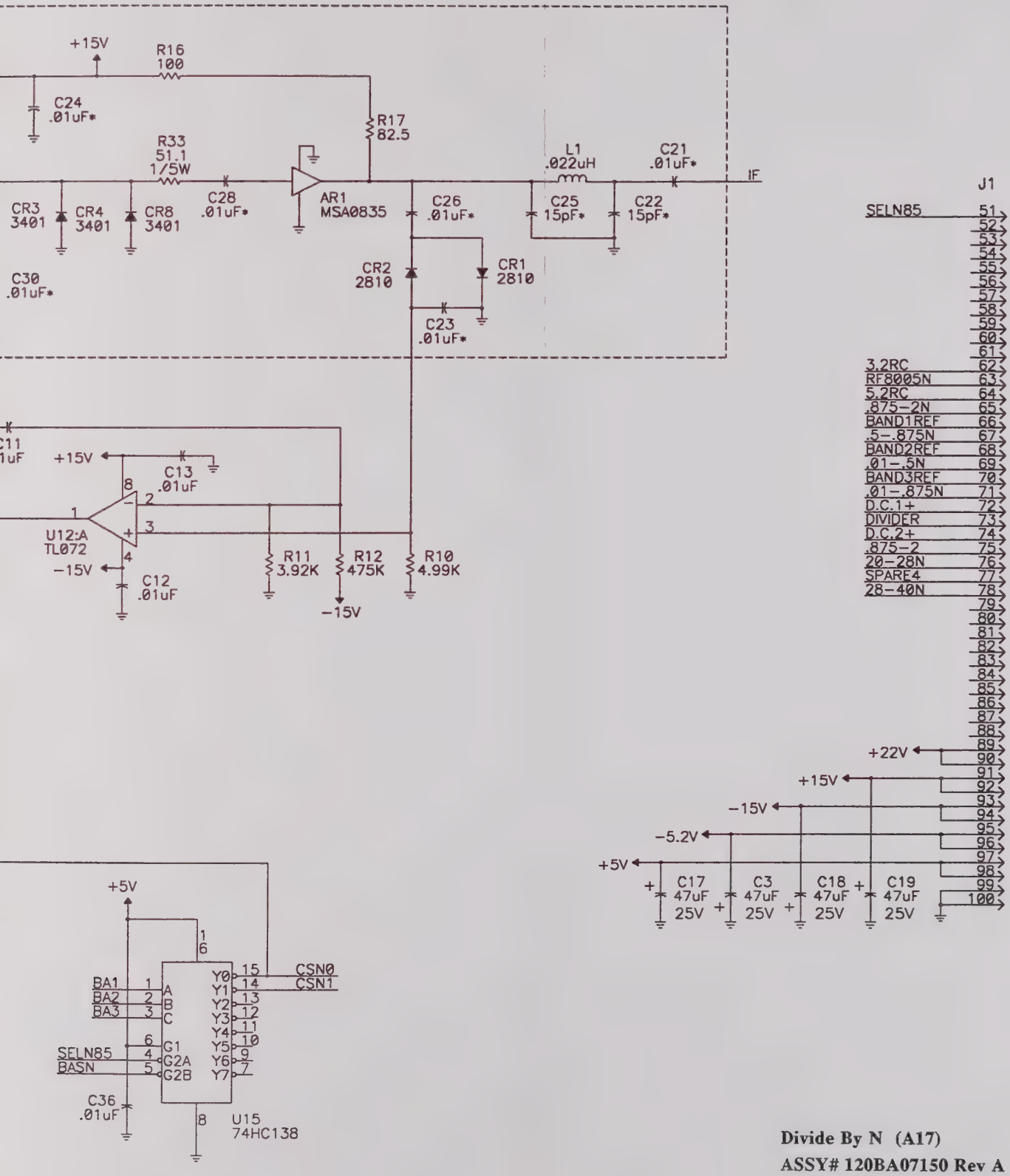



NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPACITOR VALUES ARE IN uF
2. RESISTOR VALUES ARE IN OHMS
3. RESISTORS ARE 1/4W, 1%
4. * INDICATES CHIP CAPACITOR

**Divide By N (A17)**
**ASSY# 120BA07150 Rev A**
**Sheet 3 of 5**
**7-A17-3**


GND
J1
1
2
3
4
5
6
7
8
9
10
11
12 BA3
13
14
15
16
17
18
19
20 BA2
21 BA1
22
23
24
25
26
27
28
29 BASN
30
31 BD13
32 BD12
33 BD7
34 BD15
35 BD3
36 BD5
37 BD0
38 BD1
39 BD8
40 BD6
41 BD9
42 BD10
43 BD14
44 BD11
45 BD2
46 BD4
47
48
49
50
J2
L3
.033uH
R21
51.1
1/5W
R32
0 ohms
1/5W
C54
10pF*
C55
10pF*
C32
.01uF*
AR2
MSA0835
R18
402
1/5W
C29
.01uF*
L2
22uH
C27
.01uF*
CR7
3401
R19
402
1/5W
SHIELD
6
5
7
U12:B
TL072
PN2907
Q1
-15V
+5V
C34
.01uF
BD0 3
BD1 4
BD2 7
BD3 8
BD4 13
BD5 14
BD6 17
BD7 18
D1 Q1 2 BIT0
D2 Q2 5 BIT1
D3 Q3 6 BIT2
D4 Q4 9 BIT3
D5 Q5 12 BIT4
D6 Q6 15 BIT5
D7 Q7 16 BIT6
D8 Q8 19 BIT7
11 CLK
1 CLR
+5V
U13
74HC273
+5V
C35
.01uF
BD8 3
BD9 4
BD10 7
BD11 8
BD12 13
BD13 14
BD14 17
BD15 18
D1 Q1 2 BIT8
D2 Q2 5 RF8005
D3 Q3 6 .875-2 TTL
D4 Q4 9 .5-.875 TTL
D5 Q5 12 .01-.5 TTL
D6 Q6 15 .01-.875 TTL
D7 Q7 16 DIVDERN
D8 Q8 19 .875-2N TTL
11 CLK
1 CLR
+5V
U14
74HC273

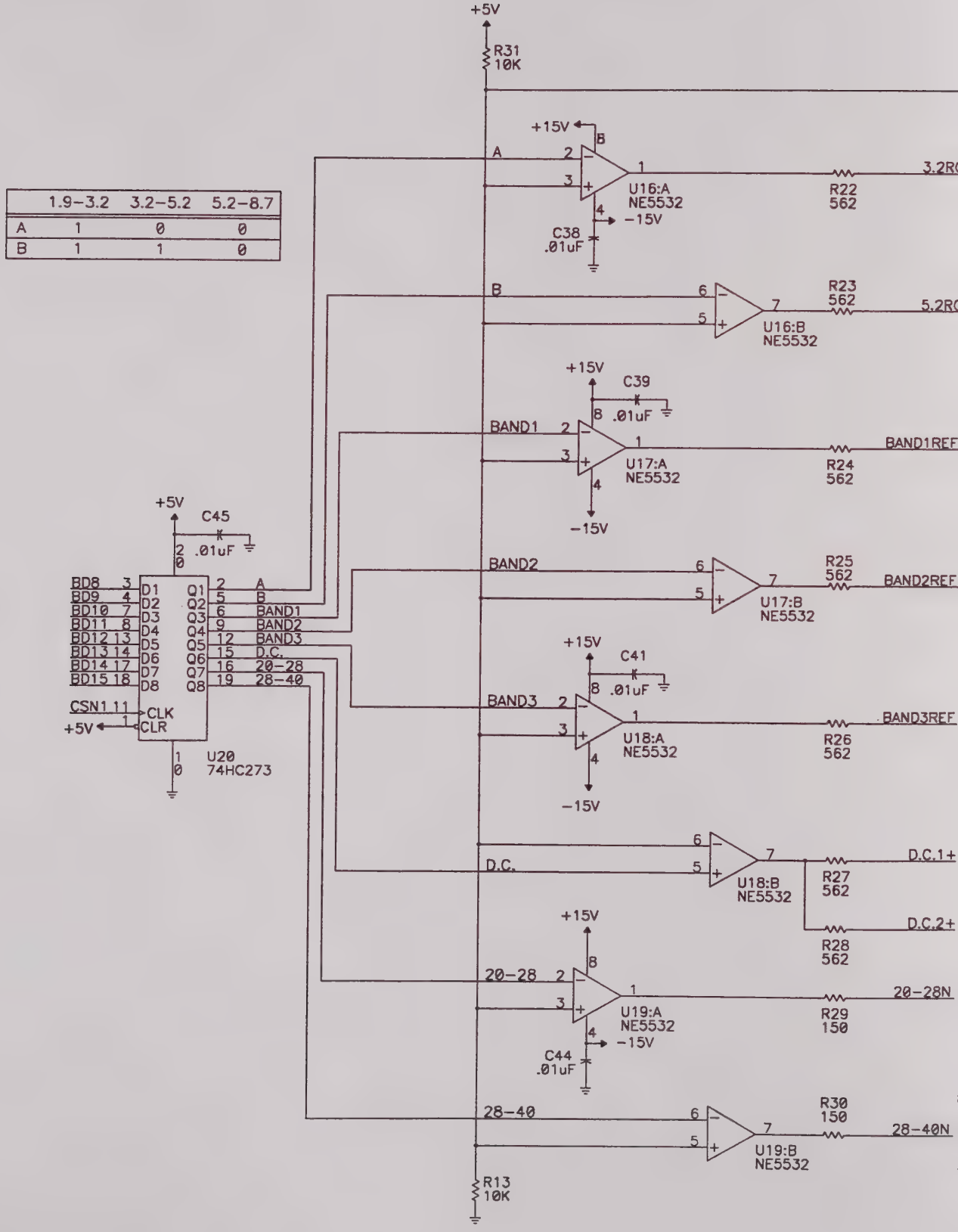


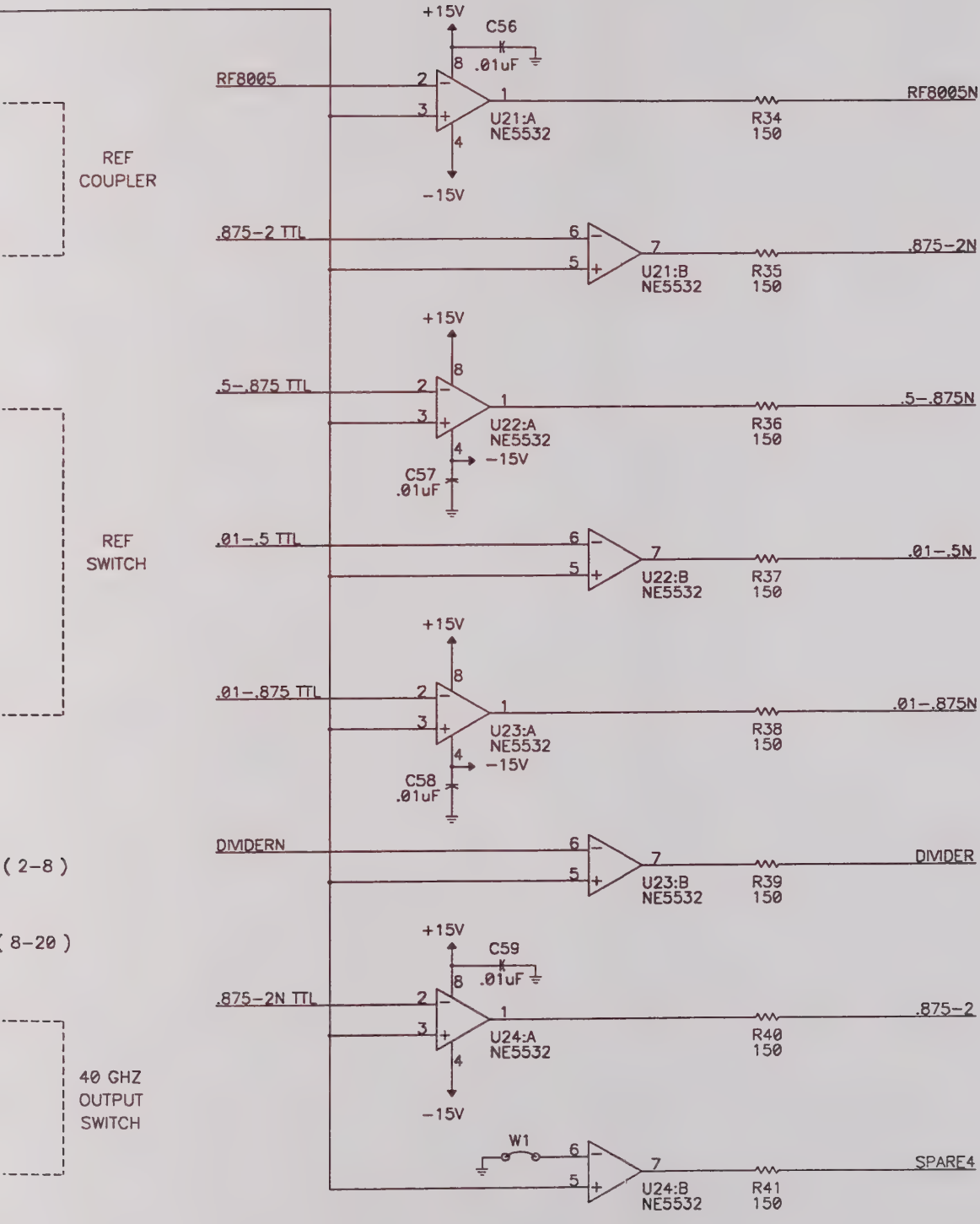

**Divide By N (A17)**

**ASSY# 120BA07150 Rev A**

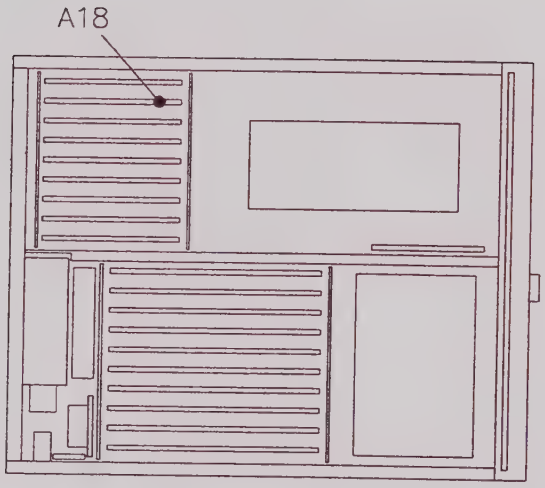
**Sheet 4 of 5**

**7-A17-4**

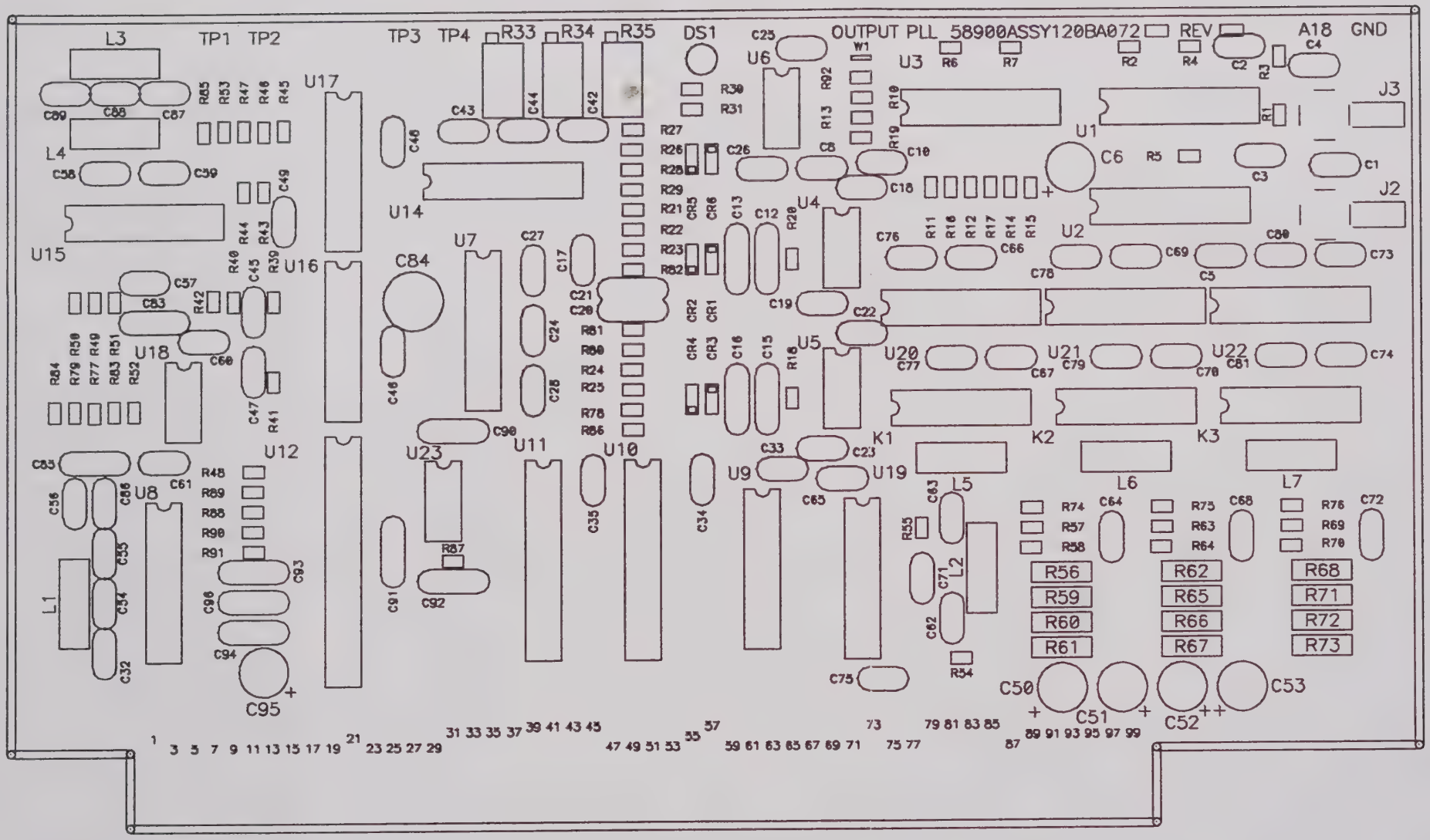

1.9–3.2 3.2–5.2 5.2–8.7
A 1 0 0
B 1 1 0
+5V
R31
10K
+15V
B
A
U16:A
NE5532
−15V
C38
.01uF
R22
562
3.2R
B
U16:B
NE5532
R23
562
5.2R
+15V
C39
.01uF
BAND1
U17:A
NE5532
−15V
BAND1REF
R24
562
+5V
C45
.01uF
BAND2
U17:B
NE5532
R25
562
BAND2REF
BD8 BD9 BD10 BD11 BD12 BD13 BD14 BD15
D1 D2 D3 D4 D5 D6 D7 D8
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8
A B BAND1 BAND2 BAND3 D.C. 20–28 28–40
CSN1
CLK
CLR
+5V
U20
74HC273
+15V
C41
.01uF
BAND3
U18:A
NE5532
−15V
BAND3REF
R26
562
D.C.
U18:B
NE5532
R27
562
D.C.1+
R28
562
D.C.2+
+15V
20–28
U19:A
NE5532
−15V
C44
.01uF
R29
150
20–28N
28–40
U19:B
NE5532
R30
150
28–40N
R13
10K




**Divide By N (A17)**
**ASSY# 120BA07150 Rev A**
**Sheet 5 of 5**
**7-A17-5**




**Output PLL (A18)**
**ASSY# 120BA07215 Rev A**
**Sheet 1 of 5**
**7-A18-1**




**OUTPUT PHASE LOCK LOOP -- PC ASSY A18**

This circuit compares the output of the divide-by-N circuit (A17) to a timebase-related reference signal and fine-tunes the output YIG oscillator in order to stabilize the divide-by-N output at 1 MHz.

The 10 MHz timebase input (J3) is buffered by U1 and then applied to U3, a frequency divider with a divisor of 10. The 1 MHz output of U3 is the reference input to the phase detector U2-6. The variable input at U2-9 is the output of the divide-by-N circuit (J2), buffered by U1, which will be at 1 MHz when the loop is locked, thus giving the correct RF output frequency. If the two inputs to the phase detector are not in phase, wide pulses are produced at either U2-12 or U2-3, depending on whether the variable input is leading or lagging the reference. The loop amplifier/filter circuit U4 A and B averages these pulses in order to produce a fine-tuning signal for the output YIG oscillator. The object is to adjust the oscillator frequency in the direction that will reduce the phase difference between the inputs to the phase detector U2.

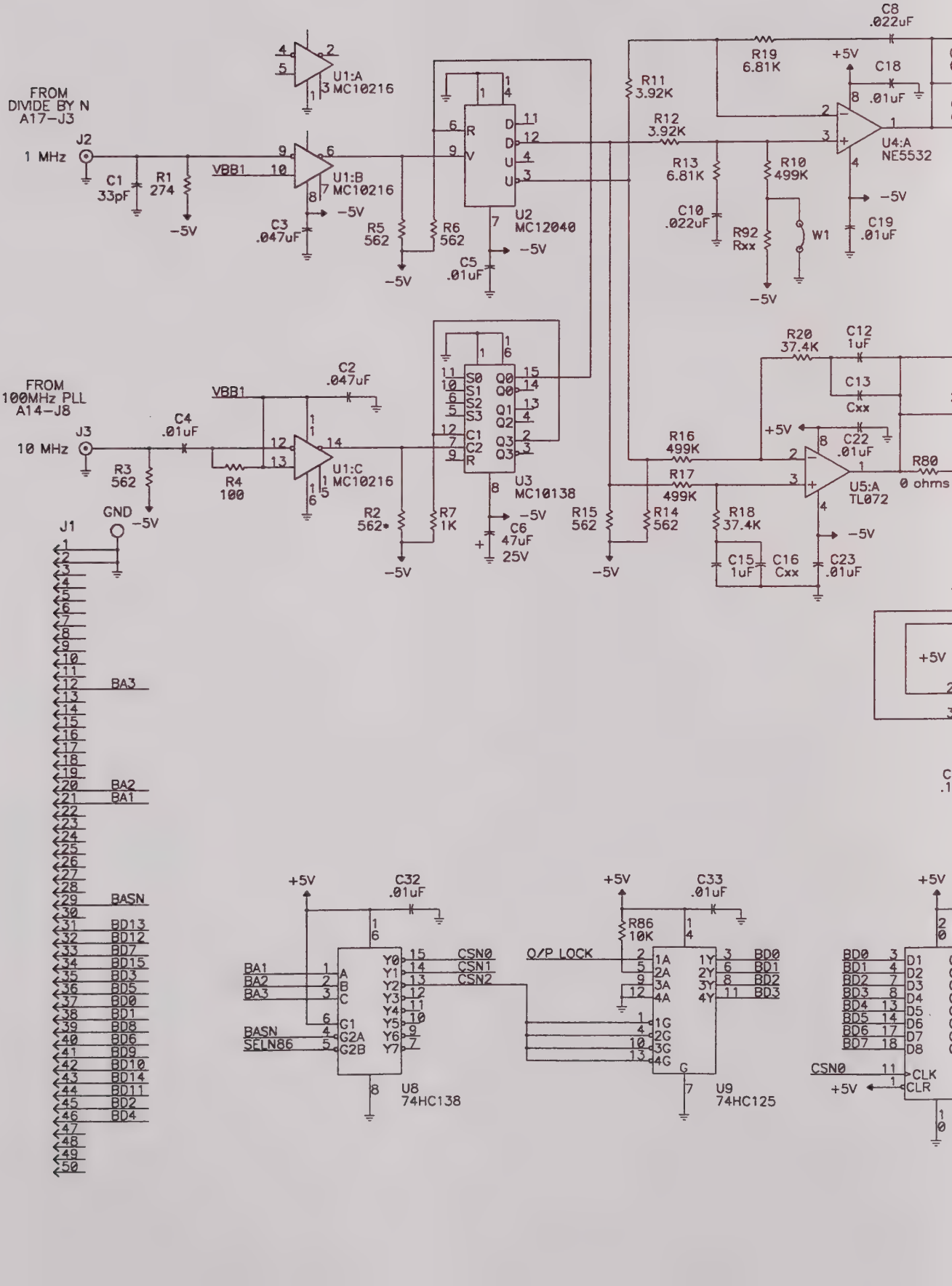
In CW mode the output of the amplifier/filter U4 A and B is applied via analog switches U7 A and B to a low pass filter (C54-56 & L1), required to filter out the 1 MHz reference frequency. The output of the filter is then applied to U18 B, an amplifier with variable AC gain used to compensate for loop gain changes due to a changing divisor for the divide-by-N. R83 and R84 provide AC attenuation. The PLL voltage is buffered by U18 A before being applied to one of three summing junctions. Analog switches U19 A & B select one of 3 circuits, U20, U21, or U22, which drive the FM tuning coils of the output YIG oscillators for each frequency band.

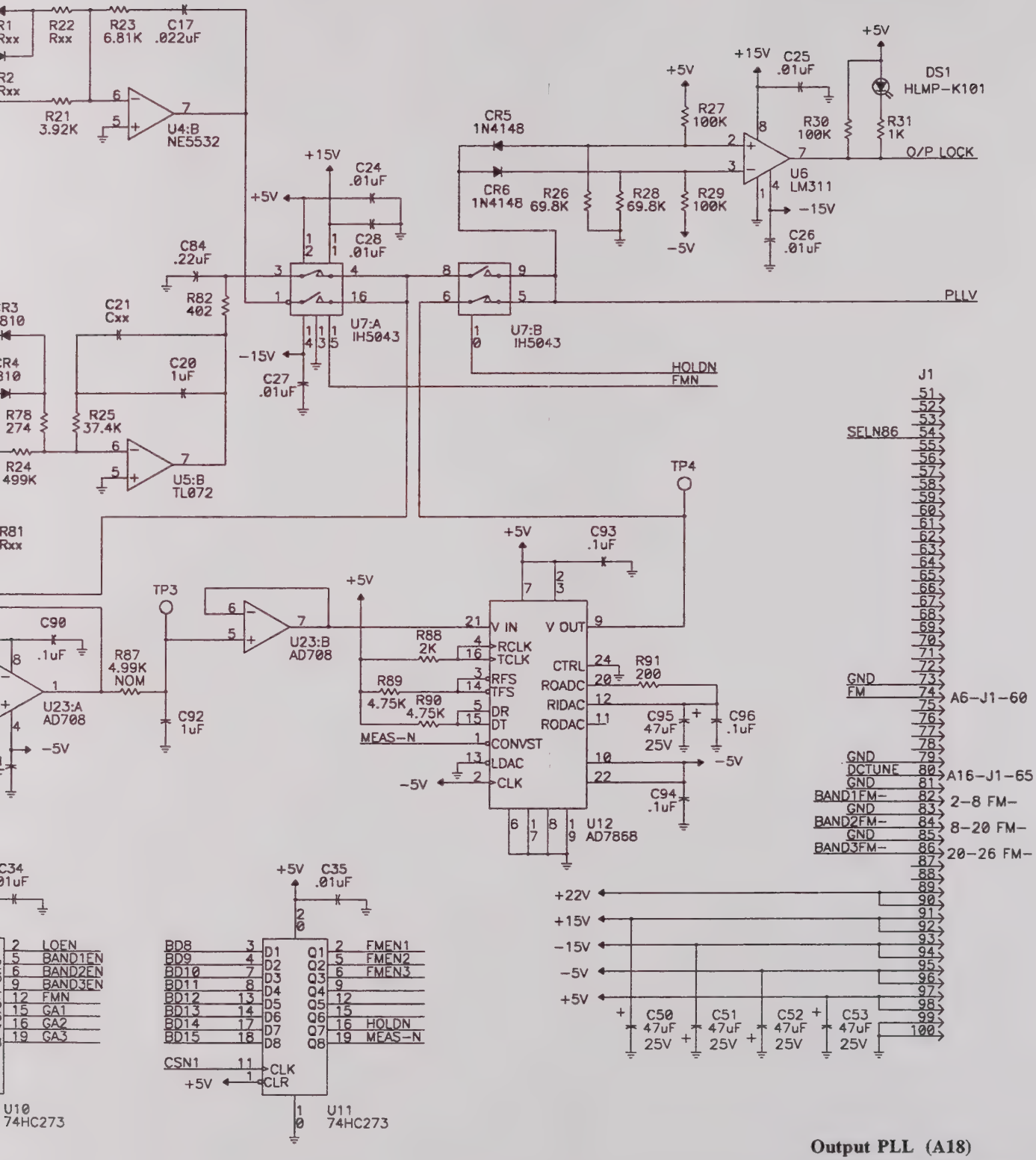
U6 is a lock detector circuit which detects when the loop voltage goes beyond a given window, thus indicating that the loop is unlocked. This circuit pulls the output lock signal low, causing the lock LED DS1 to light. When the loop voltage is within the window the loop is locked, the OUTPUTLOCK logic line is high and the lock LED on the PC board is dark.

When the FM mode is enabled an alternative loop amplifier/filter is required. In this case U5 A and B filter the output pulses of the phase detector. The outputs of both amplifier/filter circuits, U5 and U4, are applied to U7, an analog switch. When the FM mode is selected the switch U7 A enables the U5 amplifier/filter. Additionally, during FM mode the modulating signal is summed in with the loop voltage at one of the 3 FM drive circuits U20, 21, 22. The modulating signal sensitivity is adjusted via R33, R34, or R35, depending on which frequency band is active. The appropriate sensitivity is selected via switch U14 A & B and the modulating signal is then amplified by U16 and U17. U19 A furnishes the PLL voltage from the fixed LO PLL PCA to the 2-8 GHz oscillator when required for downconversion of frequencies up to 2 GHz.

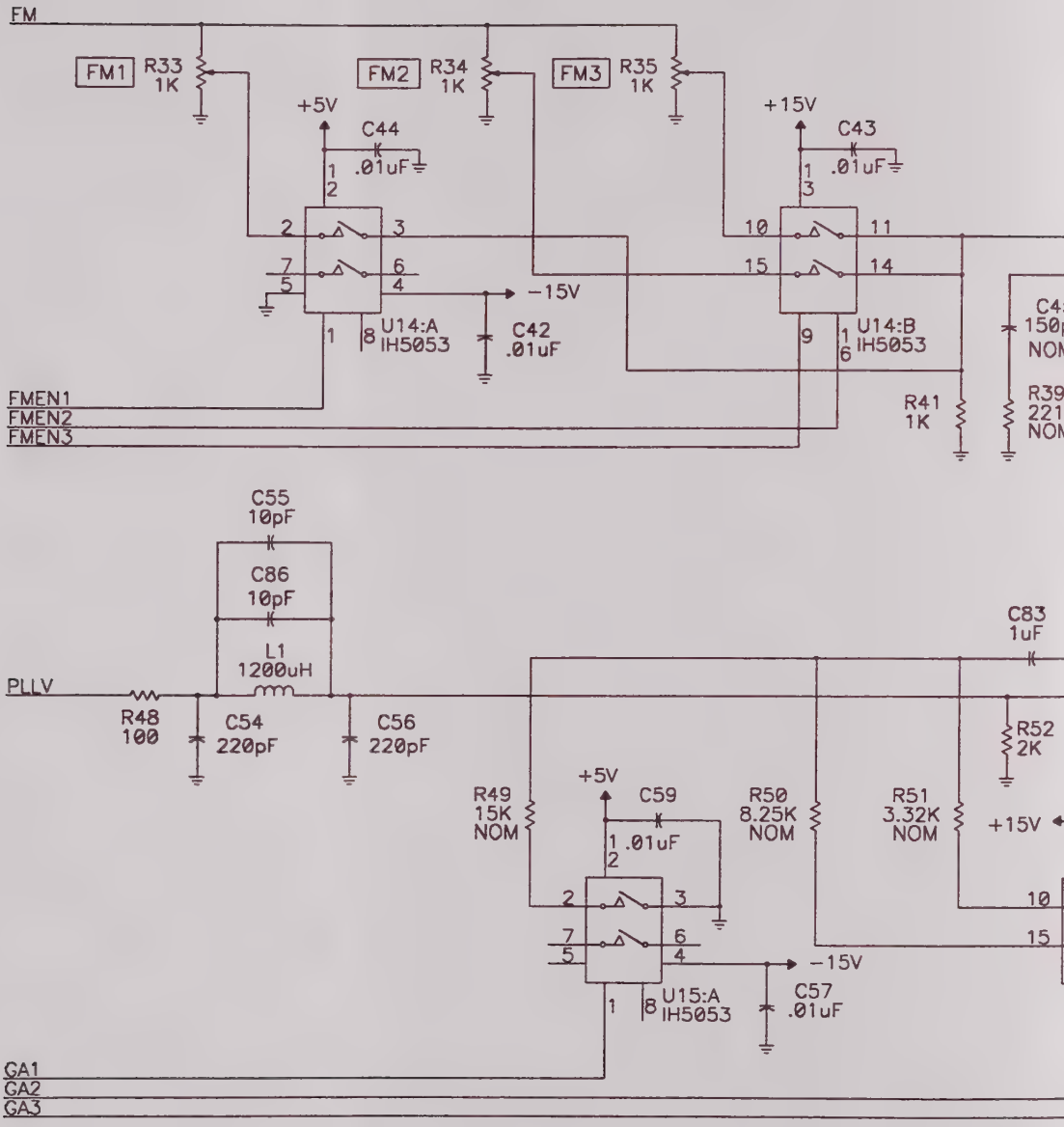
U12 operates as a sample and hold circuit during Analog Sweep operation by holding the PLL loop voltage, thereby setting the START frequency, when the analog switch U7-B receives the HOLDN low logic signal.

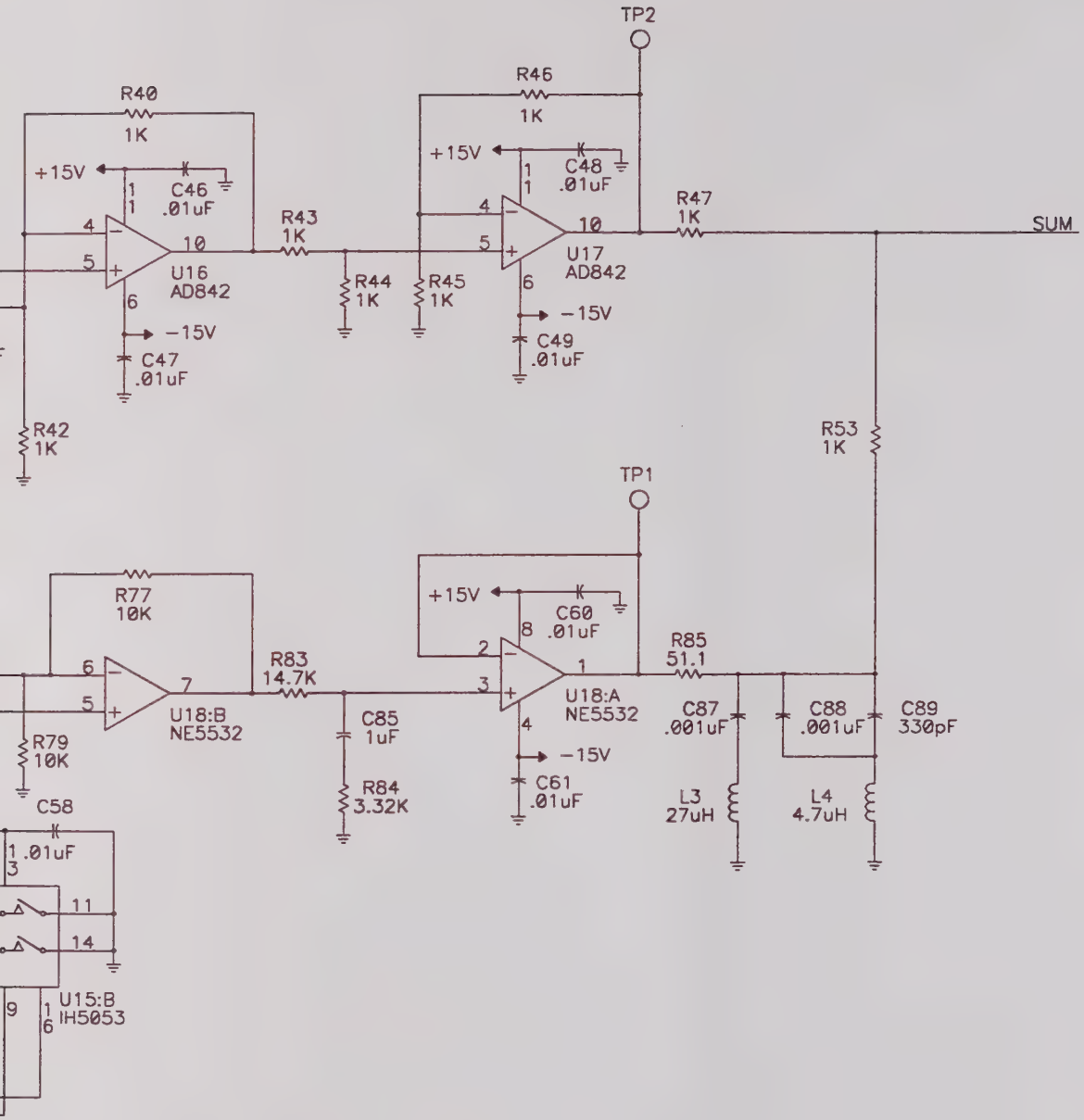
U8 provides an interface between the computer and the PCA by decoding the chip select lines. U9 buffers the output logic from the PCA so that it can be read by the computer. U10 and 11 are latches for logic input from the computer bus.


FROM DIVIDE BY N A17-J3
J2
1 MHz
C1 33pF
R1 274
-5V
VBB1
U1:A MC10216
U1:B MC10216
U1:C MC10216
C3 .047uF
R5 562
R6 562
C5 .01uF
U2 MC12040
R11 3.92K
R12 3.92K
R19 6.81K
C8 .022uF
+5V
C18 .01uF
U4:A NE5532
R13 6.81K
R10 499K
C10 .022uF
R92 Rxx
W1
C19 .01uF
FROM 100MHz PLL A14-J8
J3
10 MHz
C4 .01uF
R3 562
R4 100
C2 .047uF
U3 MC10138
R2 562*
R7 1K
C6 47uF 25V
R15 562
R14 562
R16 499K
R17 499K
R18 37.4K
R20 37.4K
C12 1uF
C13 Cxx
C22 .01uF
U5:A TL072
R80 0 ohms
C15 1uF
C16 Cxx
C23 .01uF
GND
J1
BA3
BA2
BA1
BASN
BD13
BD12
BD7
BD15
BD3
BD5
BD0
BD1
BD8
BD6
BD9
BD10
BD14
BD11
BD2
BD4
C32 .01uF
BA1
BA2
BA3
BASN
SELN86
CSN0
CSN1
CSN2
U8 74HC138
C33 .01uF
R86 10K
O/P LOCK
BD0
BD1
BD2
BD3
U9 74HC125
CSN0
CLK
CLR




**Output PLL (A18)**
**ASSY# 120BA07215 Rev A**
**Sheet 3 of 5**
**7-A18-3**

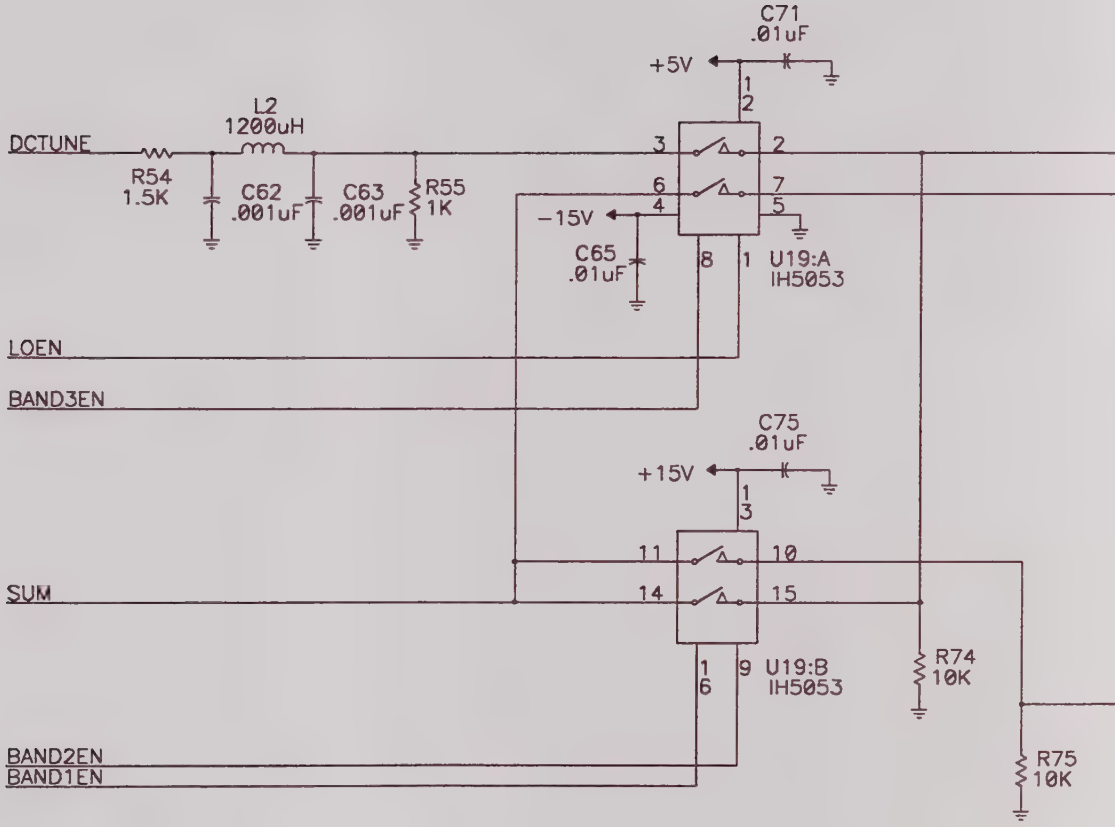

FM
FM1
R33
1K
FM2
R34
1K
FM3
R35
1K
+5V
C44
.01uF
+15V
C43
.01uF
−15V
C42
.01uF
U14:A
IH5053
U14:B
IH5053
R41
1K
FMEN1
FMEN2
FMEN3
C55
10pF
C86
10pF
L1
1200uH
PLLV
R48
100
C54
220pF
C56
220pF
C83
1uF
R52
2K
R49
15K
NOM
C59
.01uF
R50
8.25K
NOM
R51
3.32K
NOM
+15V
−15V
C57
.01uF
U15:A
IH5053
GA1
GA2
GA3

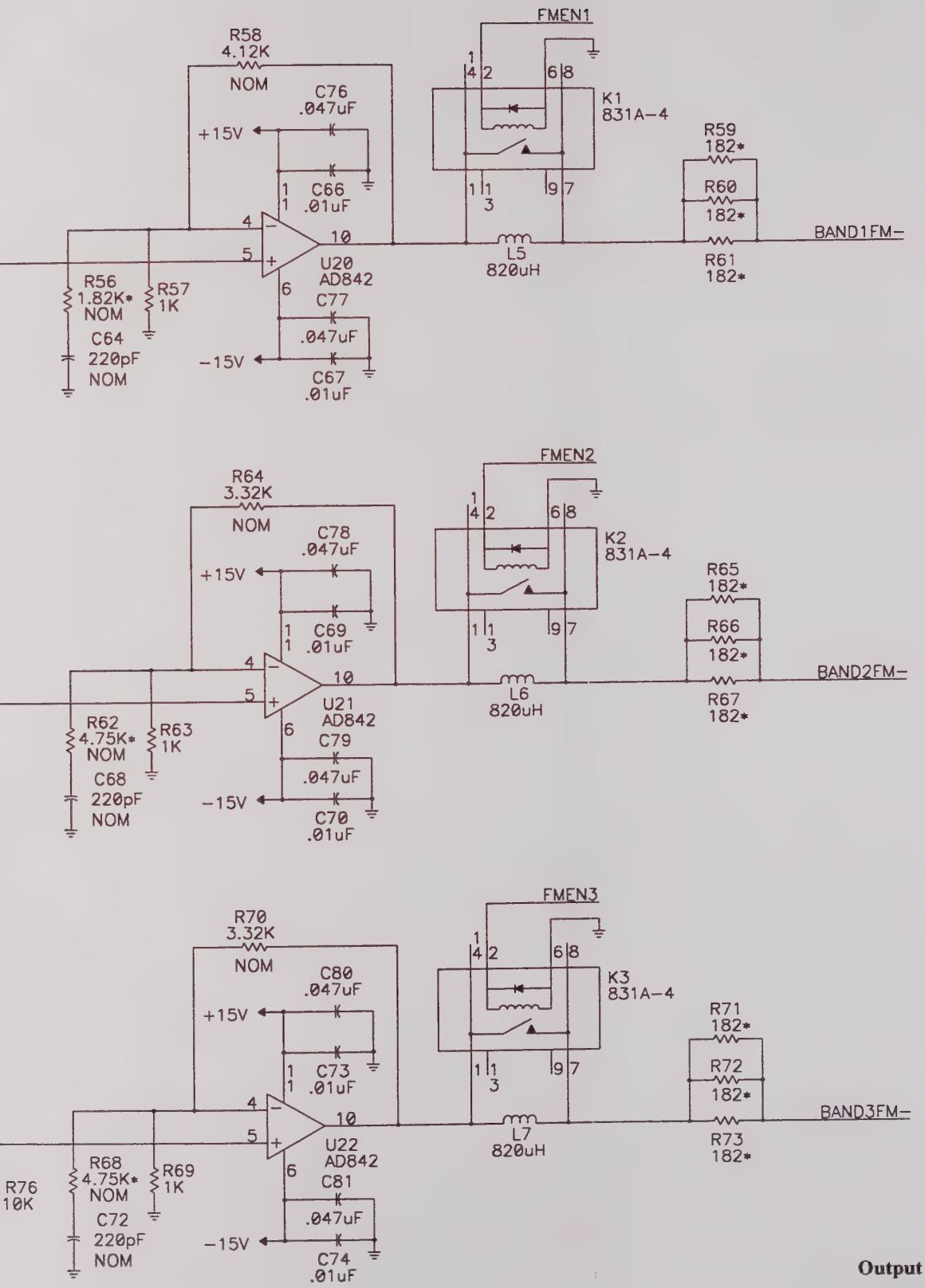



NOTES: UNLESS OTHERWISE SPECIFIED

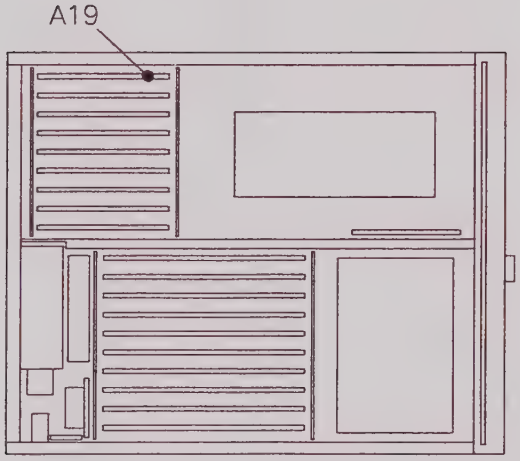
1. CAPACITOR VALUES ARE IN uF.
2. RESISTOR VALUES ARE IN OHMS.
3. RESISTORS ARE 1/5W, 1%
4. * INDICATES 1/4W, 1% RESISTORS.

**Output PLL (A18)**
**ASSY# 120BA07215 RevA**
**Sheet 4 of 5**
**7-A18-4**

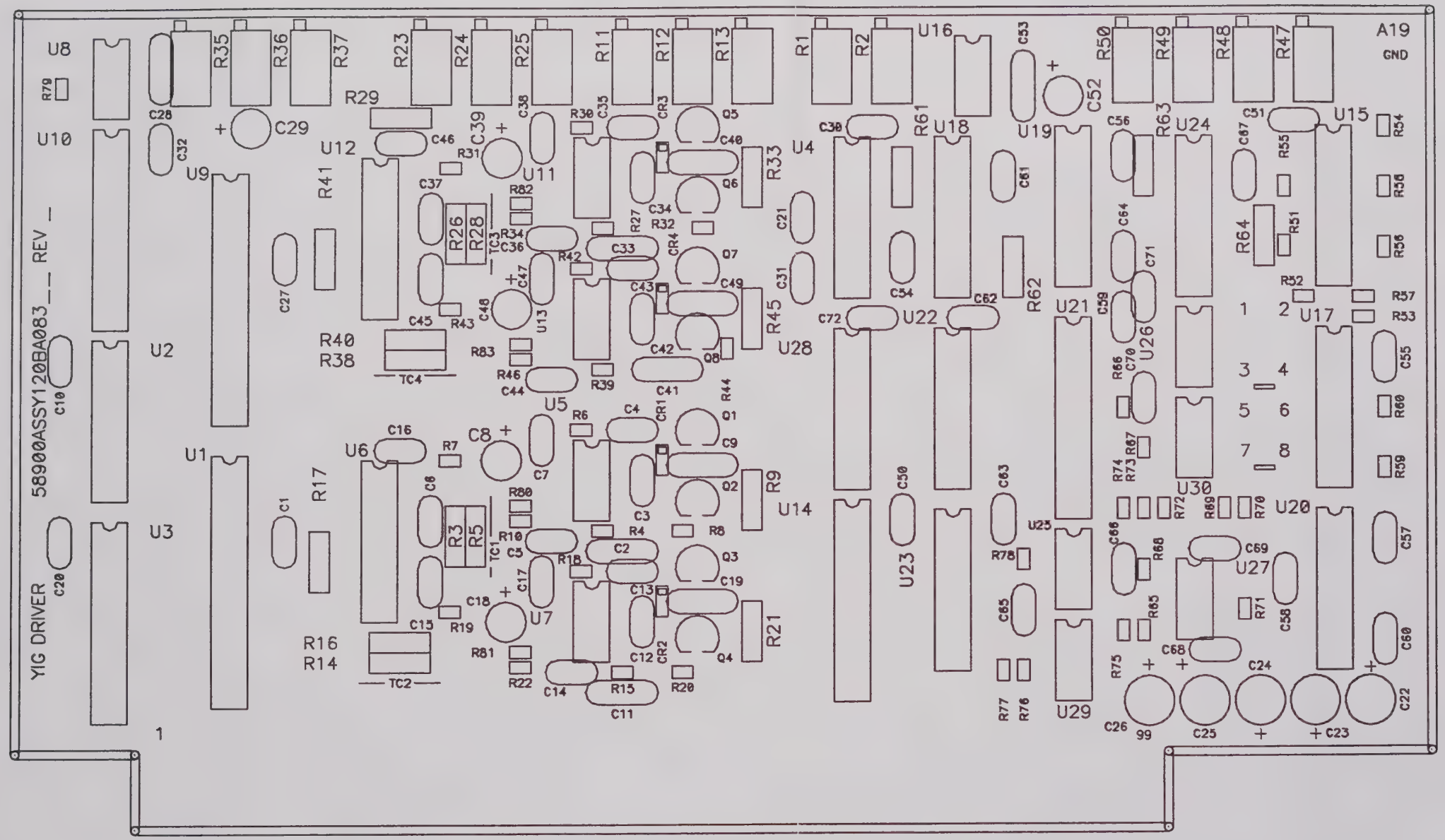

C71
.01uF
+5V
L2
1200uH
DCTUNE
R54
1.5K
C62
.001uF
C63
.001uF
R55
1K
-15V
C65
.01uF
U19:A
IH5053
LOEN
BAND3EN
C75
.01uF
+15V
SUM
U19:B
IH5053
R74
10K
R75
10K
BAND2EN
BAND1EN




**Output PLL (A18)**
**ASSY# 120BA07215 Rev A**
**Sheet 5 of 5**
**7-A18-5**




**YIG Driver (A19)**
**ASSY# 120BA08300 Rev J**
**Sheet 1 of 5**
**7-A19-1**




**YIG DRIVER – PC ASSY A19**

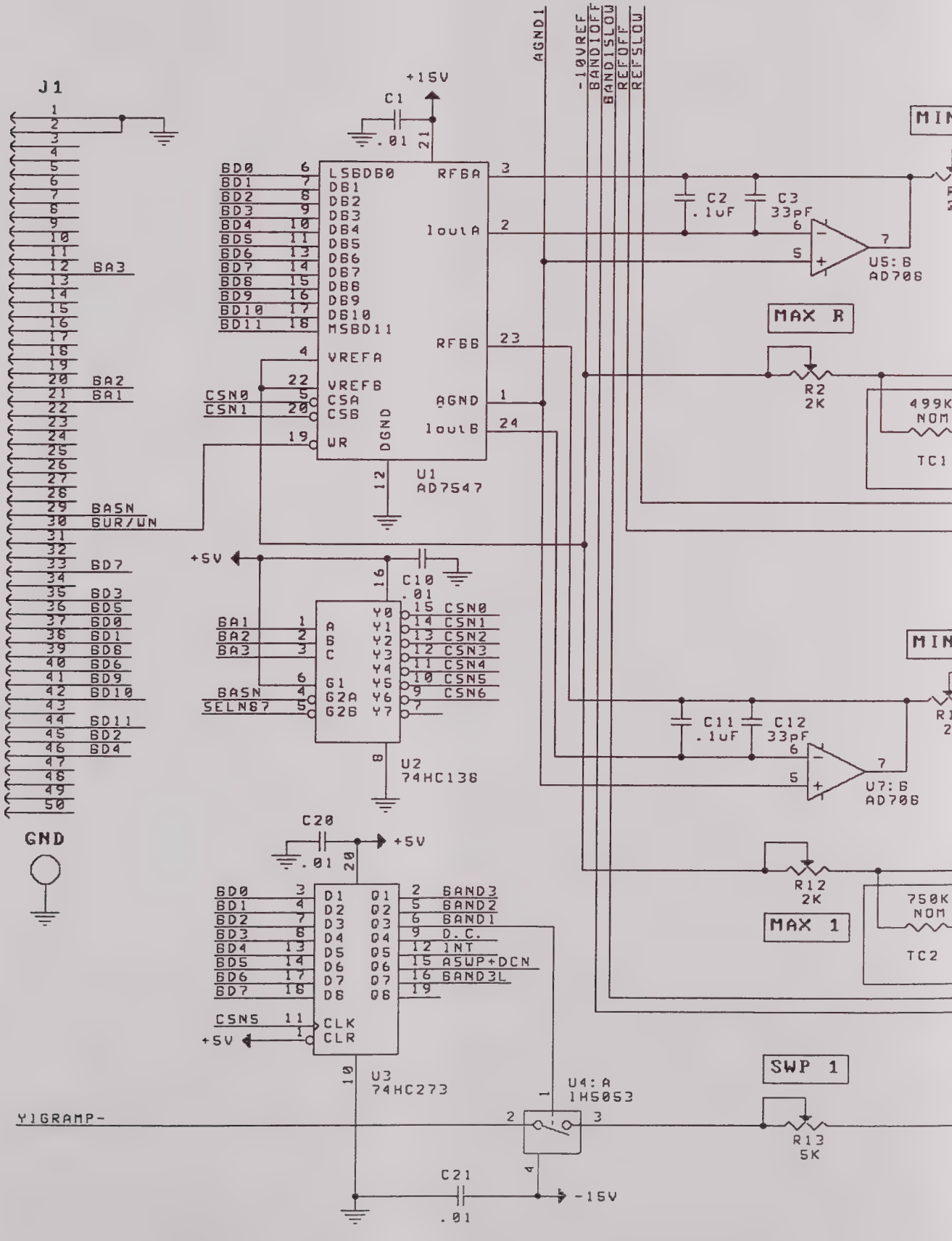
The YIG Driver PCA consists of 4 YIG driver circuits, one for each of the frequency bands (2-8, 8-20, 20-26 GHz and the Reference oscillator). In addition, this board holds the circuitry which generates the logic for different frequency bands, and for switching filters in RF modules. It also generates logic used during sweep.

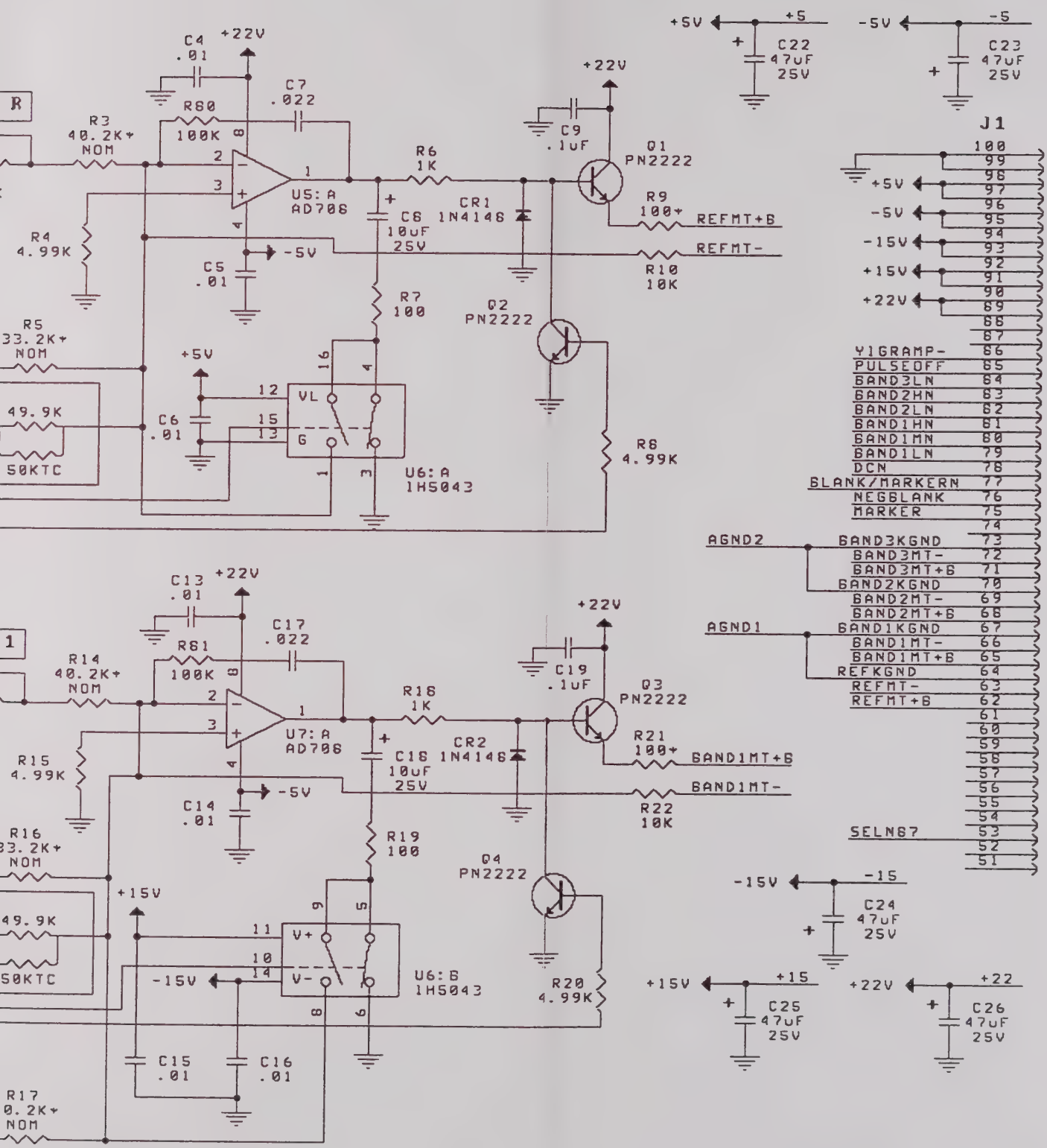
The YIG driver circuit for BAND1 consists of DAC U1 section B whose output is converted to voltage by U7 B. MIN 1 pot (R11) is used for adjusting the voltage to the YIG when at the minimum frequency in band 1. The reference voltage is also summed in at U7-2 thru MAX 1 pot (R12) which is used to adjust the voltage provided to the YIG when at the maximum frequency in band 1. At the output of U7 A there is a filter which can be switched in by U6 B when the Unit is in CW or 'SLOW' mode, ie, when the Unit is not sweeping or changing frequency. This filter is disabled, when the unit is sweeping or changing frequency, allowing the YIG voltage to change rapidly. This switched filter is known as the 'Fast/Slow' circuitry. When analog sweep is activated U4 A is switched allowing a ramp voltage to be summed into the amplifier U7 to sweep the YIG thru the specified band. Q4 is required to turn off the tuning voltage to the YIG when the band is not selected. Q3 provides the drive for the Main tune coil of the YIG.

This circuit is repeated for each of the bands. The only difference is that in the reference band there is not a ramp voltage summed in during analog sweep.

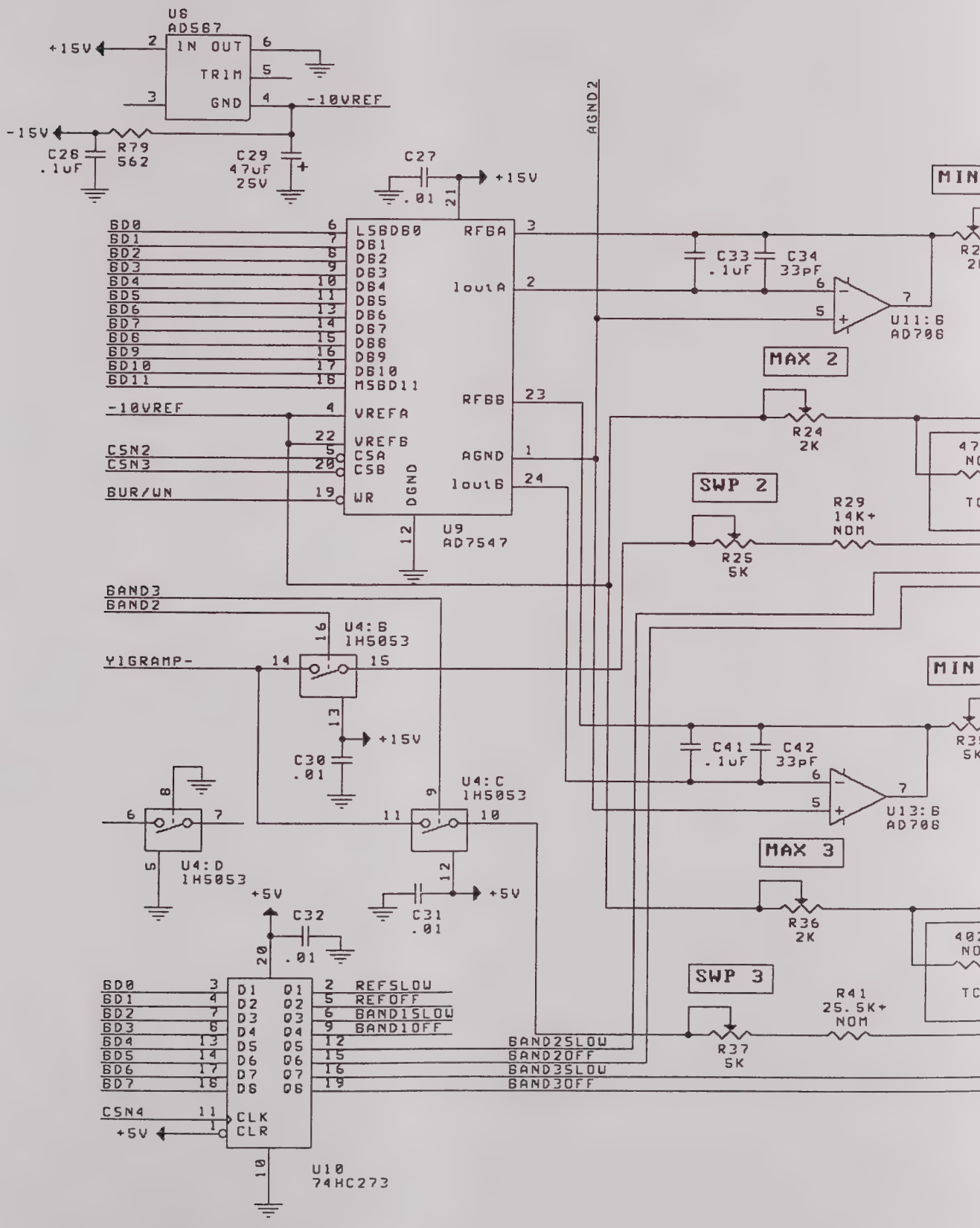
Filter switching logic and sweep logic signals are also generated on A19. When the unit is not in analog sweep U21 is cleared thereby enabling U22 and U23 to propagate the logic latched by U14 from the computer bus. These outputs drive U25 and U26 which drive the filter switches for the output switch module. When the unit is in analog sweep, the computer cannot provide the logic signals at the appropriate times therefore another method is used to detect when to switch the filters. For example, in band 1 this method involves sampling the main tuning voltage and using a comparator U15 C to detect when the main tune voltage reaches a voltage set by the 5.2 pot (R49). This 5.2 reference voltage can be adjusted to insure that the comparator output switches when the frequency is at 5.2 GHz. The output then propagates thru to U21 which is enabled during analog sweep. The remaining logic along with flip flops U18, U19 and U24 work in conjunction to supply the remaining filter logic and blanking signals required during analog sweep.

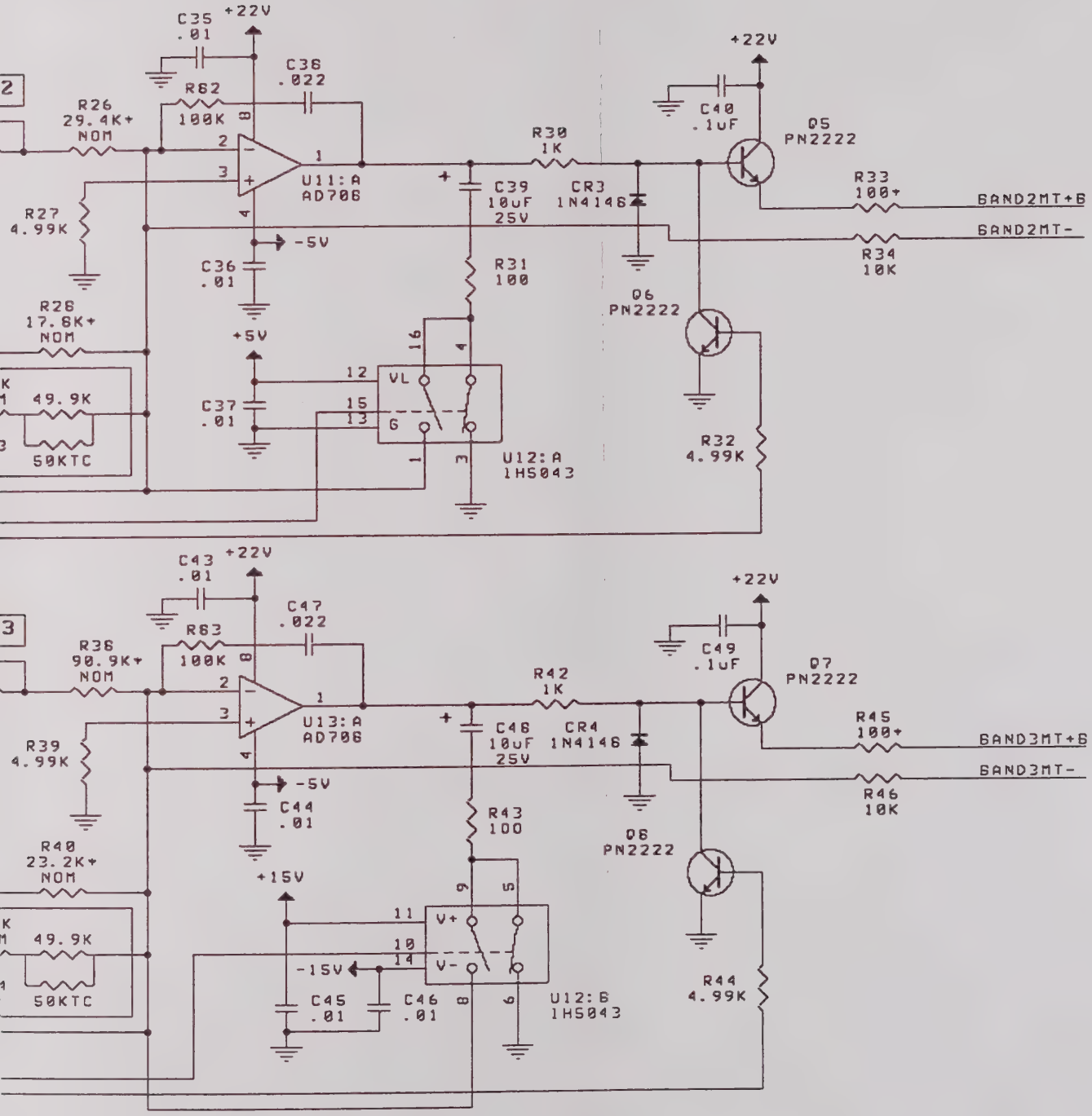
Decoder U2 decodes the chip select lines for circuits on this PC board. U3, U10 and U14 are required for computer bus interface.


J1
GND
+15V
C1
.01
AGND1
-10VREF
BAND1OFF
BAND1SLOW
REFOFF
REFSLOW
LSBDB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DB8
DB9
DB10
MSBD11
VREFA
VREFB
CSA
CSB
WR
DGND
RFBA
IoutA
RFBB
AGND
IoutB
U1
AD7547
C2
.1uF
C3
33pF
U5:B
AD706
MAX R
R2
2K
499K
NOM
TC1
+5V
C10
.01
U2
74HC138
C11
.1uF
C12
33pF
U7:B
AD706
R12
2K
750K
NOM
TC2
MAX 1
C20
.01
U3
74HC273
U4:A
1H5053
SWP 1
R13
5K
C21
.01
-15V
Y1GRAMP-
BA1
BA2
BA3
BASN
SELN87
CSN0
CSN1
CSN2
CSN3
CSN4
CSN5
CSN6
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
BD8
BD9
BD10
BD11
BD2
BD4
BD5
BD6
BUR/WN
BAND3
BAND2
BAND1
D.C.
INT
ASWP+DCN
BAND3L
CLK
CLR

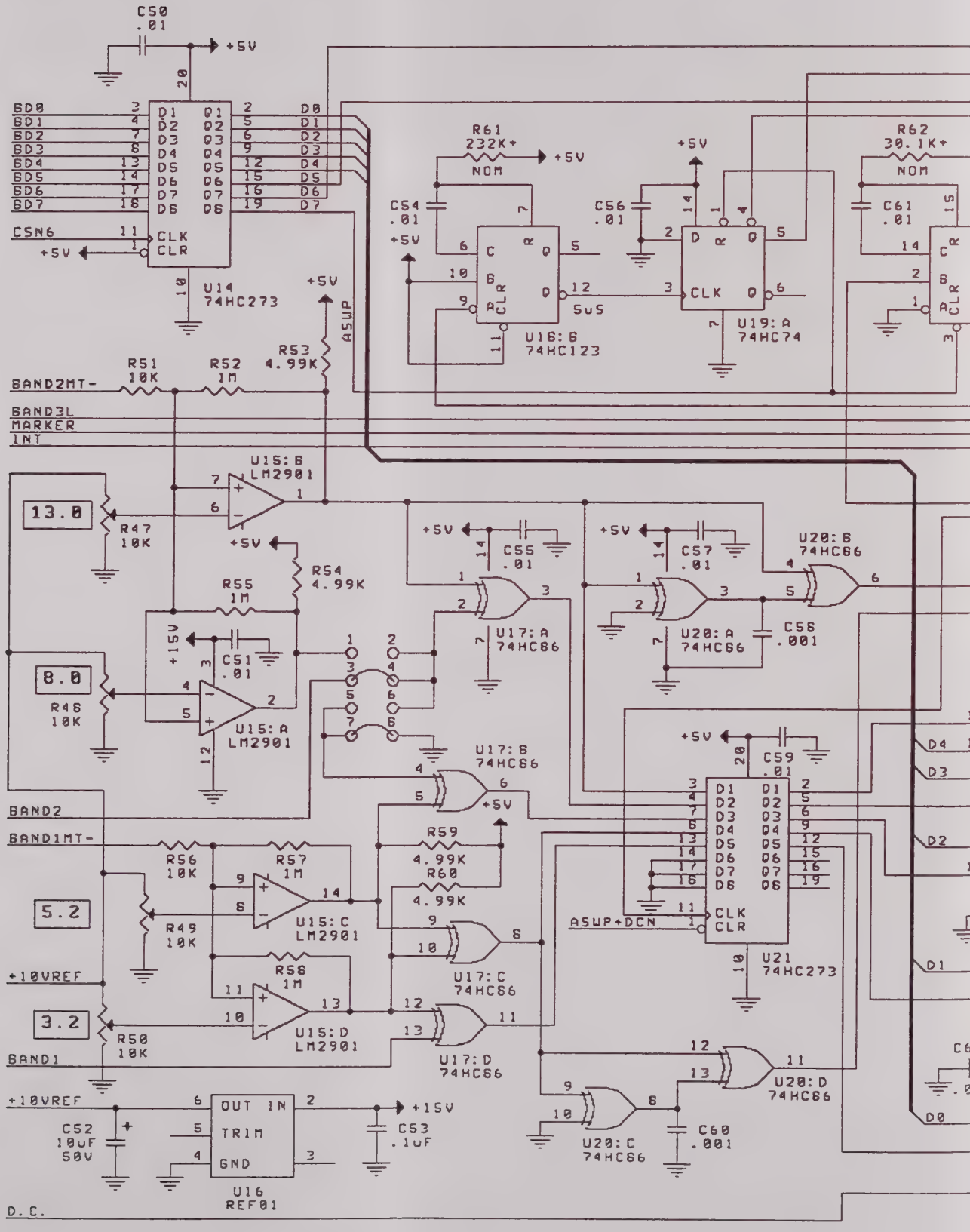


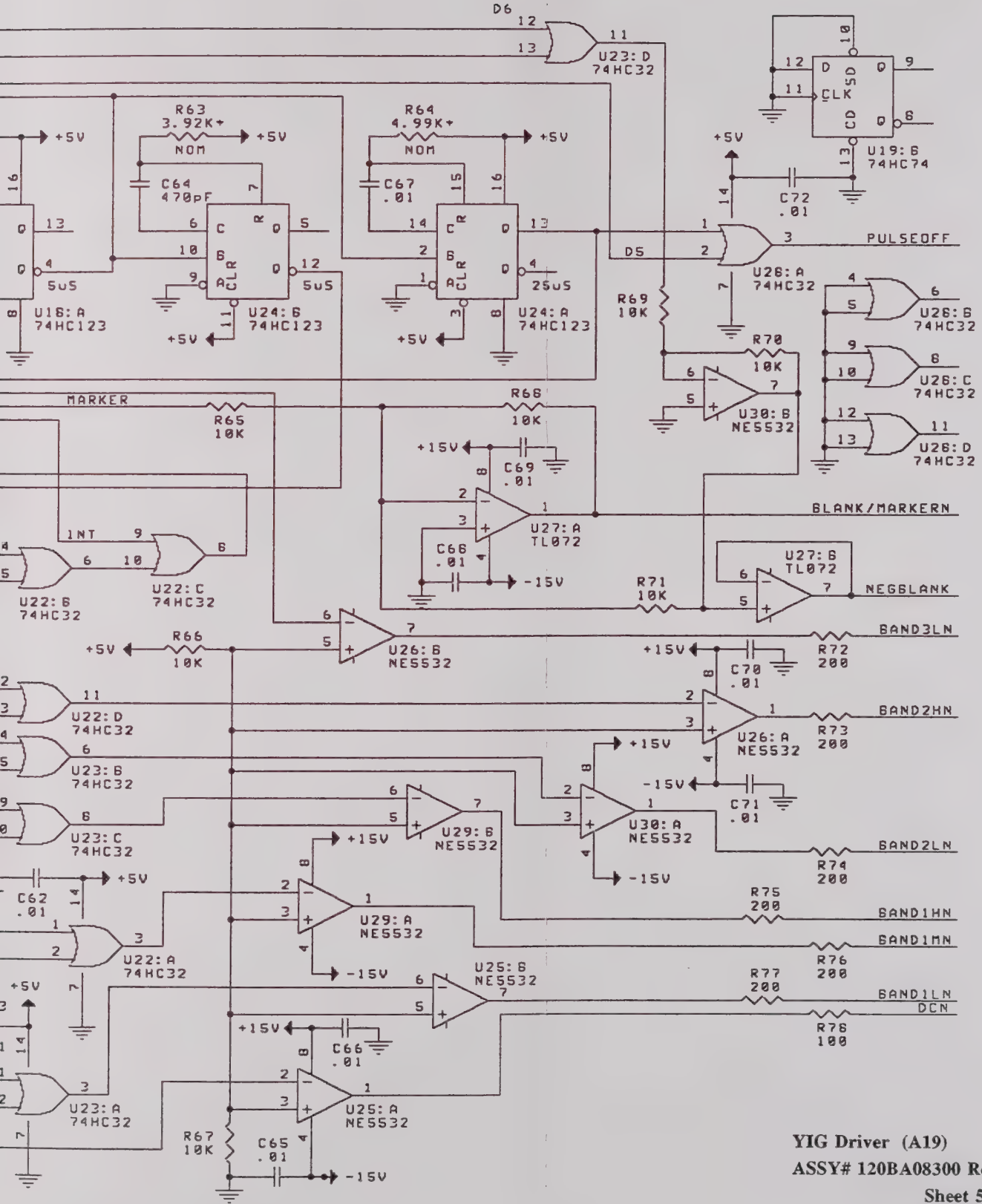

**YIG Driver (A19)**
**ASSY# 120BA08300 Rev J**
**Sheet 3 of 5**
**7-A19-3**


U8
AD587
+15V
IN
OUT
TRIM
GND
-10VREF
-15V
R79
562
C28
.1uF
C29
47uF
25V
C27
.01
+15V
AGND2
MIN
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
BD8
BD9
BD10
BD11
LSBDB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DB8
DB9
DB10
MSBD11
-10VREF
VREFA
VREFB
CSN2
CSN3
CSA
CSB
BUR/WN
WR
DGND
RFBA
IoutA
RFBB
AGND
IoutB
U9
AD7547
C33
.1uF
C34
33pF
U11:B
AD706
MAX 2
R24
2K
SWP 2
R29
14K+
NOM
R25
5K
BAND3
BAND2
U4:B
1H5053
Y1GRAMP-
C30
.01
+15V
U4:C
1H5053
U4:D
1H5053
C41
.1uF
C42
33pF
U13:B
AD706
MAX 3
R36
2K
SWP 3
R41
25.5K+
NOM
R37
5K
+5V
C32
.01
C31
.01
REFSLOW
REFOFF
BAND1SLOW
BAND1OFF
BAND2SLOW
BAND2OFF
BAND3SLOW
BAND3OFF
CSN4
CLK
CLR
U10
74HC273

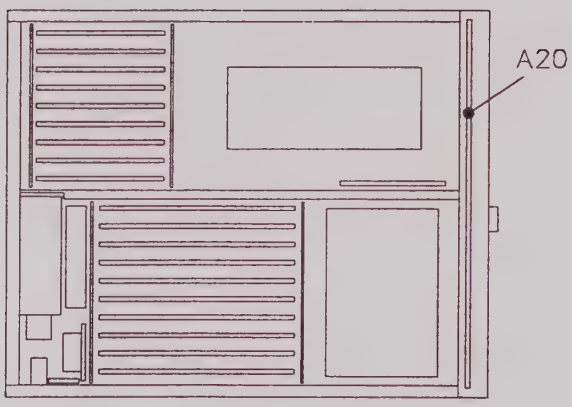



**YIG Driver (A19)**
**ASSY# 120BA08300 Rev J**
**Sheet 4 of 5**
**7-A19-4**

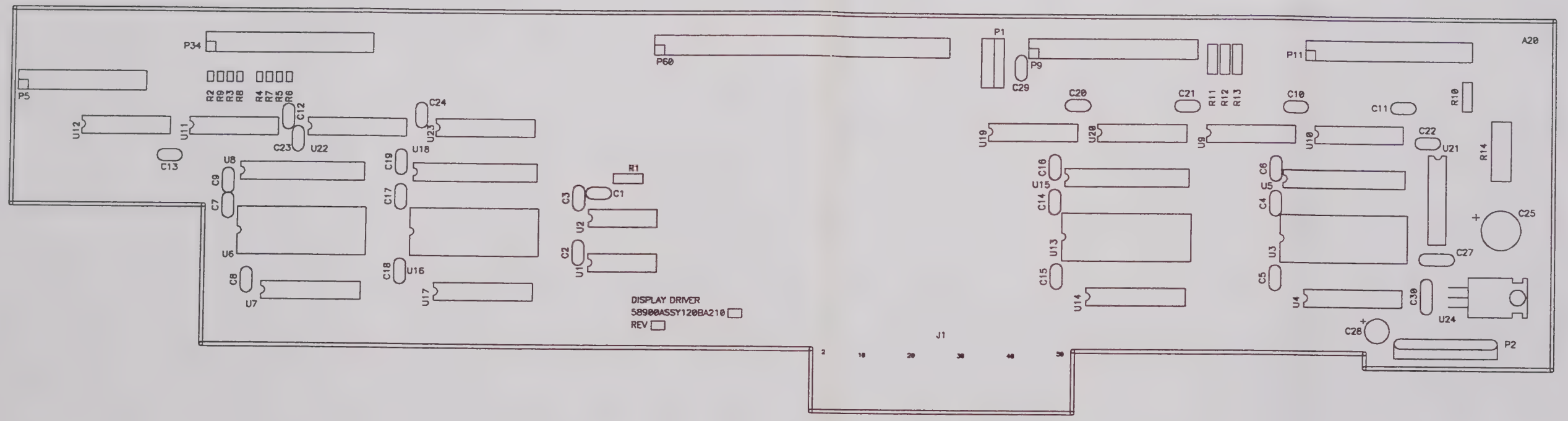

C50
.01
+5V
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
CSN6
U14
74HC273
R61
232K*
NOM
C54
.01
U18:B
74HC123
5uS
C56
.01
U19:A
74HC74
R62
30.1K*
C61
.01
R51
10K
R52
1M
R53
4.99K
ASWP
BAND2MT-
BAND3L
MARKER
INT
U15:B
LM2901
13.0
R47
10K
R54
4.99K
R55
1M
C51
.01
+15V
8.0
R46
10K
U15:A
LM2901
C55
.01
U17:A
74HC86
C57
.01
U20:B
74HC86
U20:A
74HC86
C58
.001
U17:B
74HC86
C59
.01
U21
74HC273
ASWP+DCN
BAND2
BAND1MT-
R56
10K
R57
1M
R59
4.99K
R60
4.99K
5.2
R49
10K
U15:C
LM2901
U17:C
74HC86
+10VREF
R58
1M
3.2
R50
10K
U15:D
LM2901
U17:D
74HC86
U20:D
74HC86
U20:C
74HC86
C60
.001
BAND1
C52
10uF
50V
OUT
IN
TRIM
GND
U16
REF01
C53
.1uF
D.C.
D4
D3
D2
D1
D0




**YIG Driver (A19)**
**ASSY# 120BA08300 Rev J**
**Sheet 5 of 5**
**7-A19-5**




**Display Driver (A20)**
**ASSY# 1202221000 Rev A**

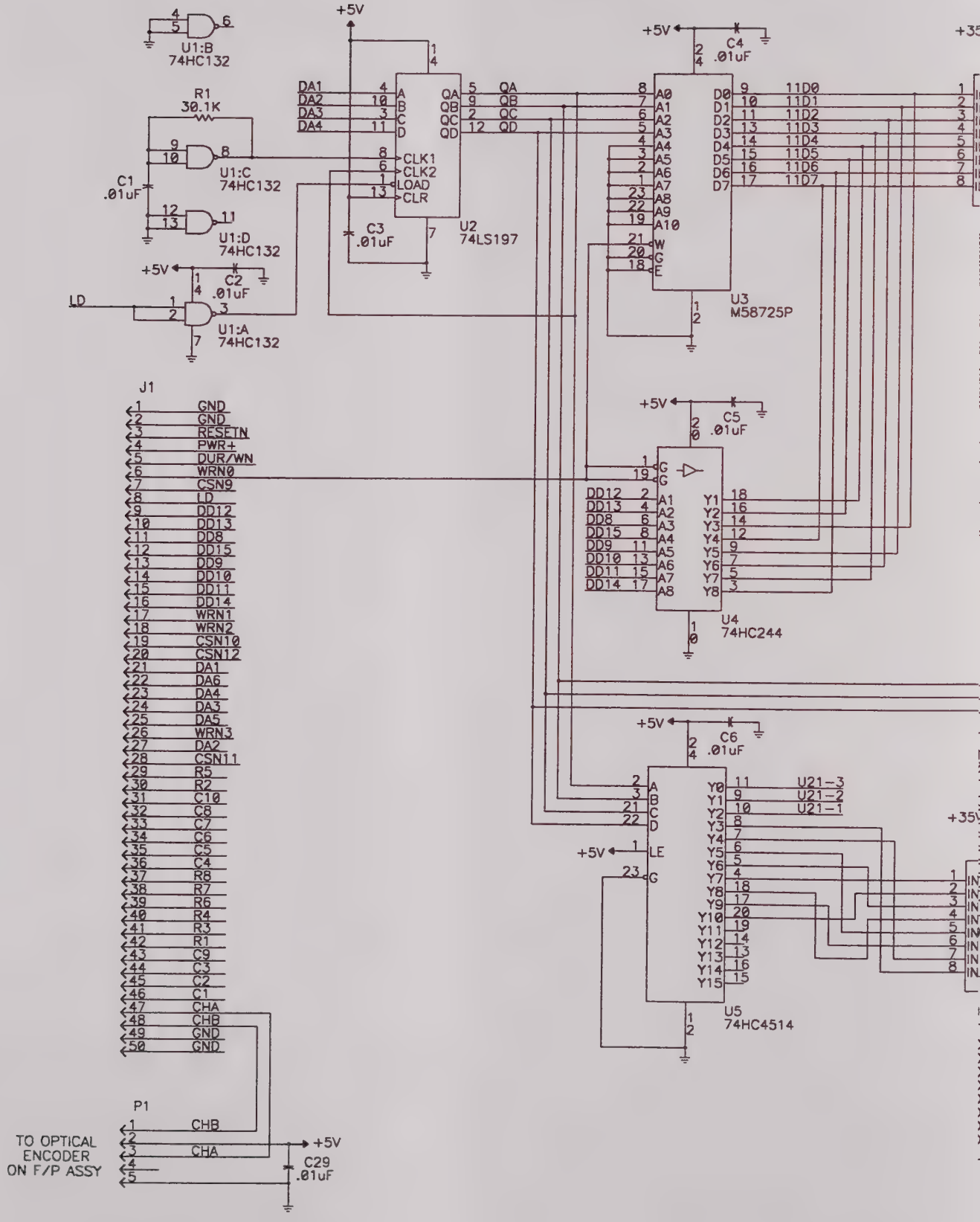


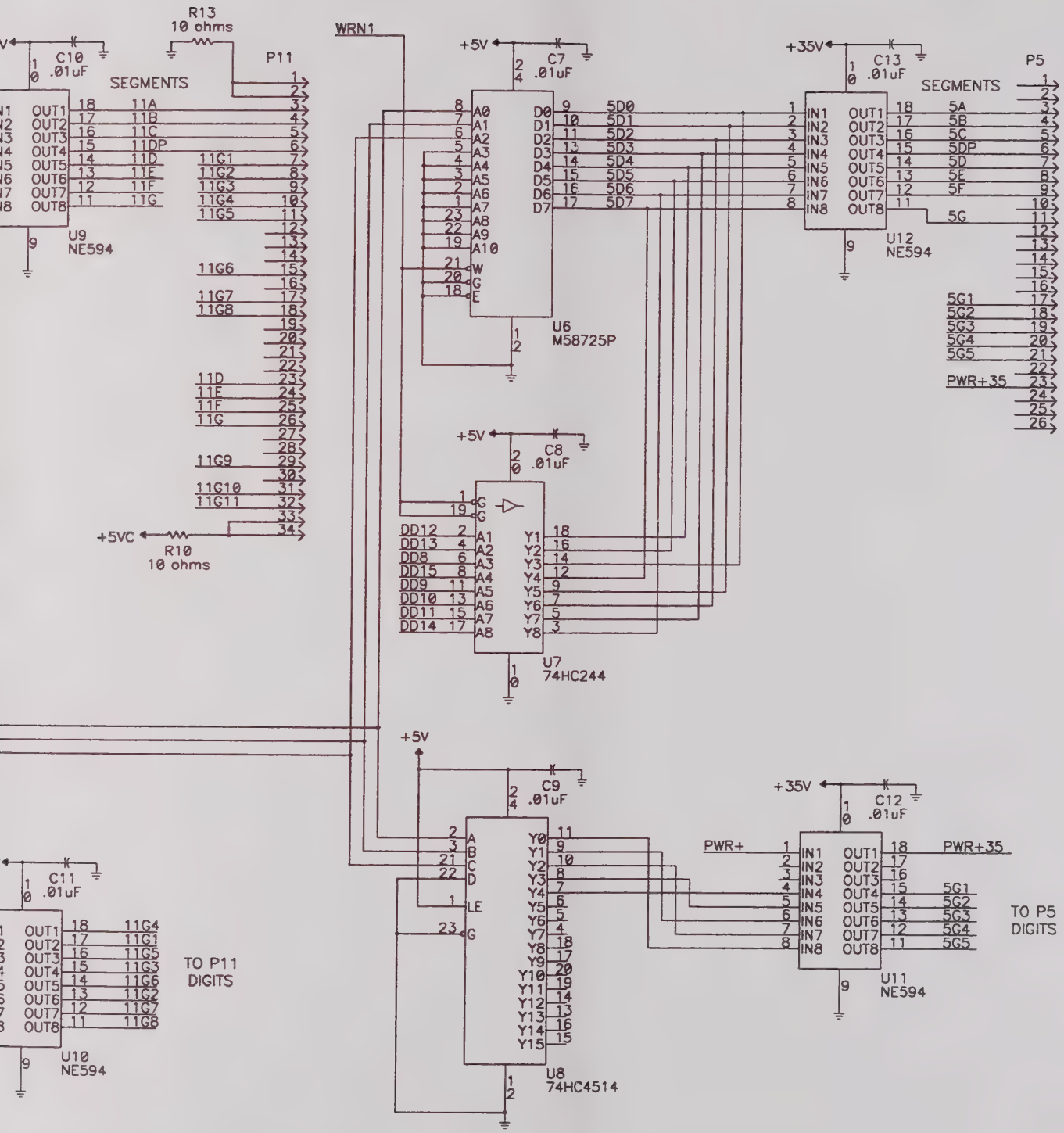

**DISPLAY DRIVER -- PC ASSY A20**

This board holds the necessary circuitry to drive the fluorescent displays and the LEDs on the front panel.

U2 is a counter which is clocked by U1 thereby cycling thru the addresses corresponding to each display digit and its segments. When the computer updates the display or when a setting has been changed, the LD line is activated, and the counter U2 stops counting and outputs the address which is on its A-D inputs, to QA-QD outputs thus addressing the decoders and RAMS when the appropriate chips are selected by the read/write lines. At this time data is available at the input of the latch U4 and can be loaded into the RAM U3. When the data has been updated for all addresses, the LD line becomes inactive and the counter U2 again cycles thru the addresses, selecting data for specific segments to be driven via U9. At the same time decoder U5 decodes the addresses to select each individual digit via U10. This scheme is used to drive all 3 fluorescent displays.

A similar scheme is used for lighting the LEDs on the front panel, the only difference is that they are addressed by rows and columns via U22 and U23 respectively.

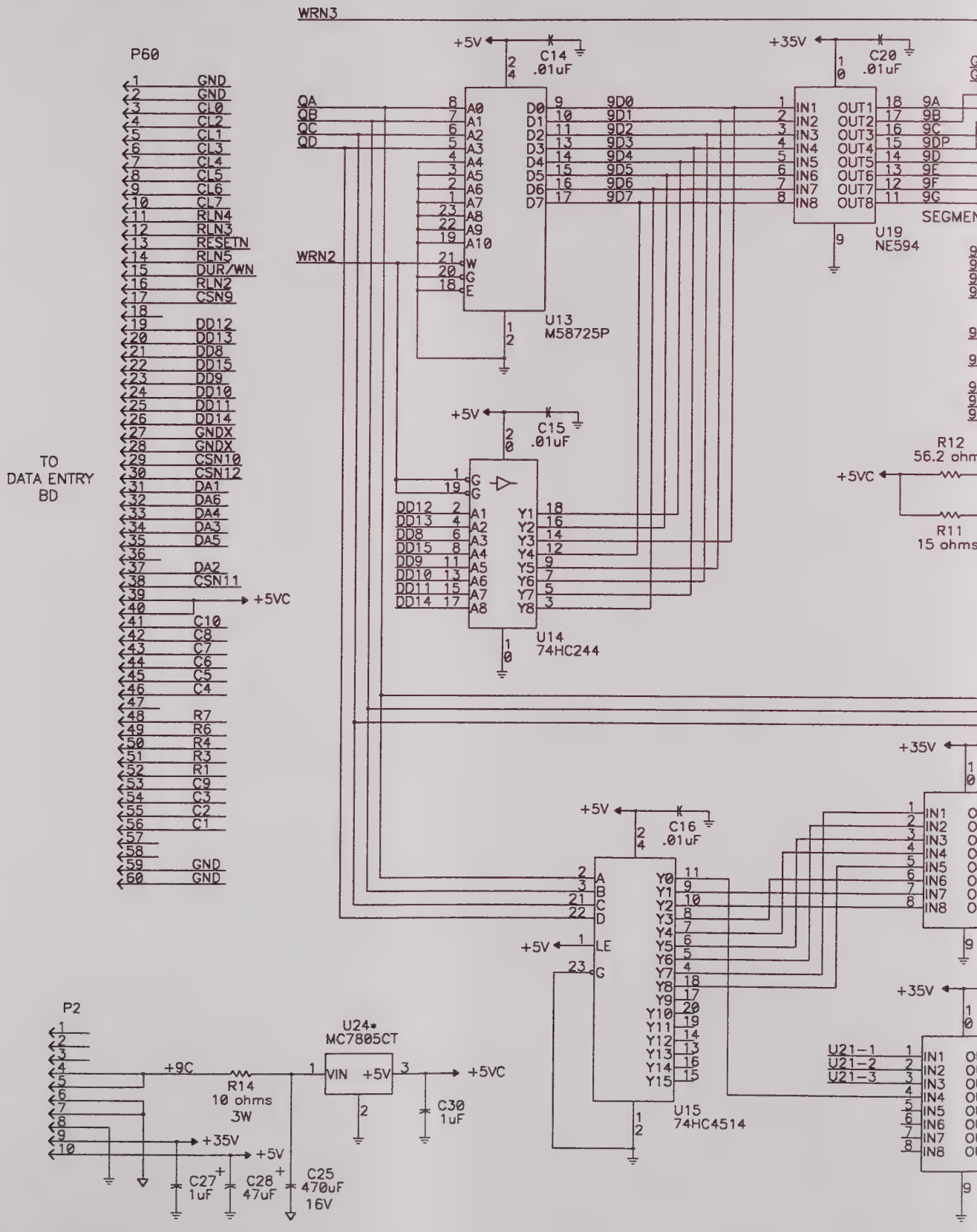

U1:B
74HC132
R1
30.1K
U1:C
74HC132
C1
.01uF
U1:D
74HC132
+5V
C2
.01uF
LD
U1:A
74HC132
+5V
DA1
DA2
DA3
DA4
CLK1
CLK2
LOAD
CLR
C3
.01uF
U2
74LS197
QA
QB
QC
QD
+5V
C4
.01uF
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
W
G
E
D0
D1
D2
D3
D4
D5
D6
D7
11D0
11D1
11D2
11D3
11D4
11D5
11D6
11D7
U3
M58725P
+5V
C5
.01uF
DD12
DD13
DD8
DD15
DD9
DD10
DD11
DD14
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
U4
74HC244
+5V
C6
.01uF
LE
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
Y9
Y10
Y11
Y12
Y13
Y14
Y15
U21-3
U21-2
U21-1
U5
74HC4514
J1
GND
GND
RESETN
PWR+
DUR/WN
WRN0
CSN9
LD
DD12
DD13
DD8
DD15
DD9
DD10
DD11
DD14
WRN1
WRN2
CSN10
CSN12
DA1
DA6
DA4
DA3
DA5
WRN3
DA2
CSN11
R5
R2
C10
C8
C7
C6
C5
C4
R8
R7
R6
R4
R3
R1
C9
C3
C2
C1
CHA
CHB
GND
GND
P1
CHB
CHA
TO OPTICAL
ENCODER
ON F/P ASSY
+5V
C29
.01uF

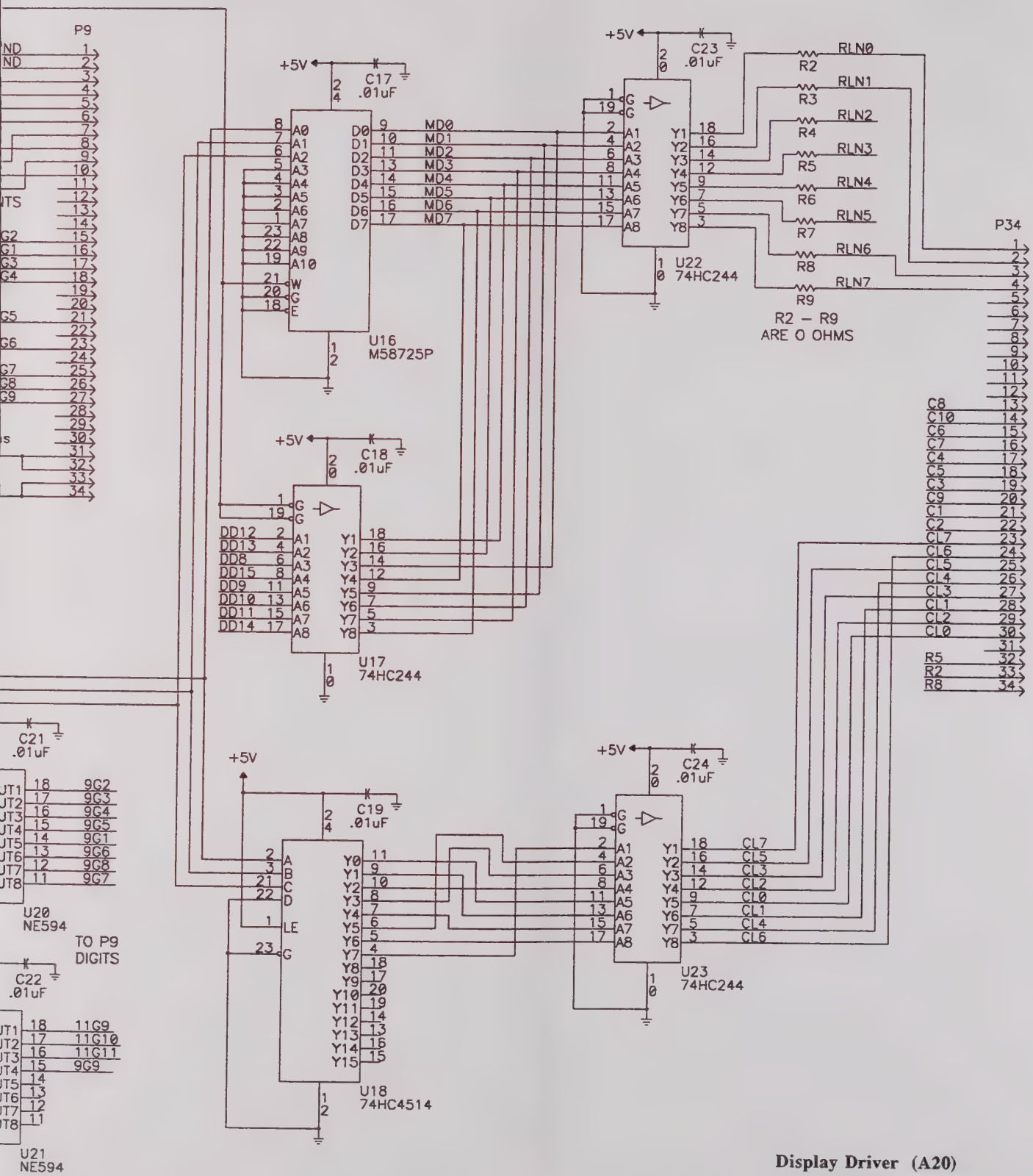



NOTES: UNLESS OTHERWISE SPECIFIED

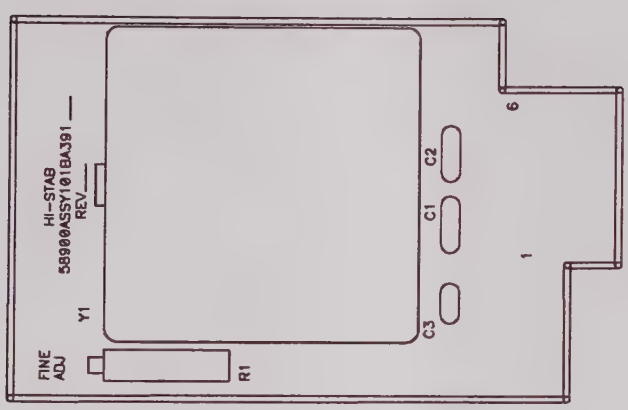
1. RESISTORS ARE IN OHMS
2. CAPACITORS ARE IN uF
3. * INDICATES HEATSINK IS REQUIRED

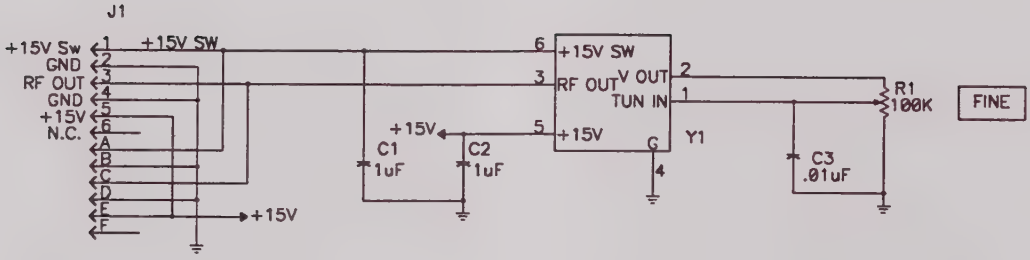
**Display Driver (A20)**
**ASSY# 1202221000 Rev A**
**Sheet 3 of 4**
**7-A20-3**


WRN3
P60
1 GND
2 GND
3 CL0
4 CL2
5 CL1
6 CL3
7 CL4
8 CL5
9 CL6
10 CL7
11 RLN4
12 RLN3
13 RESETN
14 RLN5
15 DUR/WN
16 RLN2
17 CSN9
18
19 DD12
20 DD13
21 DD8
22 DD15
23 DD9
24 DD10
25 DD11
26 DD14
27 GNDX
28 GNDX
29 CSN10
30 CSN12
31 DA1
32 DA6
33 DA4
34 DA3
35 DA5
36
37 DA2
38 CSN11
39
40 +5VC
41 C10
42 C8
43 C7
44 C6
45 C5
46 C4
47
48 R7
49 R6
50 R4
51 R3
52 R1
53 C9
54 C3
55 C2
56 C1
57
58
59 GND
60 GND
TO DATA ENTRY BD
+5V
C14 .01uF
QA
QB
QC
QD
WRN2
U13 M58725P
+35V
C20 .01uF
U19 NE594
SEGMEN
+5V
C15 .01uF
U14 74HC244
R12 56.2 ohm
+5VC
R11 15 ohms
+35V
+5V
C16 .01uF
LE
U15 74HC4514
P2
U24* MC7805CT
+9C
R14 10 ohms 3W
VIN
+5V
+5VC
C30 1uF
+35V
+5V
C27 1uF
C28 47uF
C25 470uF 16V
U21-1
U21-2
U21-3



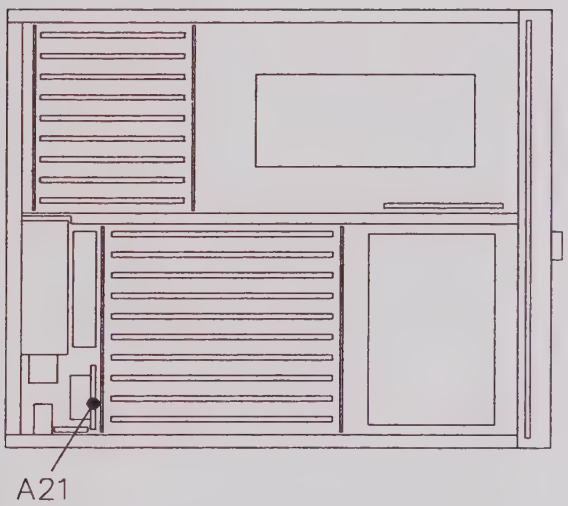

**Display Driver (A20)**
**ASSY# 1202221000 Rev A**
**Sheet 4 of 4**
**7-A20-4**



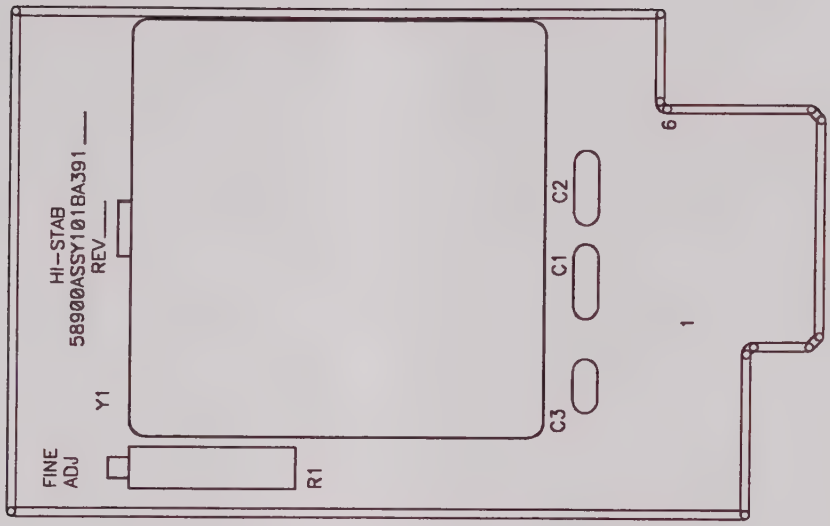



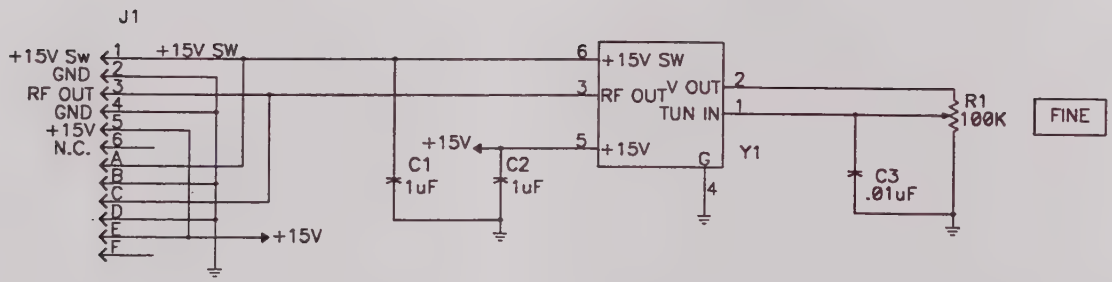

NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPACITOR VALUES ARE IN uF
2. RESISTOR VALUES ARE IN OHMS
3. RESISTORS ARE 1/5W,1%



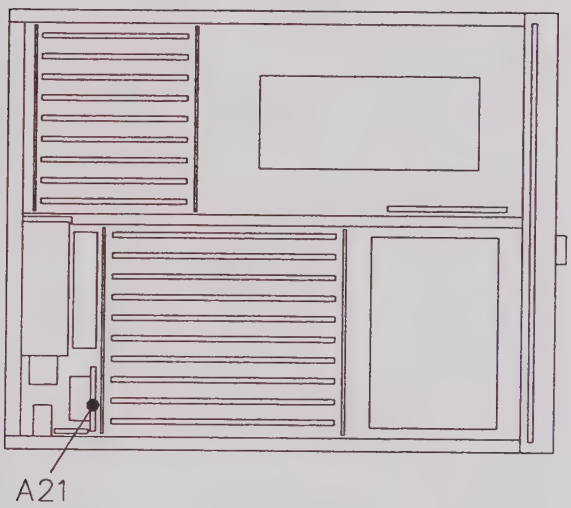

**High Stability Osc (A21)**
**ASSY# 101BA39101 Rev B**
**Sheet 1 of 1**
**7-A21-1**



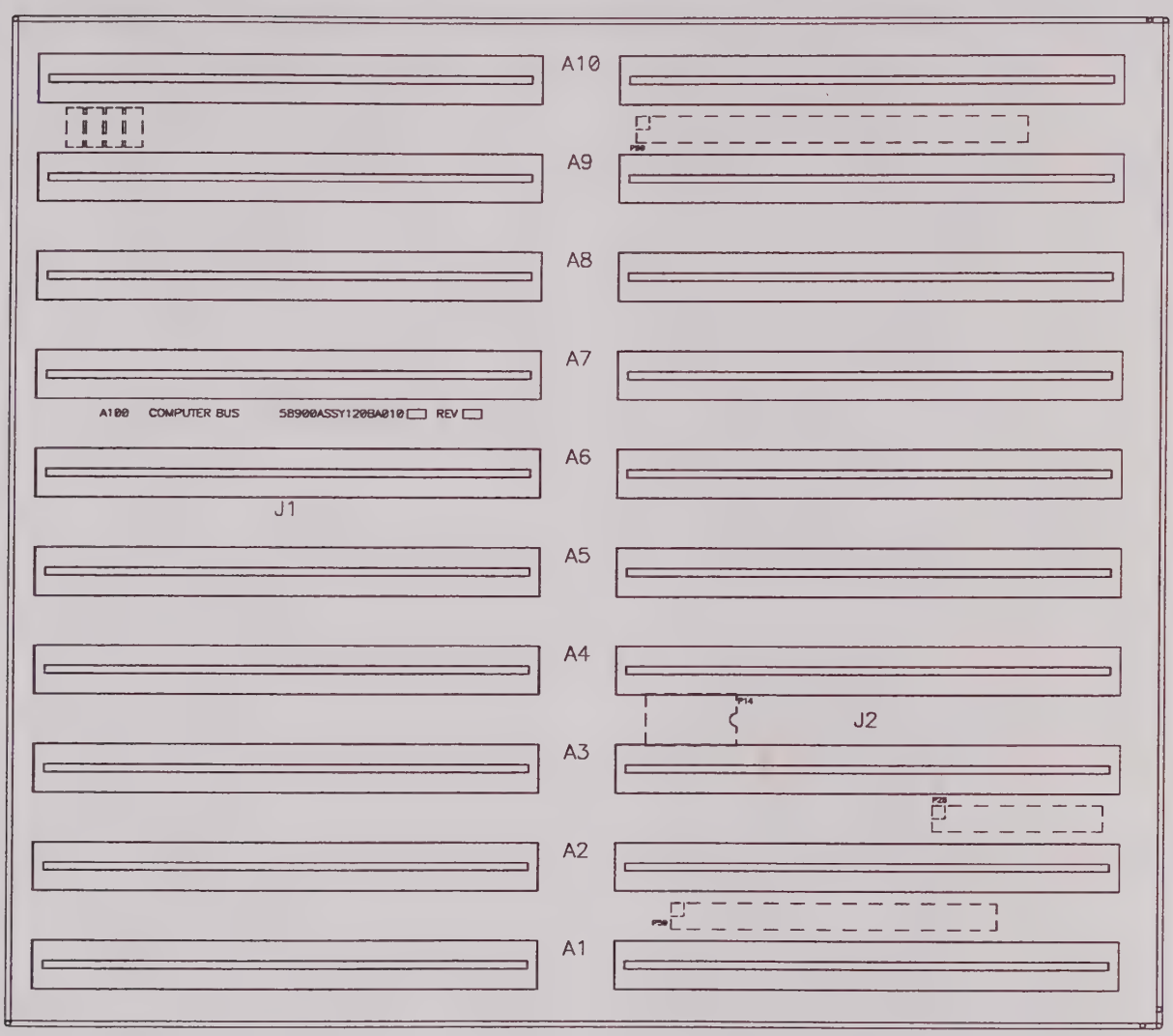



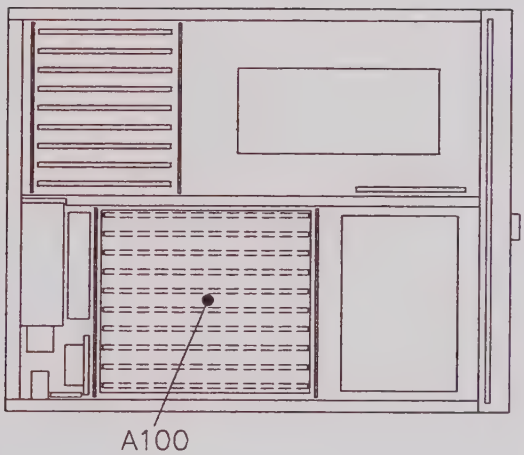

NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPACITOR VALUES ARE IN uF
2. RESISTOR VALUES ARE IN OHMS
3. RESISTORS ARE 1/5W,1%

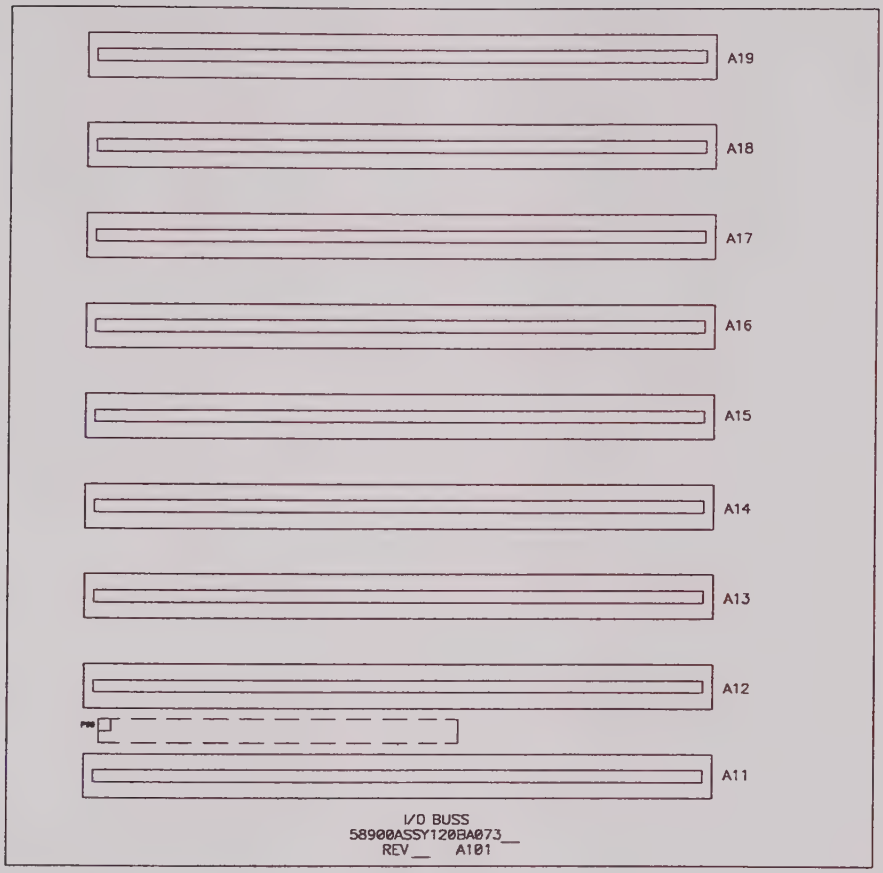


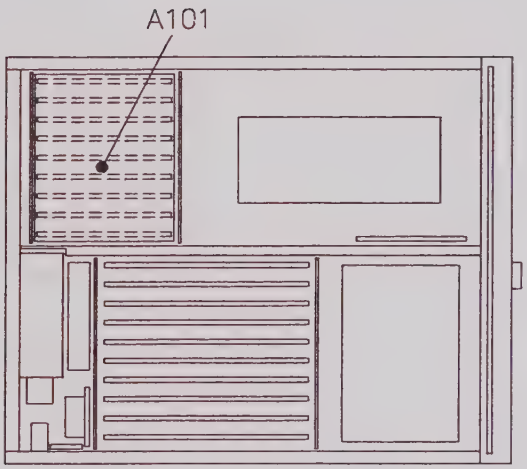

**High Stability Oscillator (A21)**
**ASSY# 101BA39103 Rev A**
**Sheet 1 of 1**
**7-A21-2**


A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A100 COMPUTER BUS 5B900ASSY120BA010 REV
J1
J2

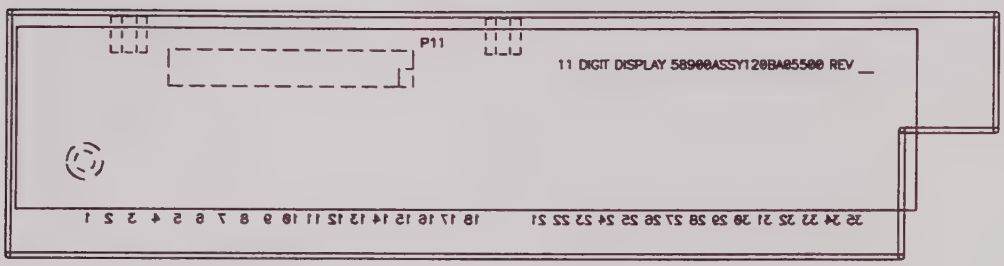


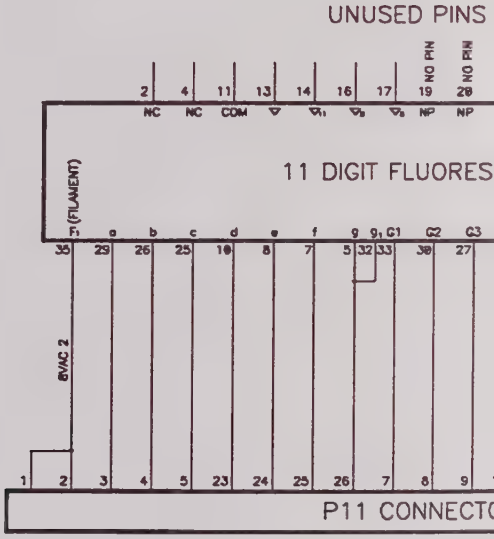

**Computer Bus (A100)**
**ASSY# 120BA01000 Rev E**
**Sheet 1 of 1**
**7-A100-1**

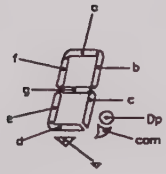

A19
A18
A17
A16
A15
A14
A13
A12
PWR
A11
I/O BUSS
58900ASSY120BA073__
REV__ A101



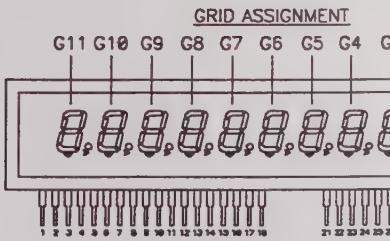

**I/O Bus (A101)**
**ASSY# 120BA07300 Rev F**
**Sheet 1 of 1**
**7-A101-1**

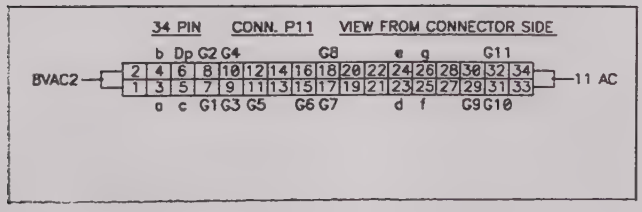


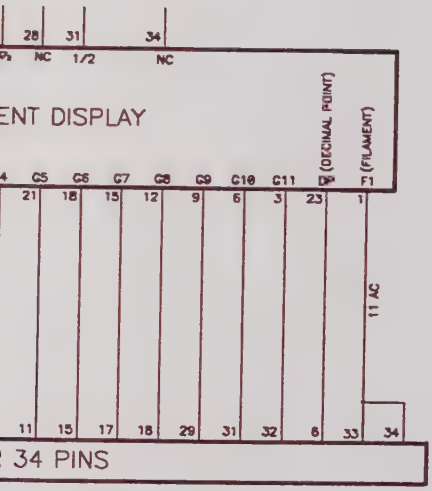



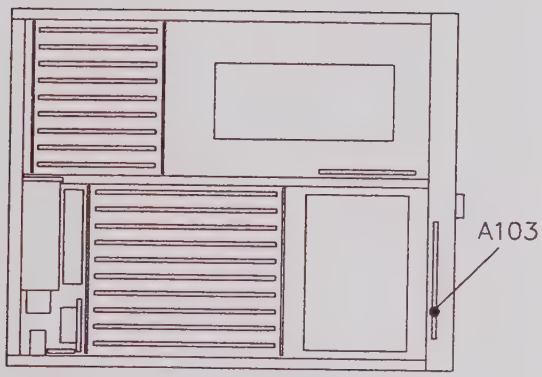



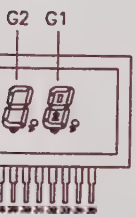

DIG 2 thru 11
SEGMENT
DESIGNATION

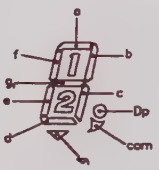




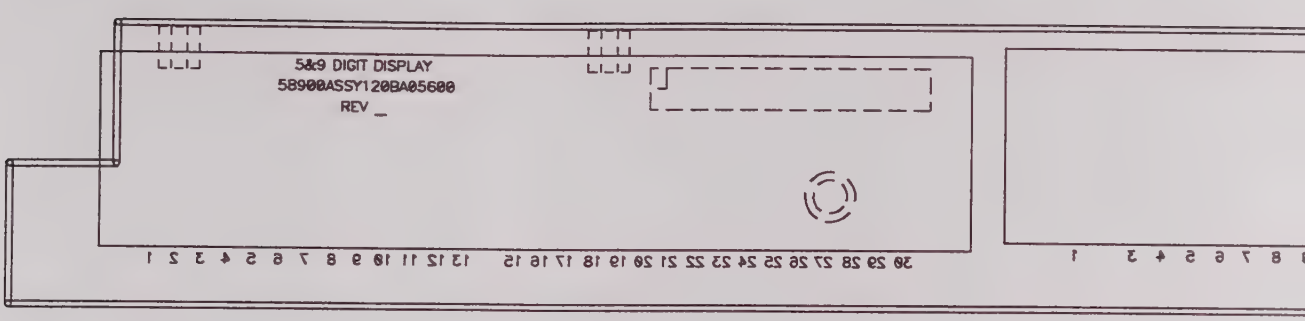



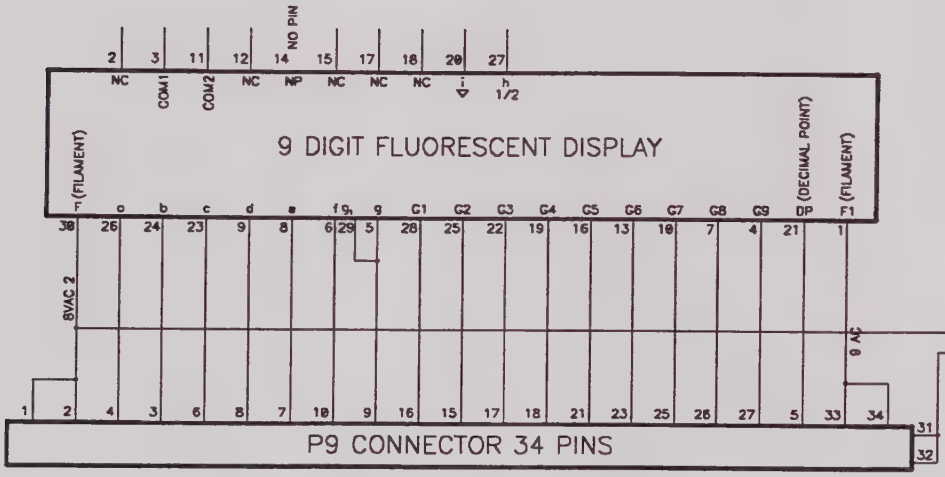



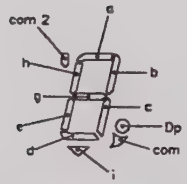

DIG. 1
SEGMENT
DESIGNATION

**11 Digit Display (A103)**
**ASSY# 120BA05500 Rev C**
**Sheet 1 of 1**
**7-A103-1**



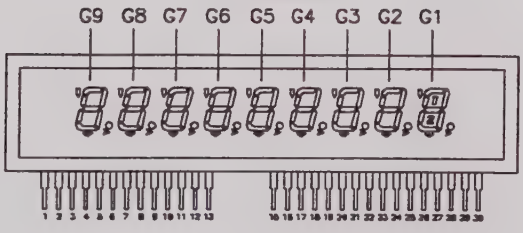

UNUSED PINS

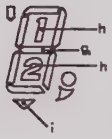



DIG 1 thru 9

GRID ASSIGNMENT




DIG. 1

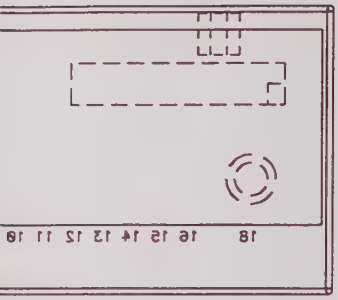
34 PIN CONN. P9 VIEW FROM CONNECTOR SIDE

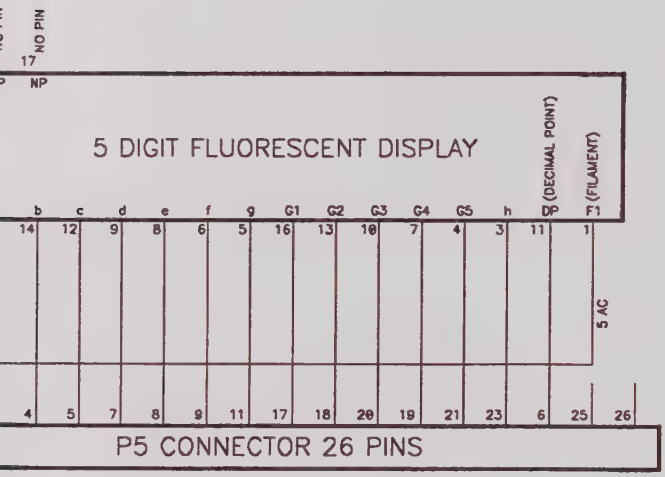
| | a | c | d | f | | | | G1 | G4 | | | G8 | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 8VAC2 | 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 | 24 | 26 | 28 | 30 | 32 | 34 |
| | 1 | 3 | 5 | 7 | 9 | 11 | 13 | 15 | 17 | 19 | 21 | 23 | 25 | 27 | 29 | 31 | 33 |
| | b | Dp | e | g | | | | 2G | 3G | | 5G | 6G | 7G | 9G | | | |

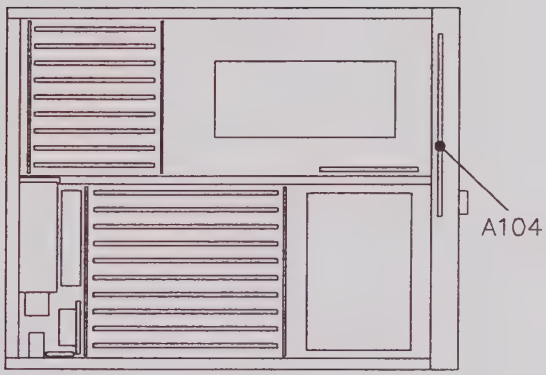
5 AC
9 AC
5 AC

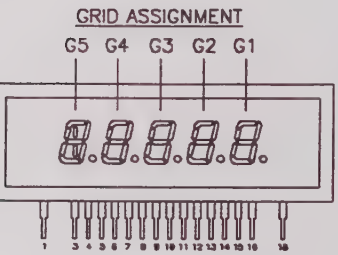
26 PIN CONN. P5 VIEW FROM CONNECTOR SIDE

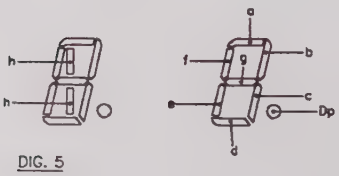
| | b | Dp | e | | | | | G2 | G3 | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 | 24 | 26 |
| | 1 | 3 | 5 | 7 | 9 | 11 | 13 | 15 | 17 | 19 | 21 | 23 | 25 |
| | a | c | d | f | g | | | G1 | G4 | G5 | h | | |



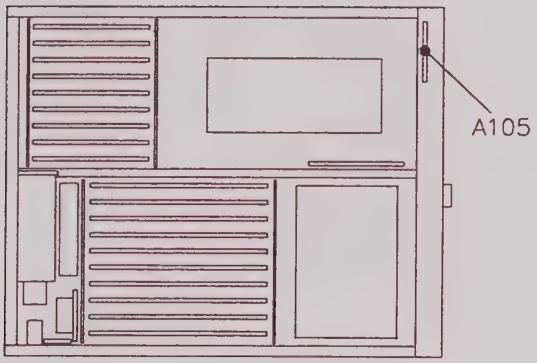

NO PIN
17
NP
5 DIGIT FLUORESCENT DISPLAY
DP (DECIMAL POINT)
F1 (FILAMENT)
b c d e f g G1 G2 G3 G4 G5 h
14 12 9 8 6 5 16 13 10 7 4 3 11 1
5 AC
4 5 7 8 9 11 17 18 20 19 21 23 6 25 26
P5 CONNECTOR 26 PINS



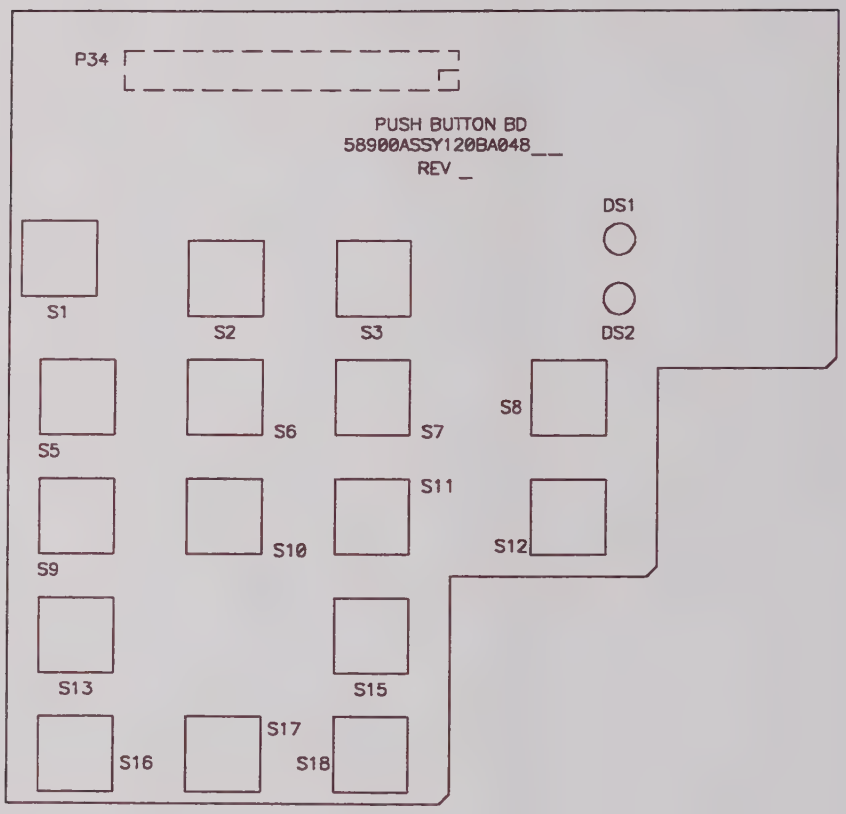



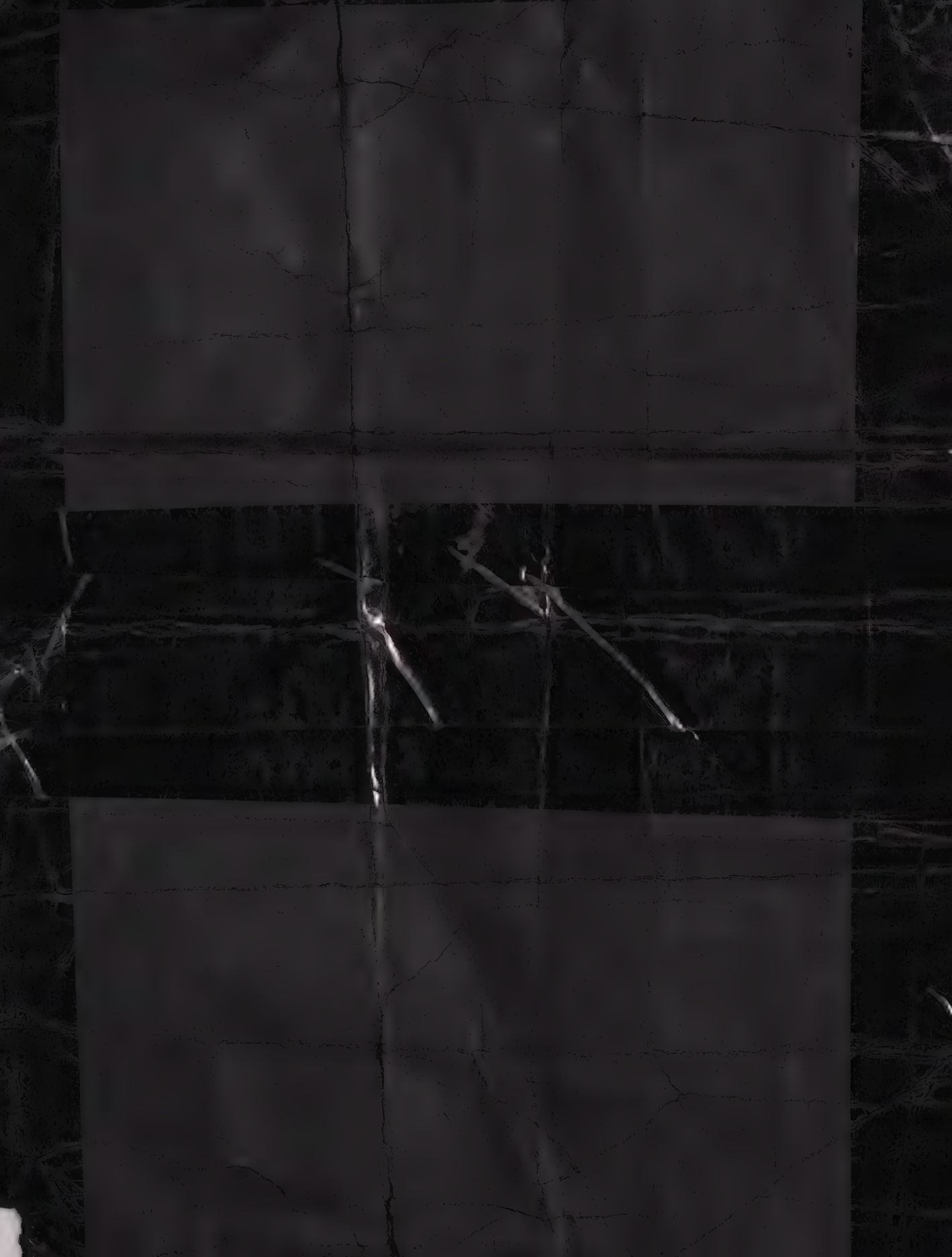

**5 & 9 Digit Display (A104)**
**ASSY# 120BA05600 Rev C**
**Sheet 1 of 1**
**7-A104-1**




**Pushbutton (A105)**
**ASSY# 120BA04801 Rev C**
**Sheet 1 of 3**
**7-A105-1**



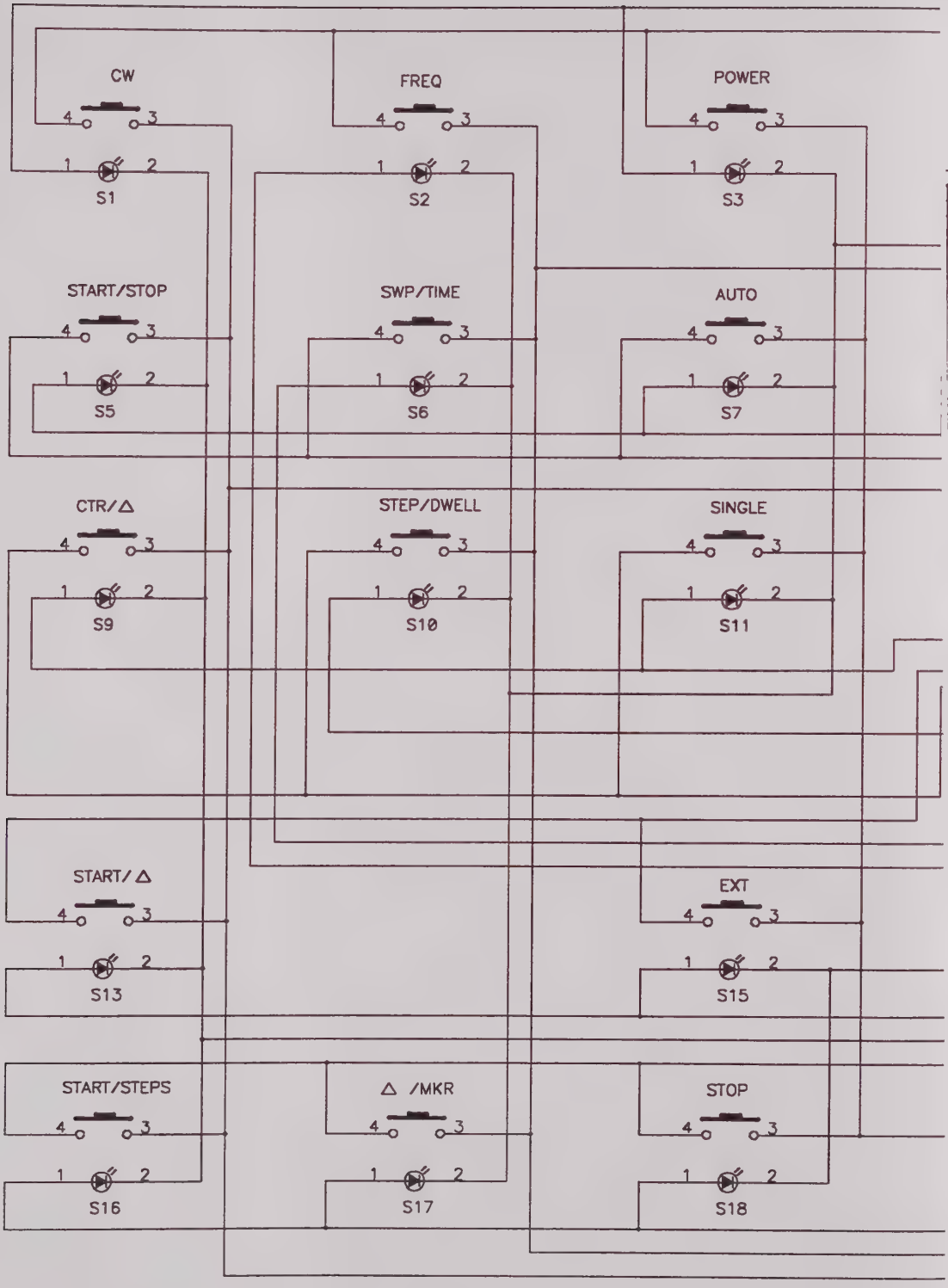

**Pushbutton (A105)**
**ASSY# 120BA04801 Rev C**
**Sheet 2 of 3**
**7-A105-2**

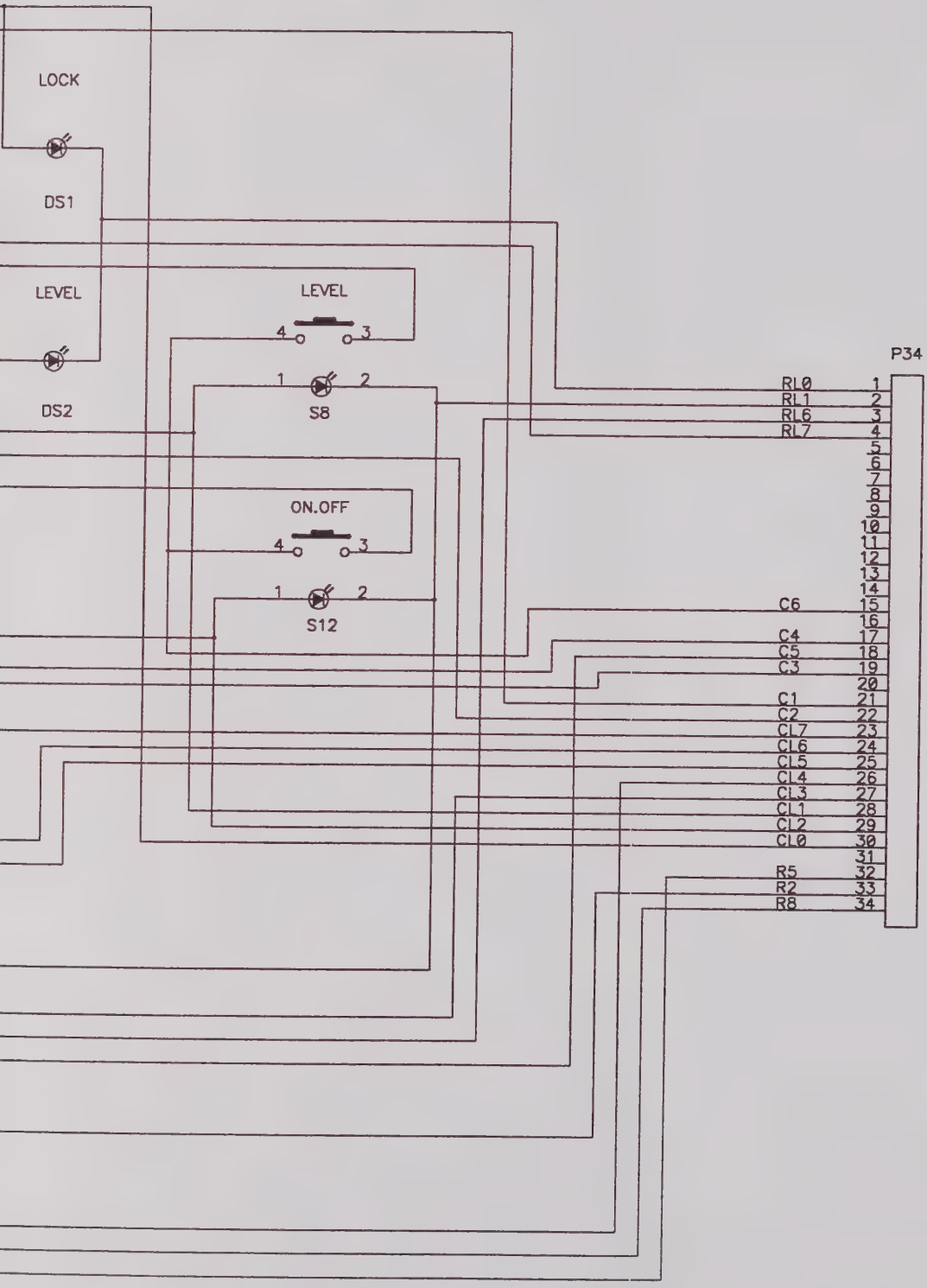


**PUSH BUTTON -- PC ASSY A105**

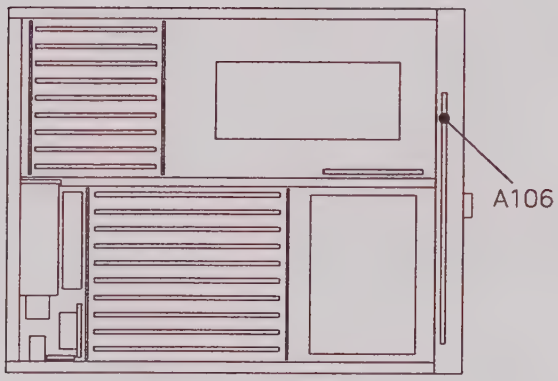
The Push Button board holds the push buttons for the sweep functions, the level buttons and their corresponding LEDs as well as the LOCK and LEVEL LEDs.

The buttons are connected together such that they can be read and identified using a row and column scheme. The LEDs are set up the same way using a row and column scheme (denoted RL and CL) to light the appropriate LEDs.

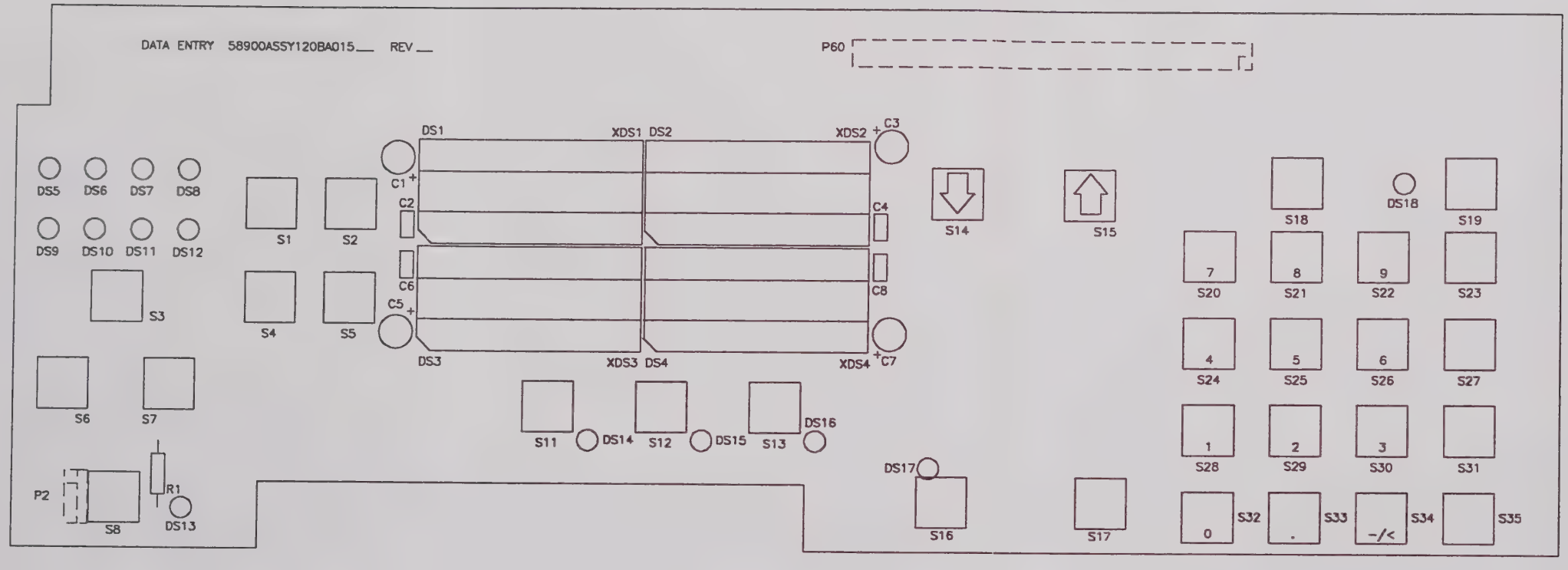

CW
FREQ
POWER
S1
S2
S3
START/STOP
SWP/TIME
AUTO
S5
S6
S7
CTR/△
STEP/DWELL
SINGLE
S9
S10
S11
START/△
EXT
S13
S15
START/STEPS
△ /MKR
STOP
S16
S17
S18




**Pushbutton (A105)**
**ASSY# 120BA04801 Rev C**
**Sheet 3 of 3**
**7-A105-3**




**Data Entry (A106)**
**ASSY# 120BA01511 Rev B**
**Sheet 1 of 4**
**7-A106-1**

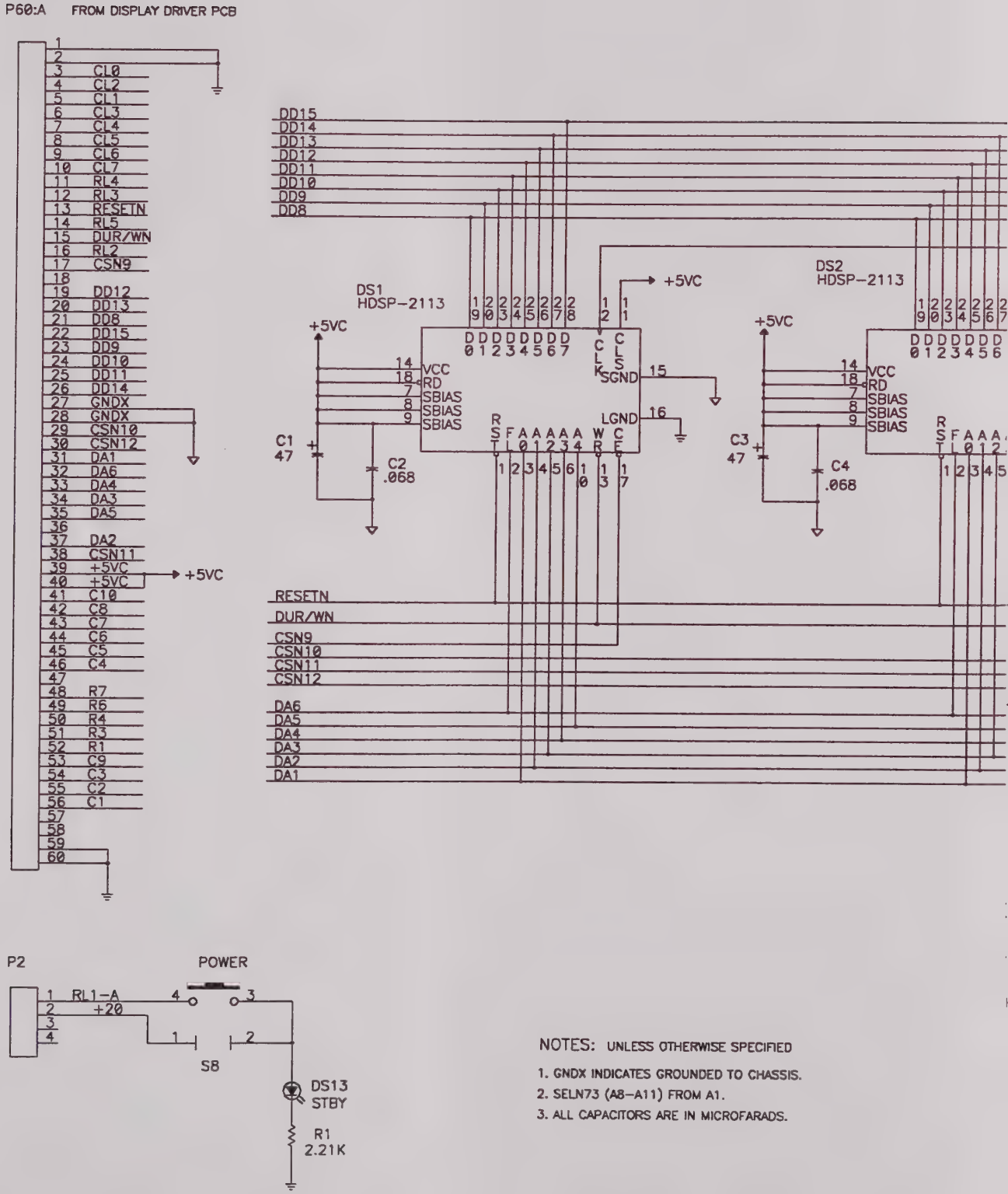



**DATA ENTRY -- PC ASSY A106**

This board holds the push buttons for the keypad, modulation buttons and the sweep marker buttons, as well as any corresponding LEDs. In addition the Intelligent HP alpha numeric displays reside on this board.

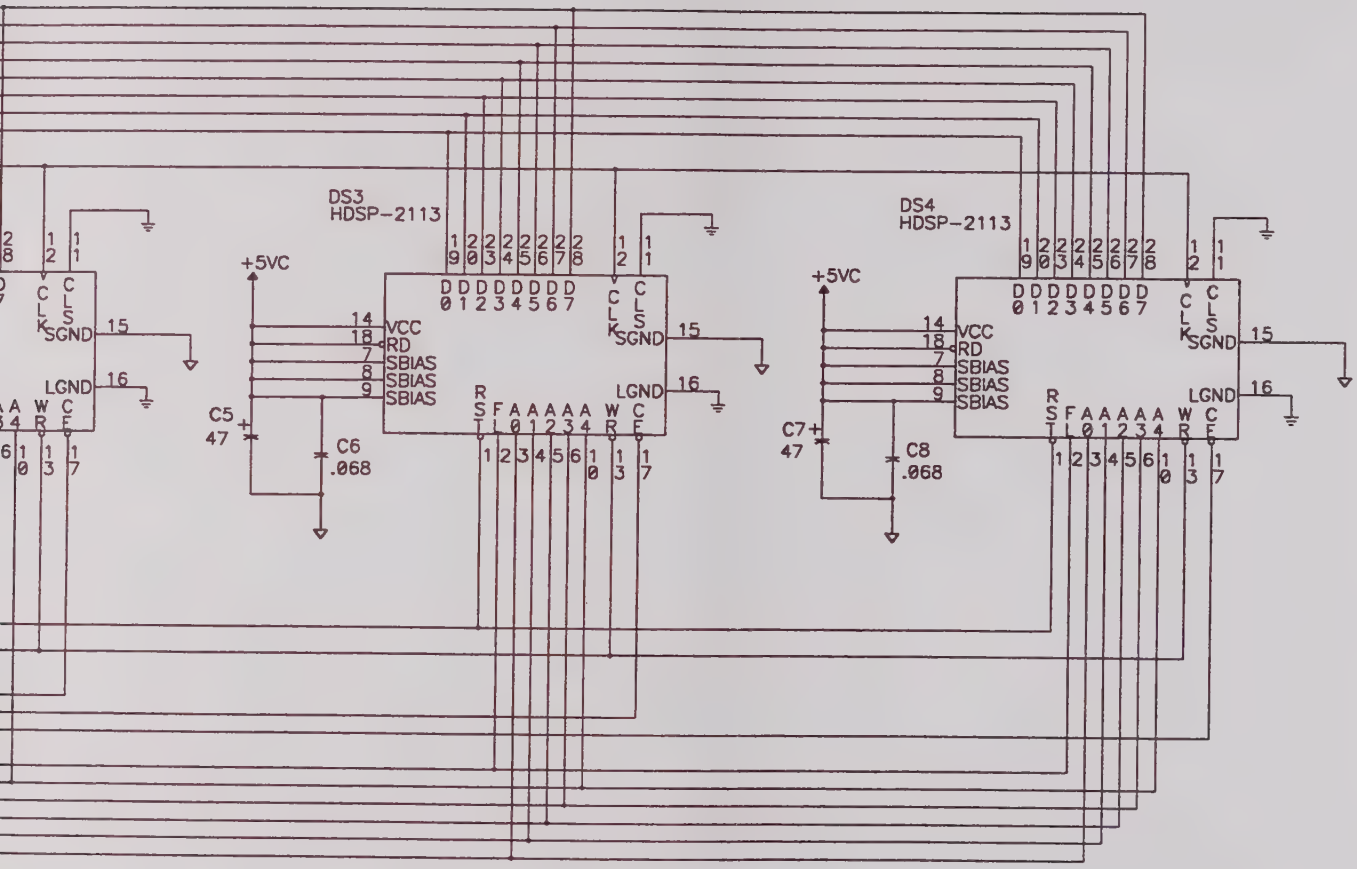
As on the Push Button Board A105, the push buttons are read and the LEDs are lit using the rows and columns scheme. The four, 8-digit Intelligent HP alpha numeric displays (DS1-DS4) receive address and data information from the display driver board.

When the unit has power applied to it the standby LED DS13 is lit by the 20V from the power supply via P2. When the power switch is activated the 20V coming in on P2 is switched to energize the power relay switch which supplies power to the rest of the unit.

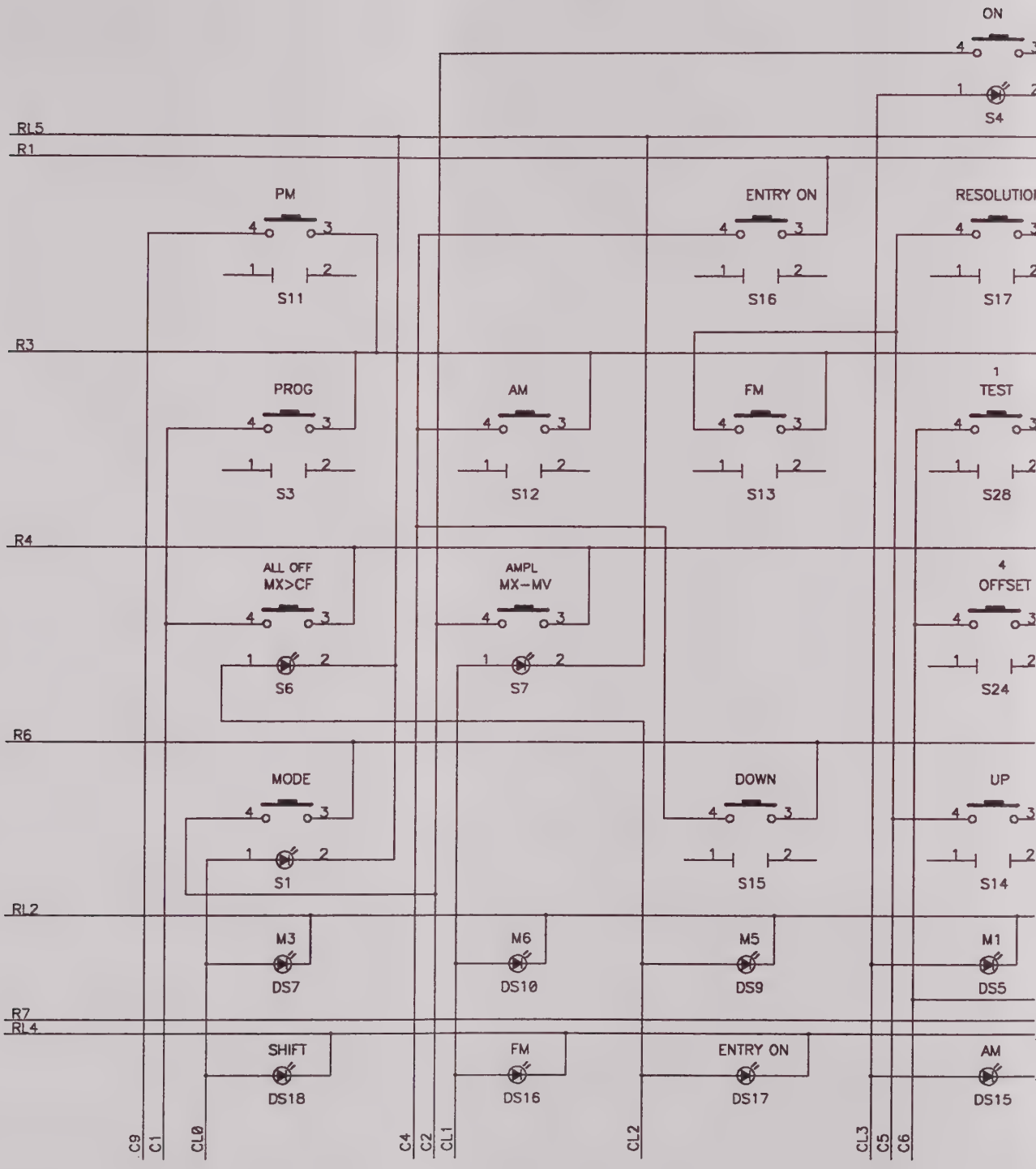


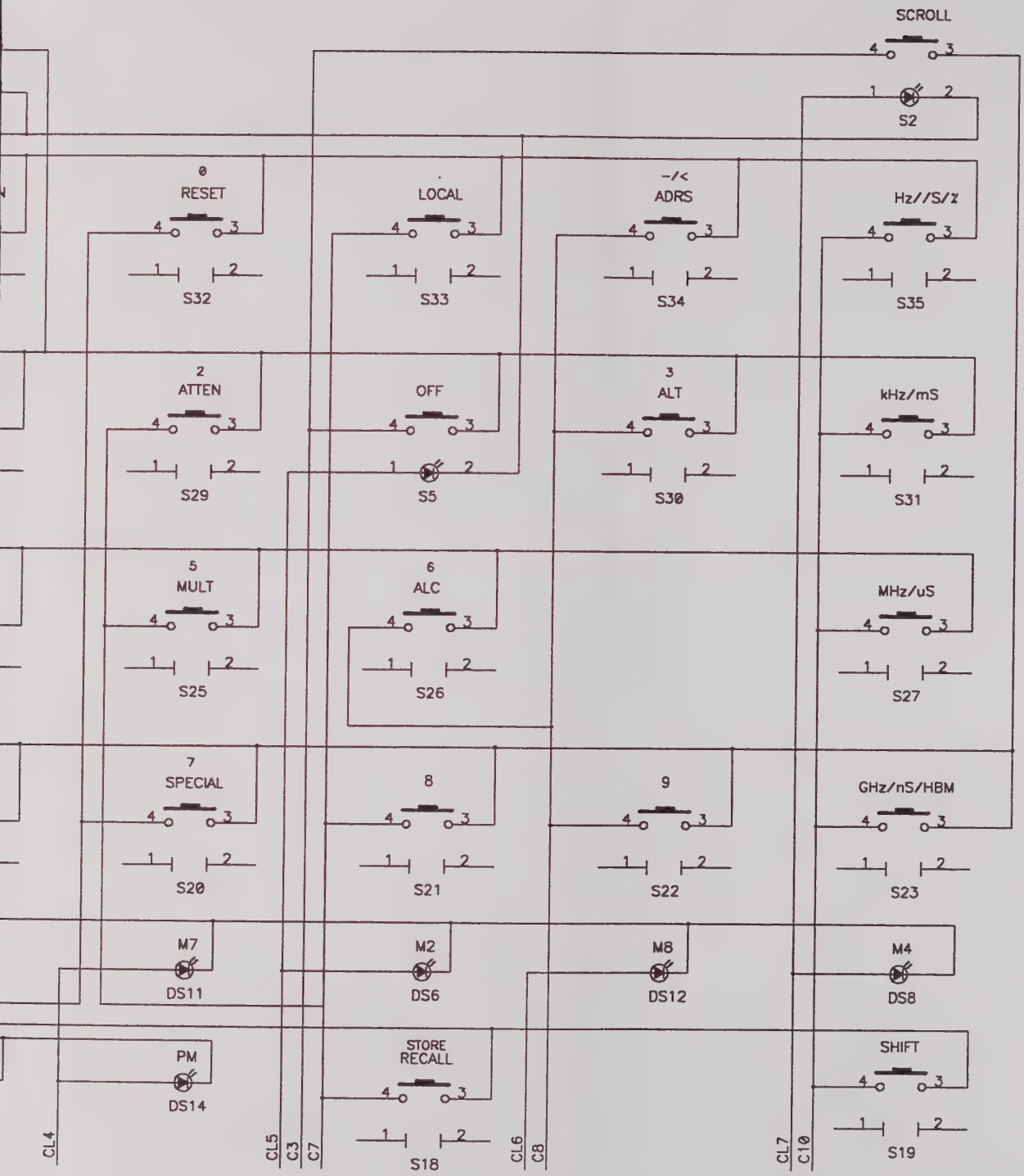

NOTES: UNLESS OTHERWISE SPECIFIED

1. GNDX INDICATES GROUNDED TO CHASSIS.
2. SELN73 (A8–A11) FROM A1.
3. ALL CAPACITORS ARE IN MICROFARADS.

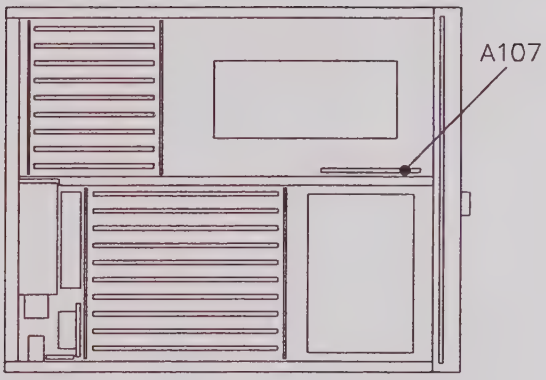



**Data Entry (A106)**
**ASSY# 120BA01511 Rev B**
**Sheet 3 of 4**
**7-A106-3**

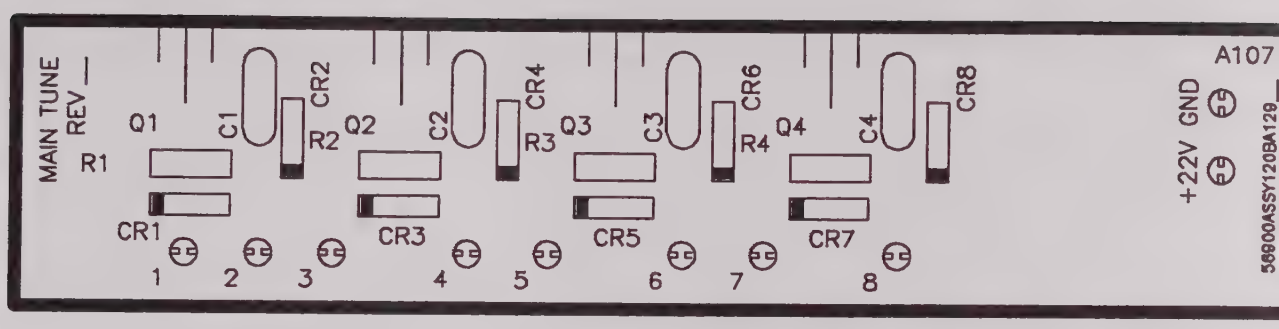

ON
S4
RL5
R1
PM
S11
ENTRY ON
S16
RESOLUTION
S17
R3
PROG
S3
AM
S12
FM
S13
TEST
S28
R4
ALL OFF
MX>CF
S6
AMPL
MX-MV
S7
OFFSET
S24
R6
MODE
S1
DOWN
S15
UP
S14
RL2
M3
DS7
M6
DS10
M5
DS9
M1
DS5
R7
RL4
SHIFT
DS18
FM
DS16
ENTRY ON
DS17
AM
DS15
C9
C1
CL0
C4
C2
CL1
CL2
CL3
C5
C6

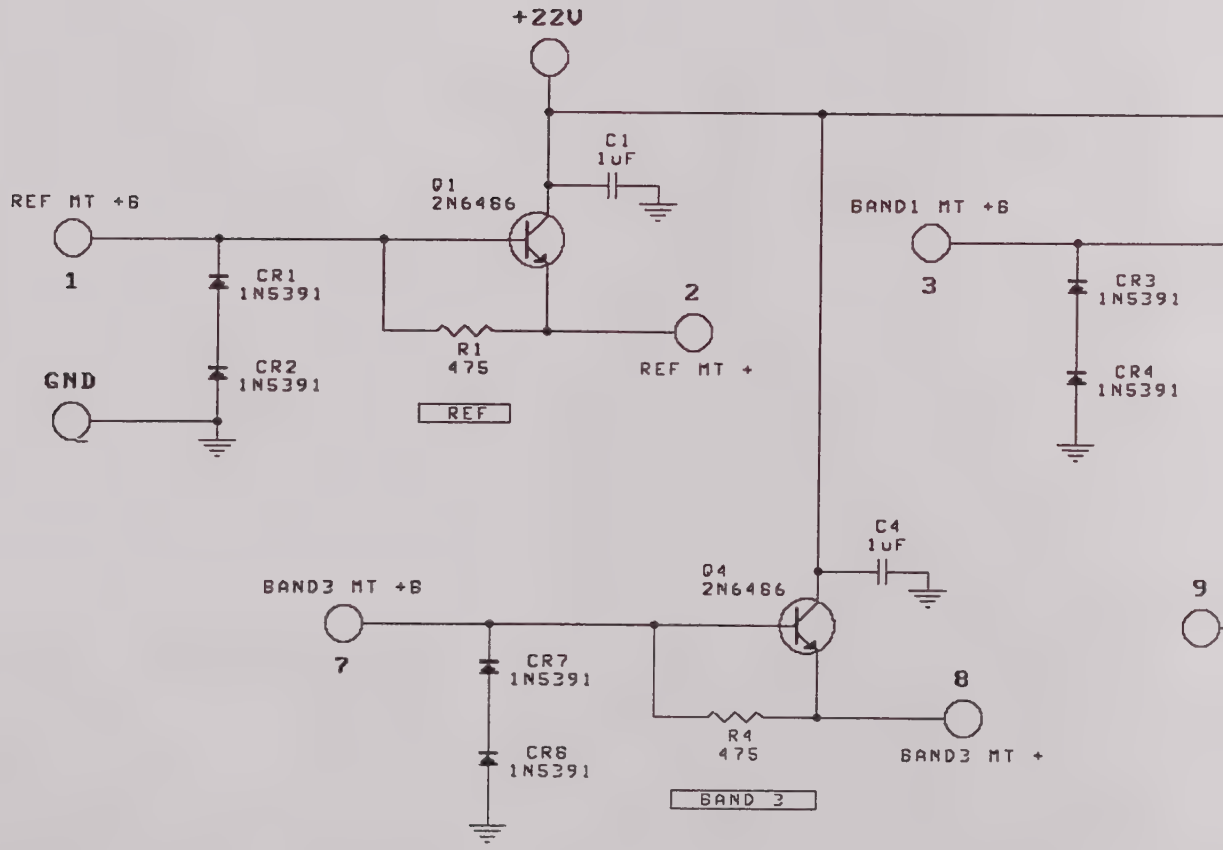



**Data Entry (A106)**
**ASSY# 120BA01511 Rev B**
**Sheet 4 of 4**
**7-A106-4**



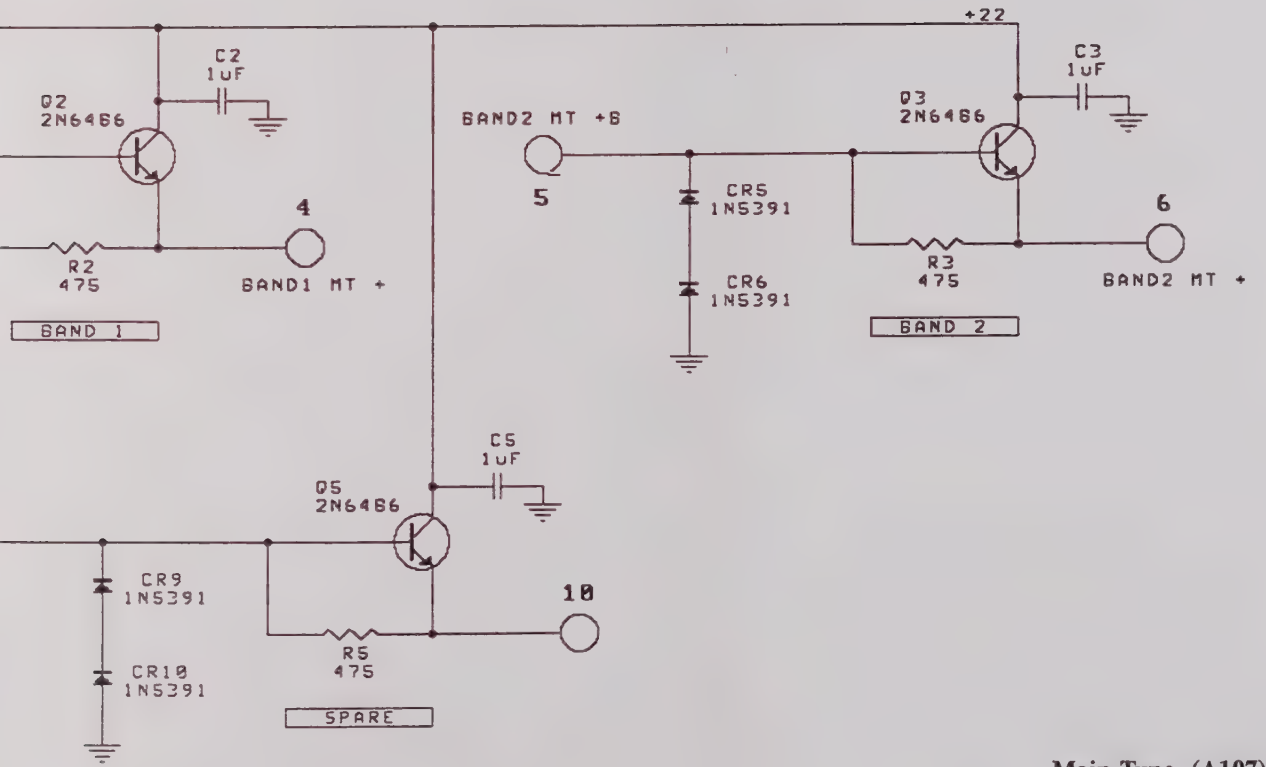

**Main Tune (A107)**
**ASSY# 120BA12900 Rev A**
**Sheet 1 of 2**
**7-A107-1**


MAIN TUNE
REV__
A107
Q1
C1
CR2
R1
R2
Q2
C2
CR4
R3
Q3
C3
CR6
R4
Q4
C4
CR8
CR1
CR3
CR5
CR7
1
2
3
4
5
6
7
8
+22V GND
50900ASSY120BA129__

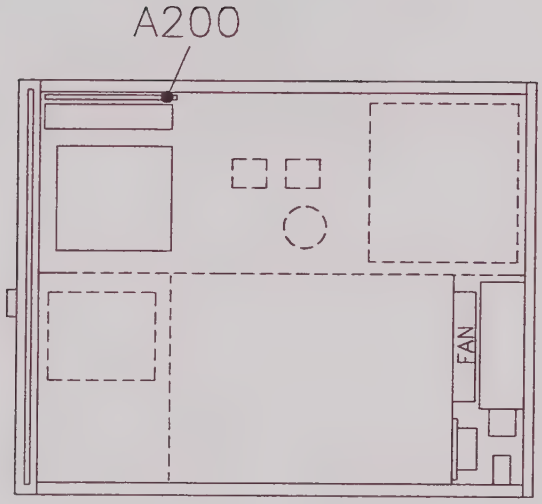

+22V
C1
1uF
Q1
2N6486
REF MT +B
1
CR1
1N5391
CR2
1N5391
GND
R1
475
2
REF MT +
REF
BAND1 MT +B
3
CR3
1N5391
CR4
1N5391
C4
1uF
Q4
2N6486
BAND3 MT +B
7
CR7
1N5391
CR8
1N5391
R4
475
8
BAND3 MT +
BAND 3
9

## MAIN TUNE -- PC ASSY A107

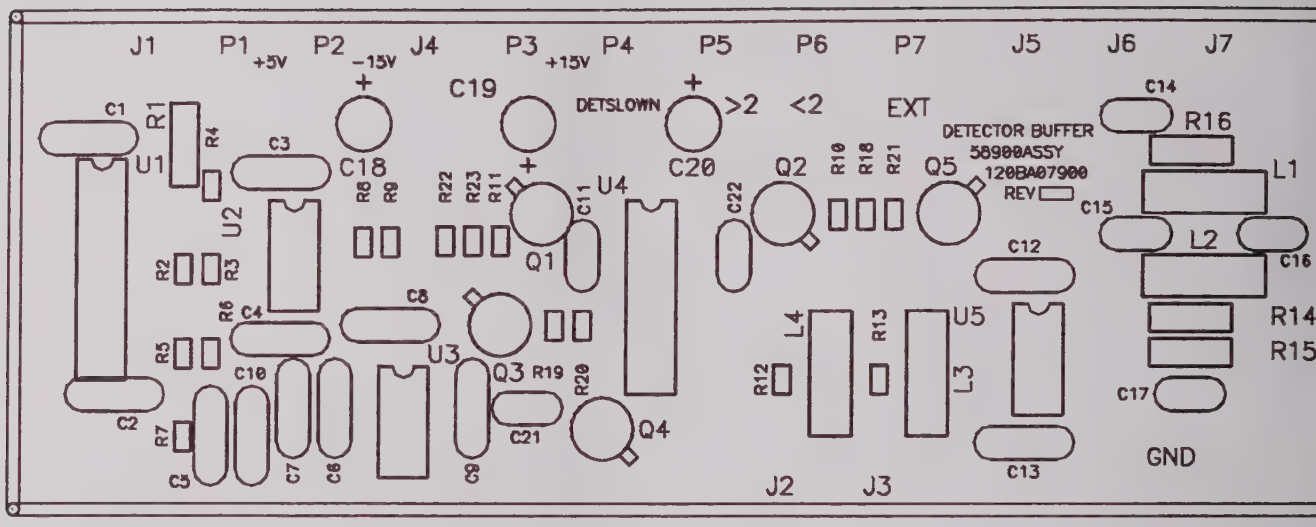
This circuit board is mounted on the chassis between the microwave deck and the power supply capacitors. The board holds the transistors which actually provide the current drive to the Main Tune coils of each of the YIG oscillators. These transistors must provide high currents, resulting in substantial power dissipation which requires the transistors to have a heat sink. The diodes at the base of each transistor are there to prevent the voltage from going too far negative.



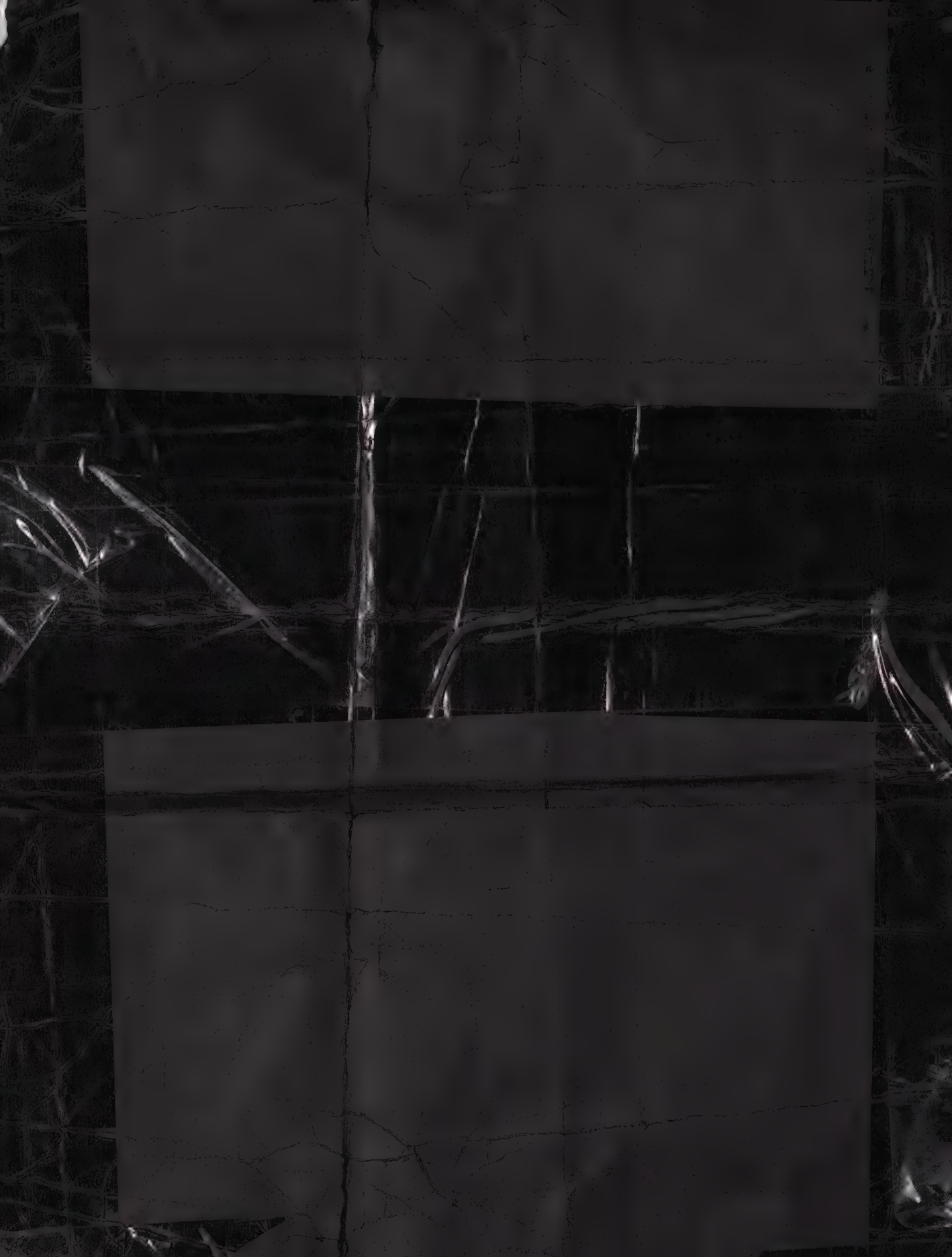

**Main Tune (A107)**
**ASSY# 120BA12900 Rev A**
**Sheet 2 of 2**
**7-A107-2**




**Detector Buffer (A200)**
**ASSY# 120BA07900 Rev D**
**Sheet 1 of 3**
**7-A200-1**



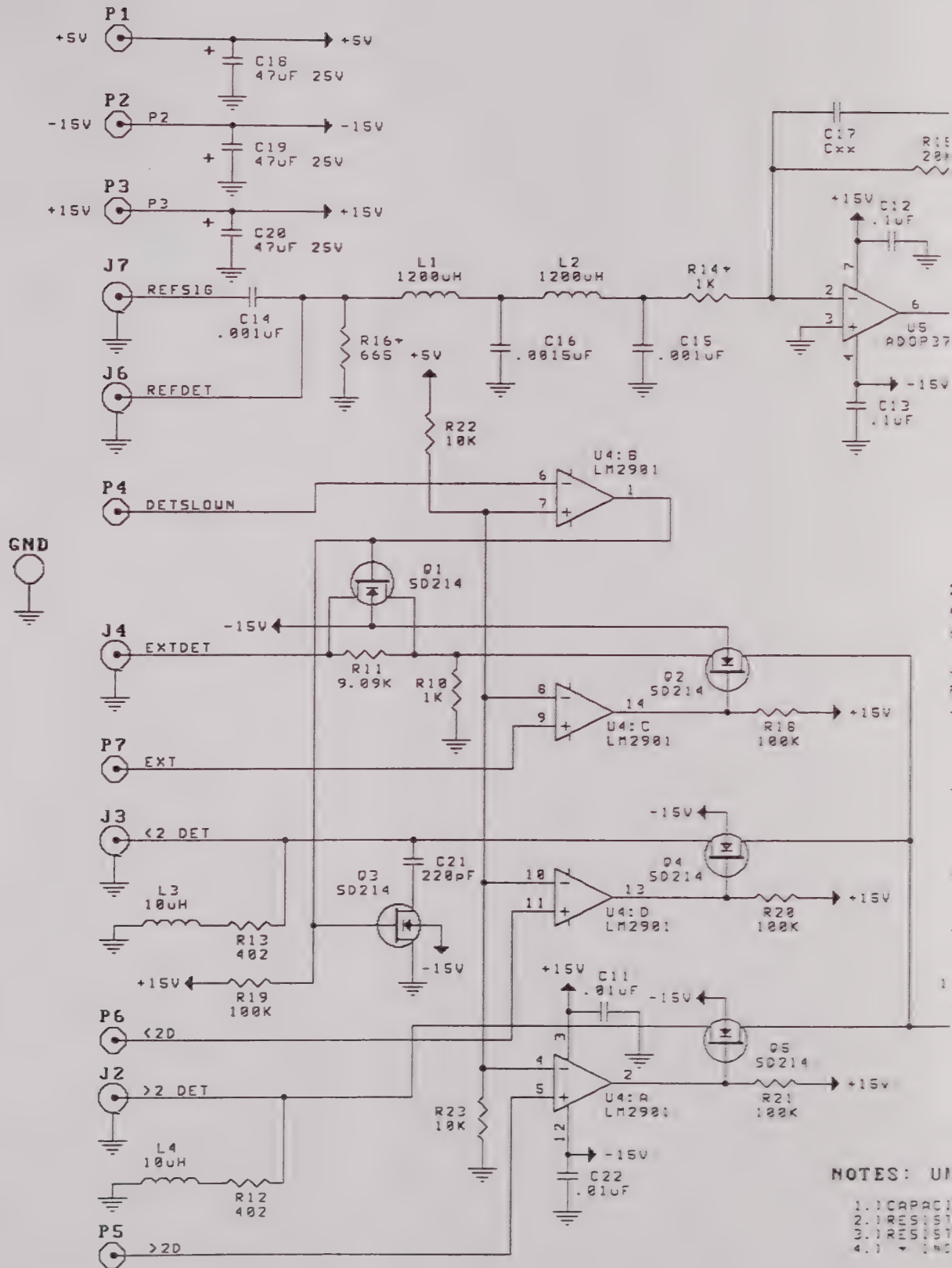

**Detector Buffer (A200)**
**ASSY# 120BA07900 Rev D**
**Sheet 2 of 3**
**7-A200-2**

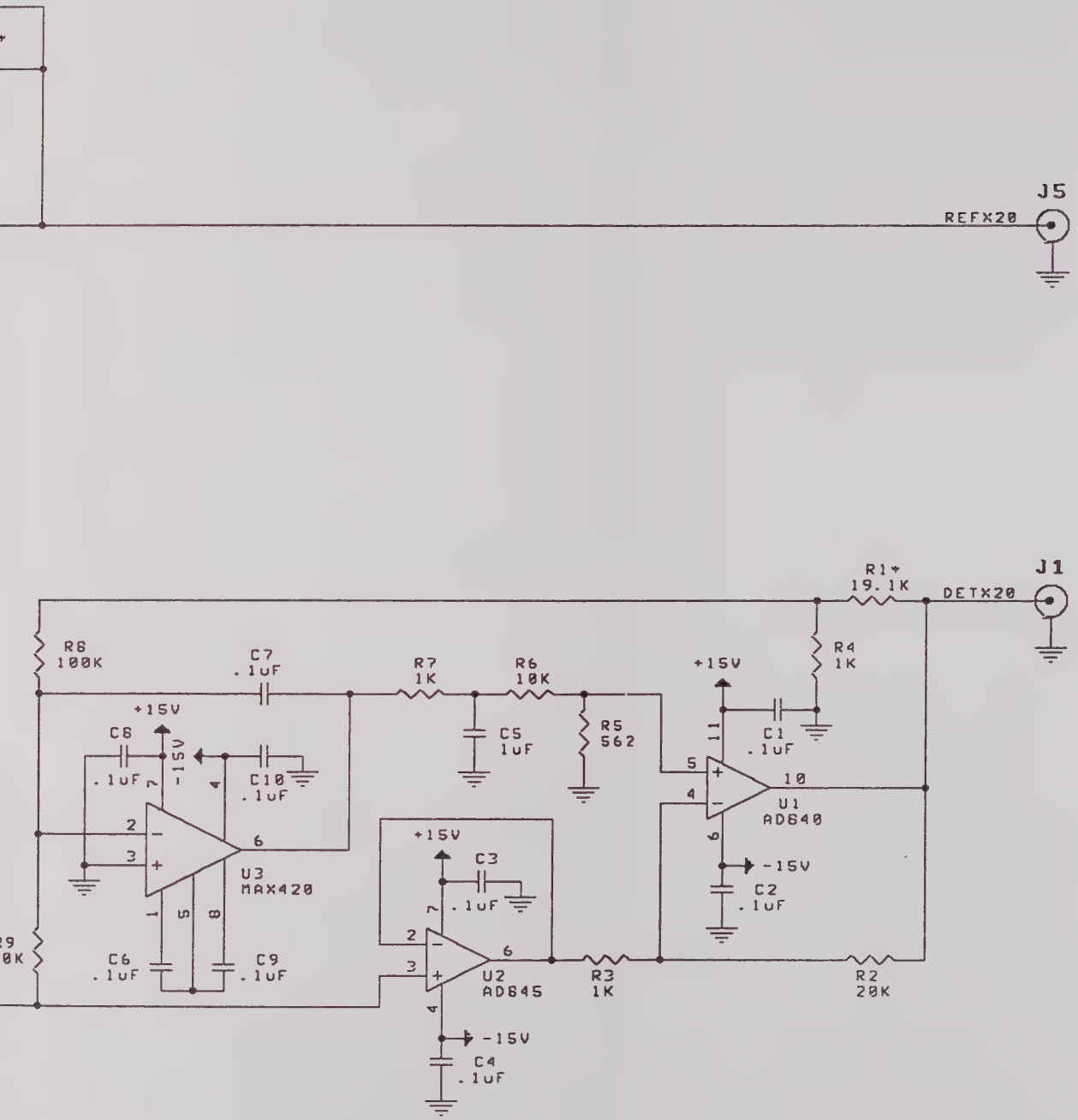


## DETECTOR BUFFER -- PC ASSY A200

The Detector Buffer module is an important part of the leveling system. The 2.5 MHz Reference signal is received from the level board (A10) at J7. This signal is detected by a detector at J6 and a DC voltage proportional to the power level of the reference signal is returned. L1, L2, C15 and C16 filter the reference signal from the DC voltage returned from the detector which is then amplified by U5 and returned to the leveling board thru J5.

The detector inputs for leveling the instrument's output signal are at J4, J3, J2 which are for an external detector (external ALC mode), the <2 band detector and >2 band detector respectively. The appropriate detector is selected by its respective logic line which switches one of 3 comparators (U4 A, C and D) which in turn switches on one FET Q2, Q4 or Q5. The turned on FET allows the proper detector signal to be fed to the amplifier consisting of U3, U2 and U1. The output is then fed back to the leveling board (A10). The remaining logic signal at P4 serves two purposes. When it is low it turns on the FET Q1 which allows the full voltage of the External Detector signal to be applied to Q2. When the logic is high the External Detector voltage is divided down by a factor of 10. The other function this logic line serves is to switch in a capacitor (when the logic is low) in the <2 path to filter out the RF signal which is coming in on the detector voltage. This logic signal remains low from 10 MHz to 50 MHz and then above 50 MHz it goes high which switches the capacitor out of the <2 detector path.

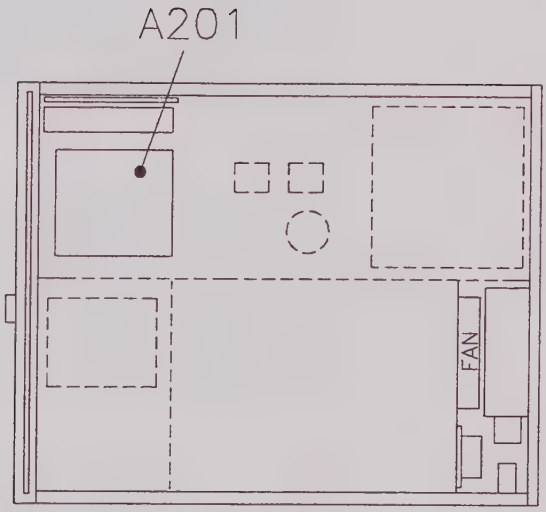

P1
+5V
+5V
C16
47uF 25V
P2
-15V
P2
-15V
C19
47uF 25V
P3
+15V
P3
+15V
C20
47uF 25V
J7
REFSIG
C14
.001uF
L1
1200uH
L2
1200uH
R14
1K
R16
665
+5V
C16
.0015uF
C15
.001uF
C17
Cxx
+15V
C12
.1uF
U5
ADOP37
-15V
C13
.1uF
J6
REFDET
R22
10K
U4:B
LM2901
P4
DETSLOUN
GND
Q1
SD214
-15V
J4
EXTDET
R11
9.09K
R10
1K
Q2
SD214
U4:C
LM2901
R18
100K
+15V
P7
EXT
J3
<2 DET
C21
220pF
Q3
SD214
L3
10uH
R13
402
+15V
R19
100K
-15V
Q4
SD214
U4:D
LM2901
R20
100K
+15V
-15V
C11
.01uF
P6
<2D
J2
>2 DET
L4
10uH
R12
402
R23
10K
Q5
SD214
U4:A
LM2901
R21
100K
+15V
-15V
C22
.01uF
P5
>2D
NOTES: U
1.1 CAPAC
2.1 RESIST
3.1 RESIST
4.1 ▼ 1MΩ



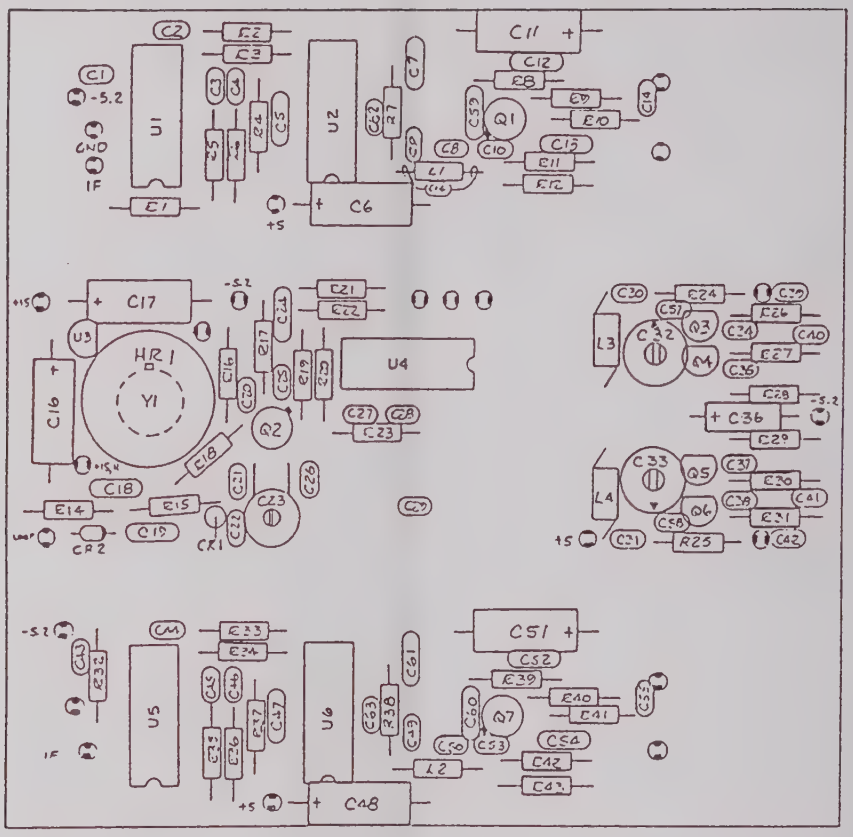

LESS OTHERWISE SPECIFIED

TOR VALUES ARE IN uF
OR VALUES ARE IN OHMS
ORS ARE 1/5W, 1%
ICATES 1/4W 1% RESISTOR

**Detector Buffer (A200)**
**ASSY# 120BA07900 Rev D**
**Sheet 3 of 3**
**7-A200-3**




**100 MHz Reference Osc (A201)**
**ASSY# 101CA04200 Rev T**




**100 MHz Reference Osc (A201)**
**ASSY# 101CA04200 Rev T**
**Sheet 2 of 4**
**7-A201-2**

## 100 MHz OSCILLATOR/SAMPLER DRIVER -- PC ASSY A201

### GENERAL

This module includes a 100 MHz Voltage Controlled Crystal Oscillator that is used to drive the sampling mixers, and two identical amplifier circuits that are used to increase the low level IF from those mixers to ECL voltage levels.

### 100 MHz OSCILLATOR

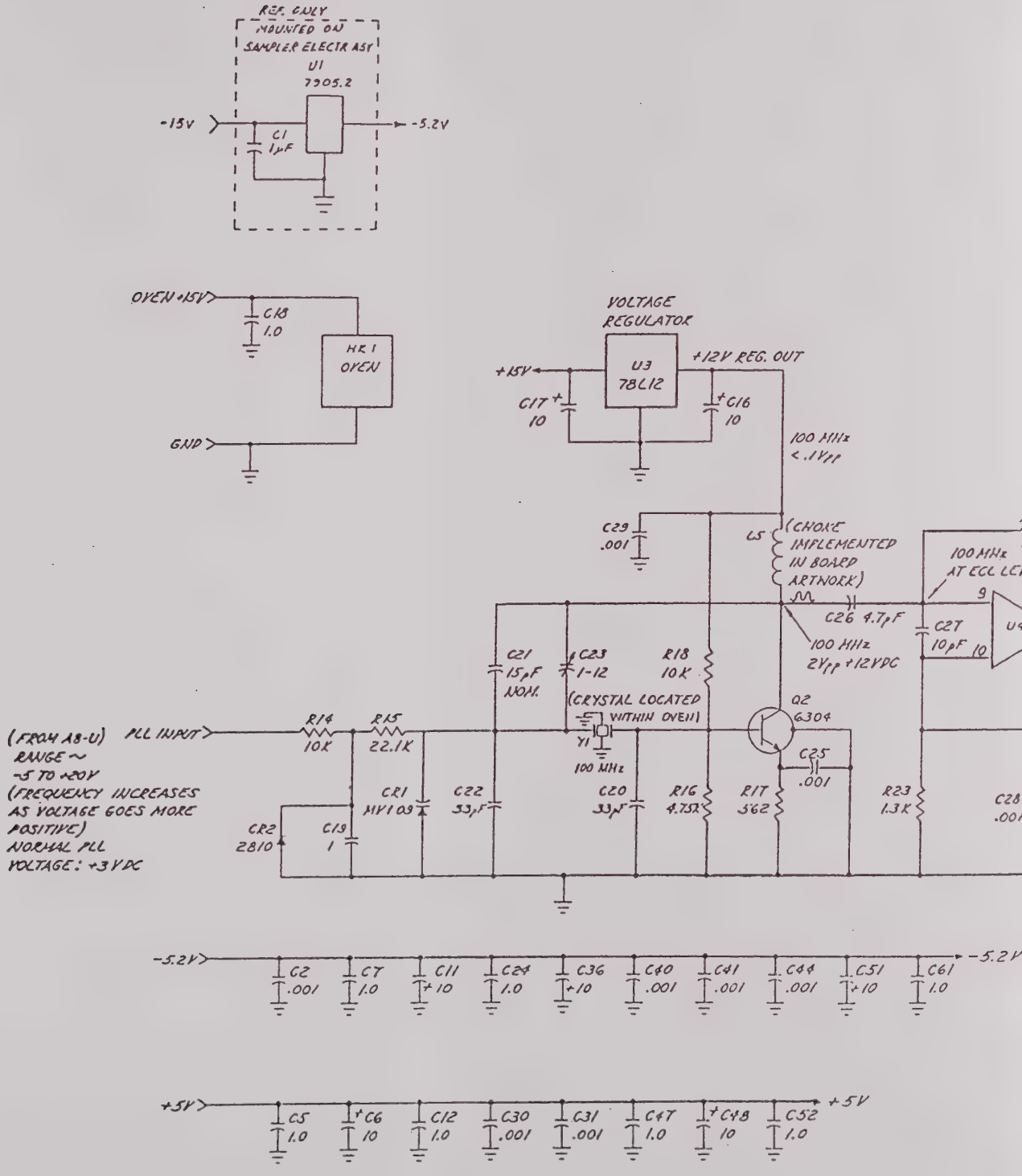
Transistor Q2, regulated by crystal Y-1, oscillates at a frequency very near 100 MHz. This frequency can be varied slightly by changing the Phase Lock Loop input voltage (and thus changing the capacitance of tuning diode CR1). This variation permits the oscillator to be phase-locked to the Master Reference. In order to bring the oscillator frequency within the relatively narrow adjustment range of the PLL circuit, nominal capacitor C21 is selected during production test, and variable capacitor C23 is adjusted during calibration. With the circuit correctly set up, the 100 MHz loop should become locked with a PLL voltage of +3V DC (this voltage is most easily measured at the Test Point on PC Assy A8, the 100 MHz PLL). Buffer IC4 produces four 100 MHz outputs; two are used to drive the sampling mixers, one returns to the 100 MHz PLL, and one is used to supply a stable 100 MHz reference to the Frequency Counter and/or the 10-12 MHz PLL (1 kHz Resolution Circuit), if installed.

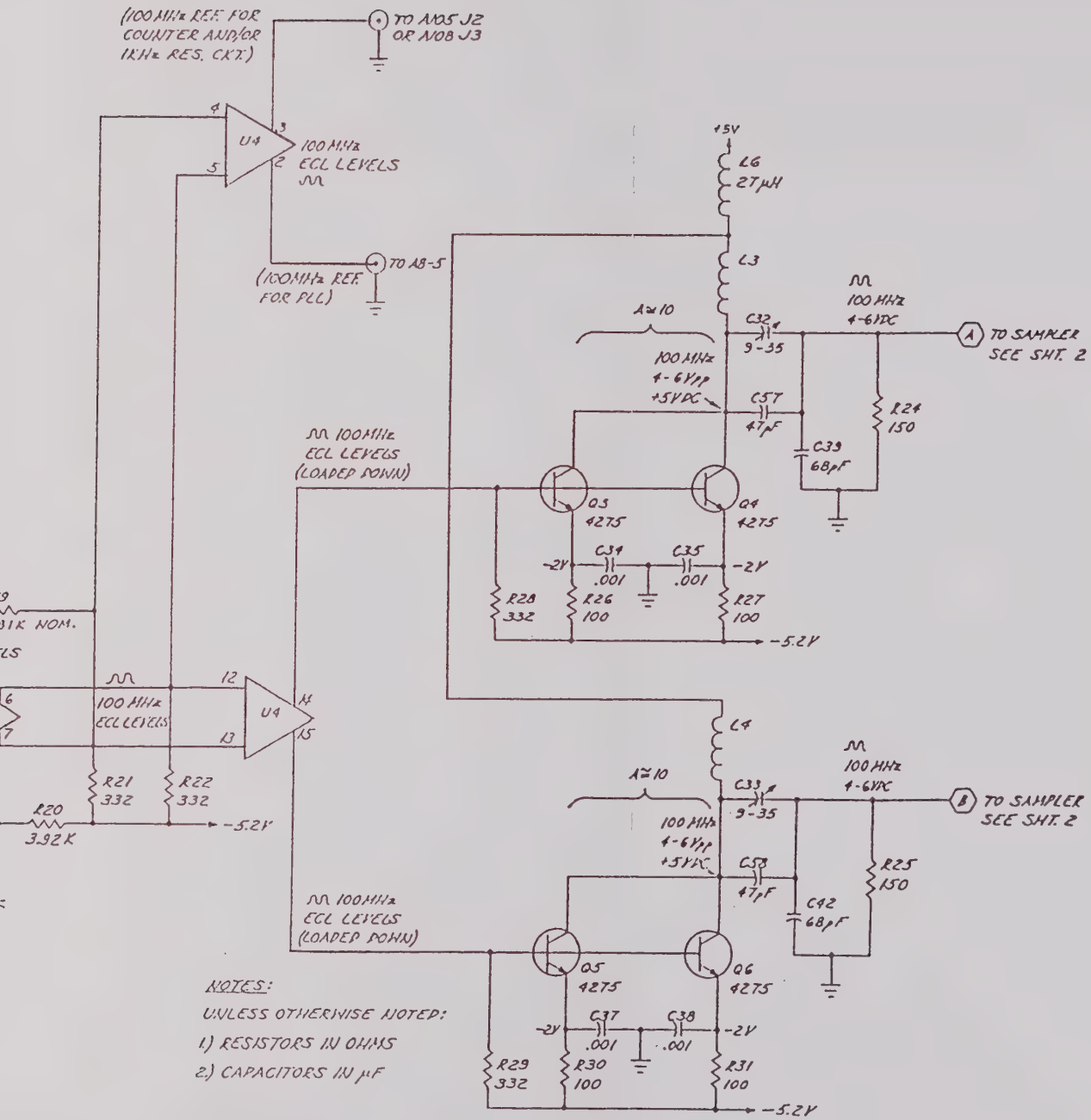
### SAMPLER DRIVE

The twin amplifier circuits (Q3-Q4 and Q5-Q6) are used to supply a large (4-6 Vpp) 100 MHz signal to the sampling mixers. Variable capacitors C32 and C33 are used for peaking this signal. The sampling mixers include a step-recovery diode multiplier, which produces numerous harmonics of the 100 MHz input. The RF input to the sampler is mixed with these high frequencies, one of which will be near enough to it in frequency to create an IF that is within the bandwidth of the Sampler IF Amplifier. Example: For an RF input to the sampler of 6905 MHz, the sampler will mix the 69th harmonic of 100 MHz (6900 MHz) with the RF input and produce a 5 MHz IF output.

### SAMPLER IF AMPLIFIER

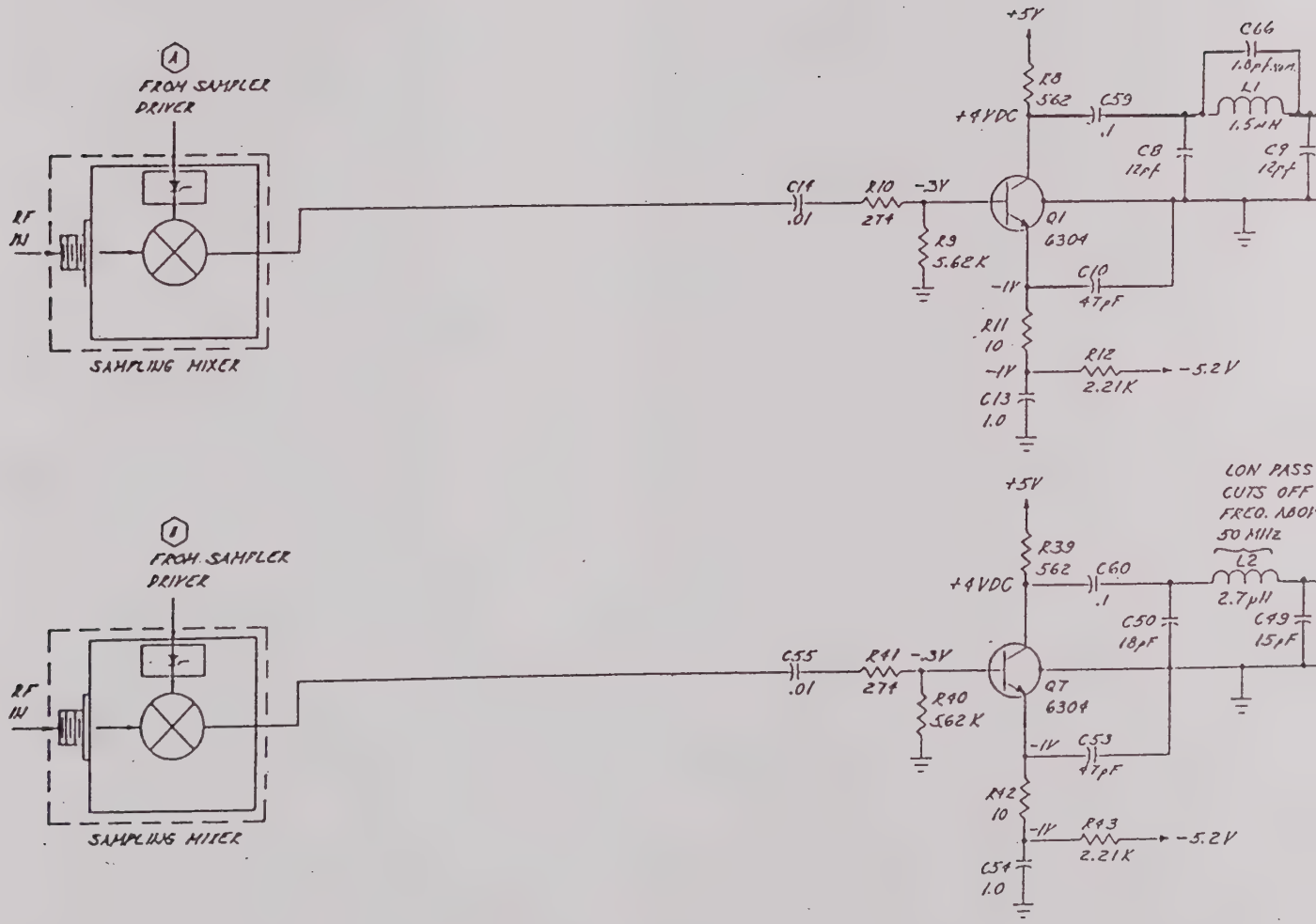
The twin amplifier circuits (Q1-IC2-IC1 and Q7-IC6-IC5) convert the low level IF produced by the samplers to ECL-level signals. Between the transistor amplifier stage and the video amplifier (IC2/IC6) is a low-pass filter that limits the bandwidth to 50 MHz, in order to block undesired high frequencies produced by the mixer. Low frequency noise is blocked by capacitors C62 and C63. The buffers (IC1/IC5) convert the IF to an ECL-level signal for use by the Reference PLL and Downconverter PLL circuits. The IF will be 5 MHz or 1.667 MHz, depending on the RF frequency input to the sampling mixer.

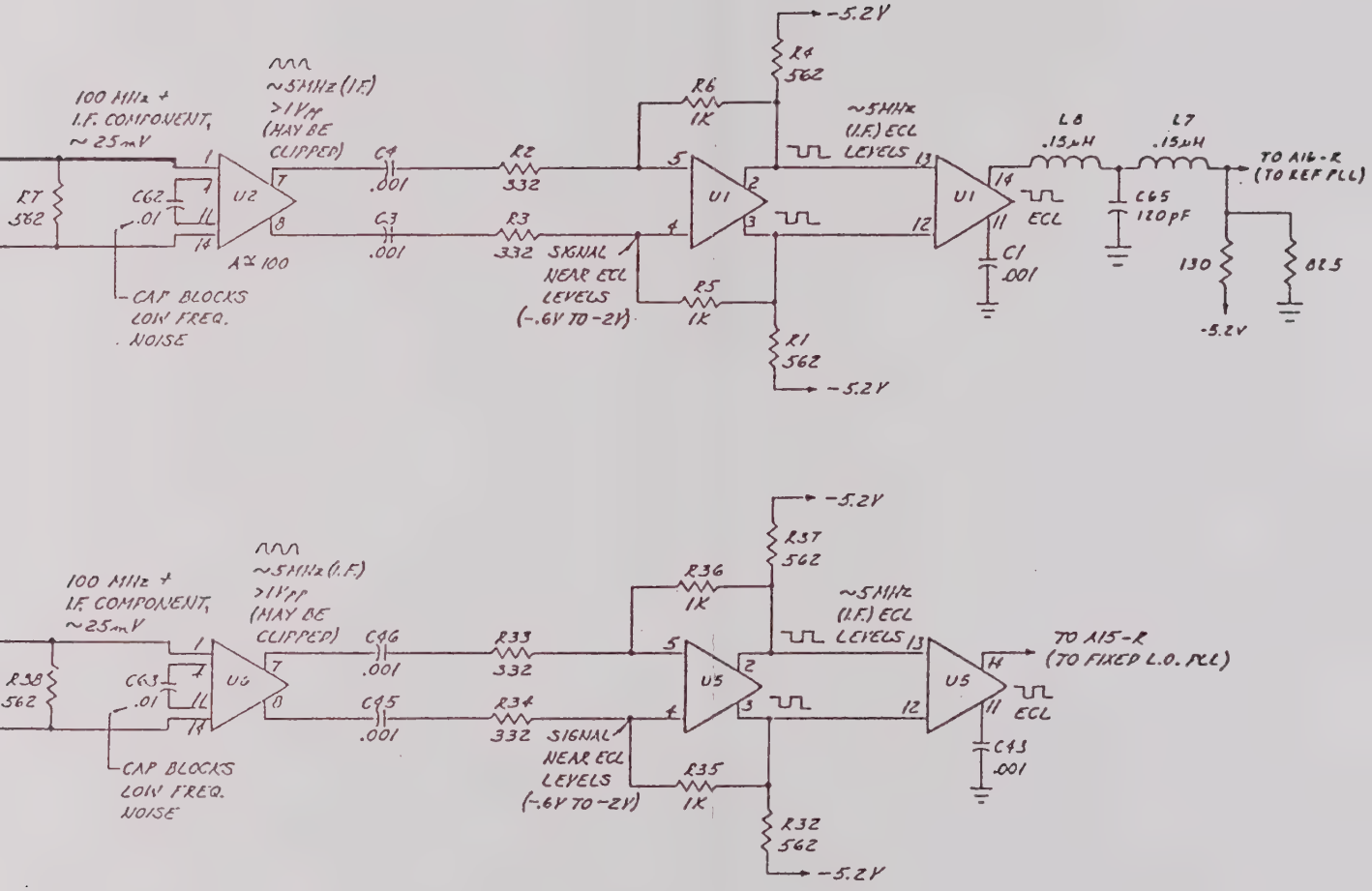

REF. ONLY
MOUNTED ON
SAMPLER ELECTR ASY
U1
7905.2
-15V
C1
1μF
-5.2V
OVEN +15V
C18
1.0
HR1
OVEN
GND
VOLTAGE
REGULATOR
U3
78L12
+15V
C17
10
C16
10
+12V REG. OUT
100 MHz
<.1Vpp
C29
.001
L5
(CHOKE
IMPLEMENTED
IN BOARD
ARTWORK)
100 MHz
AT ECL LEV
C26 4.7pF
C27
10pF
10
100 MHz
2Vpp +12VDC
C21
15pF
NOM.
C23
1-12
R18
10K
(CRYSTAL LOCATED
WITHIN OVEN)
Q2
G304
(FROM A8-U)
RANGE ~
-5 TO +20V
(FREQUENCY INCREASES
AS VOLTAGE GOES MORE
POSITIVE)
NORMAL PLL
VOLTAGE: +3VDC
PLL INPUT
R14
10K
R15
22.1K
Y1
100 MHz
C25
.001
CR1
MV1409
C22
33pF
C20
33pF
R16
4.75K
R17
562
R23
1.3K
C28
.001
CR2
2810
C19
1
-5.2V
C2
.001
C7
1.0
C11
10
C24
1.0
C36
10
C40
.001
C41
.001
C44
.001
C51
10
C61
1.0
-5.2V
+5V
C5
1.0
C6
10
C12
1.0
C30
.001
C31
.001
C47
1.0
C48
10
C52
1.0
+5V




| IC # | TYPE | PIN # -5.2 V | PIN # GND | PIN # +5 V |
|---|---|---|---|---|
| 1, 4, 5 | 10216 | 8 | 1-16 | — |
| 2, 6 | UA733 | 5 | — | 10 |

**100 MHz Reference Osc (A201)**
**ASSY# 101CA04200 Rev T**
**Sheet 3 of 4**
**7-A201-3**


A
FROM SAMPLER DRIVER
RF IN
SAMPLING MIXER
C14 .01
R10 274
-3V
R9 5.62K
+5V
R8 562
+4VDC
C59 .1
C66 1.0pf.var.
L1 1.5nH
C8 12pf
C9 12pf
Q1 6304
C10 47pF
-1V
R11 10
R12 2.21K
-5.2V
C13 1.0
B
FROM SAMPLER DRIVER
RF IN
SAMPLING MIXER
C55 .01
R41 274
-3V
R40 5.62K
+5V
R39 562
+4VDC
C60 .1
LOW PASS CUTS OFF FREQ. ABOVE 50 MHz
L2 2.7μH
C50 18pF
C49 15pF
Q7 6304
-1V
C53 47pF
R42 10
R43 2.21K
-5.2V
C54 1.0




**100 MHz Reference Osc (A201)**
**ASSY# 101CA04200 Rev T**
**Sheet 4 of 4**
**7-A201-4**

# 8 Options

The following options are available for Model GT 9000S, and are discussed under separate headings:

Option 16: 1 Hz Resolution

Option 22: Rear Panel RF Output Connector

Option 24: Internal Modulation, AM & FM Modes

Option 25: Planar Crown RF Output Connector

Option 26: 10 dB Step Attenuator

Option 27: Scan Modulation

Option 28: High Stability Timebase ($5 \times 10^{-10}$/day)

## 8.1 OPTION 16: 1 Hz RESOLUTION

If Option 16 is installed, the frequency resolution of the instrument is 1 Hz.

No special hardware is required for Option 16; 1 Hz resolution is implemented by means of modifications to installed firmware.

## 8.2 OPTION 22: REAR PANEL RF OUTPUT CONNECTOR

If Option 22 is installed, the RF output connector is relocated to the rear panel of the Model GT 9000S. This option may reduce RF output power by as much as 2 dB.

The components required for Option 22 are listed on page 6-12.

## 8.3 OPTION 24: INTERNAL MODULATION, AM & FM MODES

This option provides two built-in function generators for creating AM and FM envelopes (the built-in pulse generator for pulse modulation is standard equipment in Model GT 9000S).

This option has been incorporated into the main body of the manual; where a procedure or specification applies only to instruments with Option 24, a note to that effect is included.

The components required for Option 24 are listed on page 6-12.

## 8.4 OPTION 25: PLANAR CROWN RF OUTPUT CONNECTOR

If Option 25 is installed, the RF output connector is replaced by a Planar Crown Universal Connector, manufactured by Lucas Weinschel. This is a two-part connector; the components are referred to as the planar bulkhead and the planar crown. The bulkhead is a 2.9 mm female connector, mounted inward of the front panel, which is common to all implementations of Option 25 (see the Option 25 parts list on page 6-13). The crown is attached to the bulkhead on the outward side of the front panel, and is available in a variety of versions, as shown in the table below:

| Giga-tronics Part# | Weinschel Part# | Connector Type | Frequency Range (GHz) |
|---|---|---|---|
| JRWC-00030 | 7005-3 | type N female crown | DC to 18 |
| JRWC-00040 | 7005A-4 | type N male crown | DC to 18 |
| JRWC-00050 | 7005A-5 | type GPC-7 crown | DC to 18 |
| JRWC-00080 | 7005A-8 | type TNC female crown | DC to 18 |
| JRWC-00090 | 7005A-09 | type TNC male crown | DC to 18 |
| JRWC-00010 | 7005A-1 | type SMA female crown | DC to 26.5 |
| JRWC-00020 | 7005A-2 | type SMA male crown | DC to 26.5 |
| JRWC-00060 | 7005A-6 | 3.5 mm female crown | DC to 34 |
| JRWC-00070 | 7005A-7 | 3.5 mm male crown | DC to 34 |
| JRWC-00100 | 7005A-10 | 2.92 mm female crown | DC to 40 |
| JRWC-00110 | 7005A-11 | 2.92 mm male crown | DC to 40 |

## *8.5* OPTION 26: 10 dB STEP ATTENUATOR

Under this option, an attenuator is placed in the RF output path of the instrument, which provides up to 110 dB of attenuation in 10 dB increments.

This option has been incorporated into the main body of the manual; where a procedure or specification applies only to instruments with Option 26, a note to that effect is included.

The components required for Option 26 are listed on page 6-13.

## 8.6 OPTION 27: SCAN MODULATION/LINEAR AM

In instruments with Option 27, a scan modulator (a FET-based variable attenuator) is placed in the RF path, between the level control system and the output step attenuator. This modulator is digitally controlled and linearized, and can operate in Scan mode (DC coupled, with depth specified in dB) or Linear AM mode (AC coupled, with depth specified in per cent).

The modulator can also be used as a variable attenuator; attenuation values entered (in dB) are relative to the power level set by the instrument's level control system (if the instrument's level is set to -10 dBm, and a variable attenuation value of -12 dB is specified, the instrument's actual output level will be -22 dBm).

All modes of scan modulation can be operated simultaneously with pulse modulation and frequency modulation.

Installation of Option 27 may degrade the maximum output level by as much as 2 dBm when not activated, and by as much as 7 dBm when activated. Also, standard amplitude modulation (the specifications for which are given in Section 1 of the manual) is not available in instruments with Option 27.

*SPECIFICATIONS (General)*

| | |
|---|---|
| FREQUENCY OF OPERATION: | From 100 MHz to 20 GHz, in .01-20 GHz instruments; across the entire frequency range in other instruments. |
| RF CARRIER HARMONICS: | Not specified. |

*SPECIFICATIONS (DC Coupled 'Scan' Mode, or Variable Attenuator mode)*

| | |
|---|---|
| RANGE: | 0 to 60 dB |
| FREQUENCY RESPONSE: | DC to 150 kHz, sine wave |
| STEP RESPONSE: | <1 µs, for 50 dB change |
| LINEARITY (at cal points): | ±.6 dB (0 to 20 dB);<br>±1 dB (20 to 60 dB). |
| SENSITIVITY: | -10 dB/V |
| INPUT IMPEDANCE: | 50 Ω, nominal |

*SPECIFICATIONS (AC Coupled 'Linear AM' Mode)*

| | |
|---|---|
| MODULATION DEPTH: | 0 to 90% |
| MODULATION BANDWIDTH: | 10 Hz to 50 kHz, ±3dB |
| INPUT SENSITIVITY: | 1 Vpp, for 50% depth ±10% depth, at 1 kHz |
| INPUT IMPEDANCE: | 50 Ω, nominal |

*INTERNALLY GENERATED SCAN/AM ENVELOPE*

| | |
|---|---|
| WAVEFORM: | sine, square, or triangle wave |
| RATE: | 1 Hz to 100 kHz |
| RESOLUTION: | 1 Hz |
| ACCURACY: | ±0.01 Hz |

### 8.6.1 Option 27 Front Panel Operation

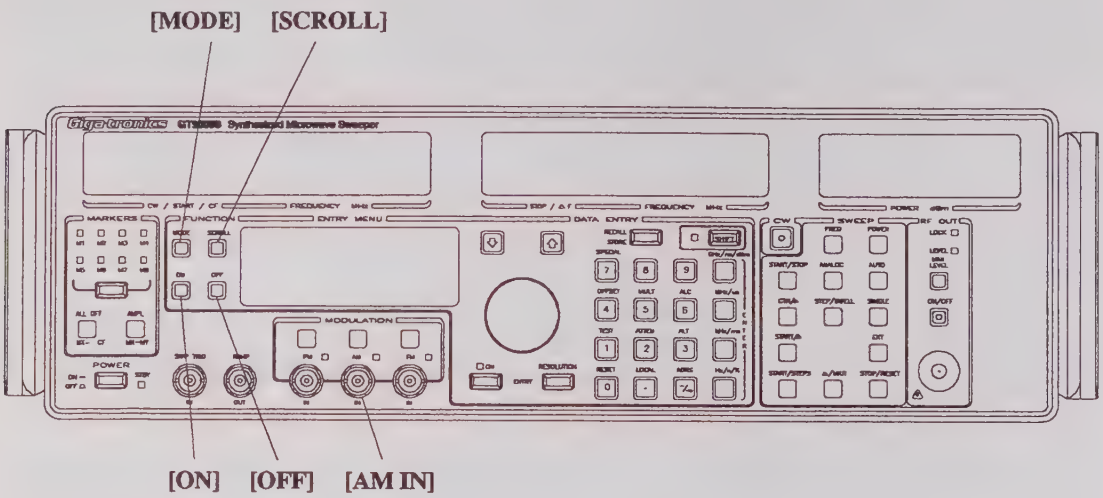



*Figure 8.1: Scan/AM modes*

To select any of the modulation modes provided under Option 27, press **[AM]**. The entry menu display should read 'SCAN EXT: OFF'. This indicates that Scan mode is selected but is presently turned off; use the **[ON]** button to activate this mode. Scan modulation requires an external input, which must be supplied to the 'AM' input BNC connector on the front panel.

To select any of the Scan modes, press the **[MODE]** button until the desired mode is displayed. The choices are:

SCAN EXT = scan modulation, external
LIN AM EXT = linear AM, external
VAR ATTN = variable attenuation

If Option 24 (internal modulation) is also installed, there are six additional modes:

SCAN SIN = scan modulation, internal, sine wave
SCAN SQR = scan modulation, internal, square wave
SCAN TRI = scan modulation, internal, triangle
LIN AM SIN = linear AM, internal, sine wave
LIN AM SQR = linear AM, internal, square wave
LIN AM TRI = linear AM, internal, triangle

Having reached the desired mode, you may set parameters under that mode, pressing the **[SCROLL]** button if necessary until the desired parameter is displayed. Parameter settings may be entered by means of the numeric keypad, or adjusted by means of the digi-dial or the up/down arrow keys.

No parameters are settable under external modulation. Depth (in dB) is settable under variable attenuation. Under all six of the internal modulation modes, rate is settable in Hz; depth is settable in dB (for scan modulation) or in per cent (for linear AM).

### 8.6.2 Option 27 Theory of Operation

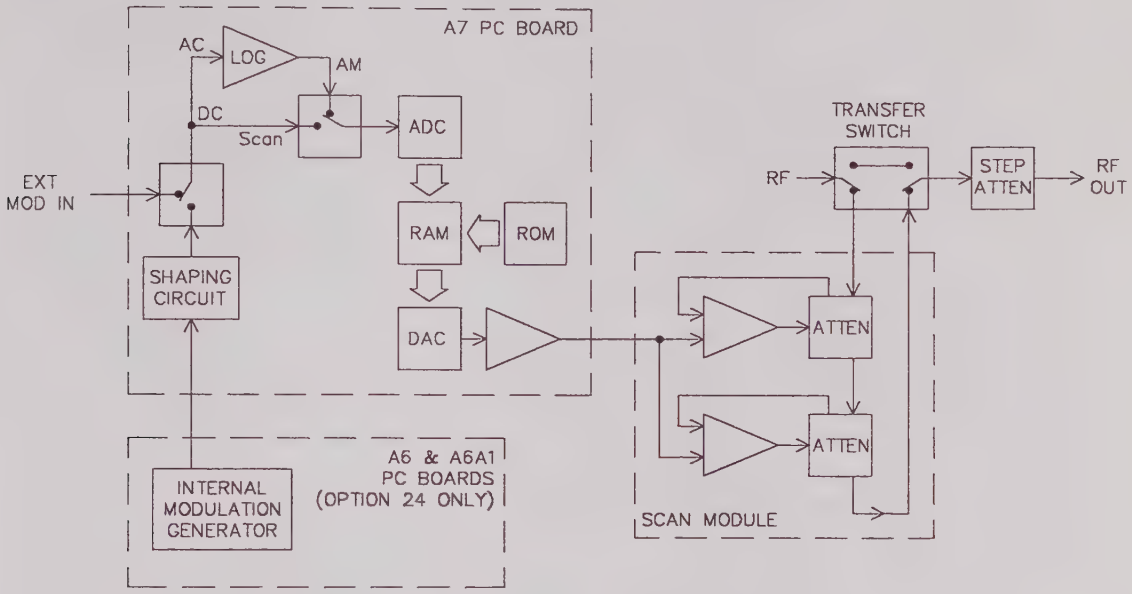



*Figure 8.2: Scan modulation*

The modulating waveform can be applied from an external source, or (if Option 24 is installed) generated internally. Internal modulating signals are transmitted through a shaping circuit which adapts them to the input requirements of the scan circuit. The modulating signal is then applied, through a switch, to either of two input paths: a DC-coupled path for the 'scan' mode or 'variable attenuator' mode, and an AC-coupled path (including a logarithmic amplifier) for the 'linear AM' mode.

The modulation input is applied to an analog-to-digital converter, and converted to a binary number. This number (in the form of a set of parallel data lines) is applied to the address bus of a RAM. The RAM is loaded with correction data stored in ROM (there are several tables of correction data in ROM, for different frequency ranges; the appropriate table is loaded into RAM when Scan modulation is selected or when the frequency changes). When the RAM is addressed by the output of the ADC, the data stored at the relevant address is furnished to the input of a digital-to-analog converter. The DAC converts this correction data to an analog signal which drives the scan module. As the input waveform changes, different storage areas in the RAM are addressed, so that the correction factors retrieved from memory constantly track the input. The correction data is tailored to the individual scan module installed in the instrument; it is needed to linearize the response of that module to the modulation input.

The scan module contains a pair of voltage controlled attenuator circuits; each has a dynamic range of 30 dB, and since they are placed in series, the dynamic range of the whole is 60 dB. Each attenuator is driven by a loop amplifier which provides correction of its attenuator's response (the first corrects for linearity, the second for input/output impedance matching).

During modulation, the two variable attenuators of the scan module are switched into the RF output path of the instrument. The modulating input to the scan module controls the attenuation, and therefore the RF output level. When modulation is deactivated, this module is switched out of the RF path.

### *8.6.3* Option 27 Acceptance Test Procedure (Linear AM Mode)

1. Select 'AMf EXT: ON'.
2. Connect the Model GT 9000S RF output to a mixer box, as shown in the illustration. On the 8902, select 50 Hz and 15 kHz filters, AM mode. Set the GT 9000S RF output frequency to 5 GHz. Using a BNC 'T' connector and oscilloscope, apply a 1.0 Vpp, 1 kHz sine wave to the 'SCAN' input BNC on the GT 9000S rear panel.
3. Measure the percentage of distortion at 1 kHz; verify that distortion is $\leq$ 5%.
4. Increase the input modulation to obtain 80% AM. Verify that distortion is < 5%.
5. Check the distortion at 30% and 80% modulation at the following frequencies: 1 GHz, 5 GHz, 15 GHz, and 22 GHz.
6. Disconnect external modulation. Select 'AMfSIN: ON', 1 kHz rate, 50% depth. Using 8902A, measure AM%. Verify a modulation reading of 47 to 53%. Verify a distortion reading of <5% at 1 kHz.
7. Select 'AMfSQR: ON', 50% depth. Turn off all filters on 8902A. Verify an AM% reading of 45 to 55% on 8902A.
8. Select 'AMfTRI: ON', 50% depth. Turn on 50 Hz and 15 kHz filters on 8902A. Verify an AM% reading of 47 to 53% on 8902A.
9. Connect a detector to Model GT 9000S RF out. Connect detector output to scope, channel B, 50 Ω on. Set scope to 2 mV and 200 µsec.
10. Select 'AMfEXT: ON'.
11. Apply a 1 Vpp, 1 kHz sine wave to the 'SCAN' input BNC. Adjust the channel B input vernier for a display of the waveform that spans six vertical divisions.
12. Adjust the external modulation rate for 10 Hz; verify that the displayed waveform has an amplitude of >4 divisions on the scope. Vary the rate from 10 Hz to 100 kHz, and verify that the waveform amplitude maintains an amplitude of $\geq$4 divisions.

### *8.6.4* Option 27 Acceptance Test Procedure (Scan Mode)

1. Apply a 0-1 V (10 dB depth) sine wave to the 'SCAN' input BNC.
2. Select 'SCAN EXT: ON'.
3. Connect a detector to the Model GT 9000S RF output, and connect the output of the detector to the oscilloscope (channel B, 50 Ω on). Set oscilloscope to 2mV, 200 µsec, and adjust the channel B input vernier for a display of the waveform that spans six vertical divisions.
4. Vary the external modulation rate between 1 kHz and 300 kHz; verify that the displayed waveform maintains a minimum amplitude of 4 vertical divisions.
5. Set the modulation rate to 50 kHz, square wave. Compare the input modulation rising edge with the detector output rising edge; verify that the delay is less than 800 nsec.
6. Compare the input modulation falling edge with the detector output falling edge; verify that the delay is approximately 1 µsec.
7. Connect the Model GT 9000S RF output to the spectrum analyzer. Set the RF output frequency to 1 GHz. Set the analyzer span to 5 MHz and center the 1 GHz signal on the screen. Set the span to 0 Hz. Apply a 0-4V sine wave to the 'SCAN' input BNC. Verify a 0 to -40 dB sine wave on the analyzer. Change the input sine wave to 0-2V; verify a 0 to -20 dB sine wave on the analyzer. Change the input sine wave to a triangle wave and square wave; verify clean waveforms on the analyzer screen from 0 to -20 dB.

### *8.6.5* Option 27 Calibration

1. Select 'AMfEXT: ON', but *do not* apply a modulating signal.
2. Measure TP3 on the Scan Modulation PC board (A7), and verify a DVM reading of +2.5 V, $\pm$.05 V.

3. Move the jumper on P1-1 and P1-6 to P1-2 and P1-5.
4. Adjust the Zero pot (R14) for a DVM reading of 0.0 VDC on TP1.
5. Move the jumper on P1-2 and P1-5 to P1-3 and P1-4.
6. Adjust the Gain pot (R19) for a DVM reading of +6.0 VDC on TP1.
7. Move the jumper on P1-3 and P1-4 to P1-1 and P1-6.
8. Adjust the Level pot (R25) for a DVM reading of +0.65 VDC on TP1.
9. Connect the Model GT 9000S and test equipment as shown in the illustration. On the 8902, select 50 Hz and 15 kHz filers, AM mode. Set the GT 9000S RF output to 5 GHz.
10. Using a BNC 'T' connector and oscilloscope, apply a 1.0 Vpp, 1 kHz sine wave to the 'SCAN' input BNC on the Model GT 9000S rear panel.
11. Adjust the Sense pot (R4) for a 50.0% reading on the 8902.
12. Measure the distortion at 1 kHz; adjust the Gain pot (R19) for the lowest distortion reading.
13. Check the distortion at the RF output frequencies shown in the following table. Adjust R19 as needed to bring the distortion within the acceptable range at all calibration points.

| ***AM Calibration Points*** | | |
|---|---|---|
| **RF Frequency** | **Distortion at 80%** | **Distortion at 30%** |
| 1 GHz | <5% | <10% |
| 5 GHz | <5% | <10% |
| 15 GHz | <5% | <10% |
| 22 GHz | <5% | <10% |

14. Select 'AMfSQR: ON', depth 50%. Turn off all filters on 8902A, and verify an AM% reading of 45-55% on the 8902A.
15. Select 'AMfTRI: ON', depth 50%. Turn on 50 Hz and 15 kHz filters on the 8902A, and verify an AM% reading of 47-53% on 8902A.

### *8.6.6* Option 27 Assemblies

This option has been incorporated into the main body of the manual; where a procedure or specification applies only to instruments with Option 27, a note to that effect is included.

The components required for Option 27 are listed on page 6-13.

## *8.7* OPTION 28 (HIGH STABILITY TIMEBASE)

When Option 28 is installed, a special timebase oscillator having an aging rate of $5 \times 10^{-10}$/day is substituted for the standard timebase oscillator.

This option has been incorporated into the main body of the manual; where a procedure or specification applies only to instruments with Option 28, a note to that effect is included.

The components required for Option 28 are listed on page 6-13.

# 9 Special Configurations

## 9.1 SPECIAL CONFIGURATIONS

If the instrument is specially configured (as indicated by a three-digit number on the "Config." line of the Model/Serial/Config. sticker), a supplement describing the configuration is added to the manual, beginning on the following page. Modifications of the instrument, its circuits, and its performance characteristics are listed in that supplement.

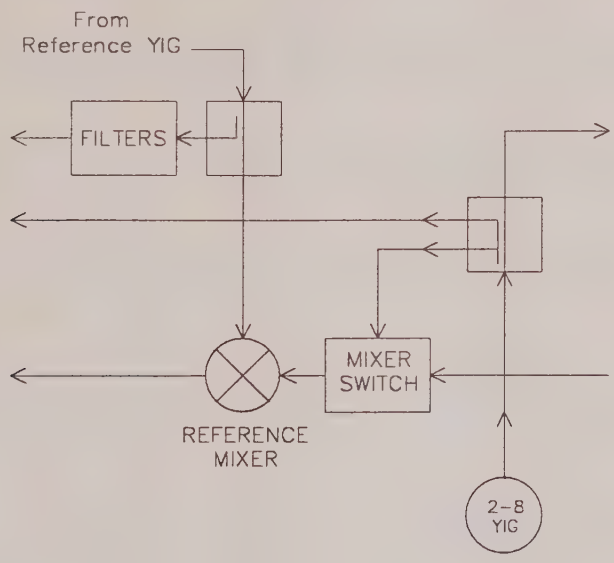
# *Manual Changes Supplement*
# *April 21, 1994*

*This supplement lists any manual errors which were discovered after printing (these are placed under the heading 'Errata'), together with any revisions of circuits or assemblies which were implemented after printing (these are placed under the heading 'Design Changes').*

# *Errata*

***Page 4-3, paragraph 4.2, step 2:***
The test point referred to as 'TP1' should be changed to 'TP4'.

***Page 7-1 (Functional Block Diagram):***
In this diagram, the connections between the Reference YIG coupler, the 2-8 YIG coupler, the reference mixer, and the mixer switch are shown incorrectly. The actual connections are illustrated in the drawing below.



# *Design Changes*

The Pulse Driver PC board (A5) may be changed to Revision C. The circuit is modified as follows: Item 1 is changed from 120CF09303 to 120CF09302. C45 and C47 are changed to 100 pF. C56, and R55 through R59, are deleted.

The Data Entry PC board (A106) may be changed to Revision C. The circuit is modified as follows: R1 is changed to 3.92K (Part# RN55-13920).

The Display Driver PC board (A20) may be replaced by an alternative version (DWG# 120BA01411, Revision A); the parts list and drawings for this circuit are attached.

The Function Generator PC board (A6A1) may be changed to Revision B. This change affects the method of assembly only, and does not modify the circuit as it is described in the manual.

The Level Driver PC board (A10A1) may be changed to Revision B. This change affects the method of assembly only, and does not modify the circuit as it is described in the manual.

The Power Supply PC board (A11) may be changed to Revision B. The circuit is modified as follows: R22 is changed from 3 Ω to a 0 Ω jumper. R23 is changed from 3 Ω to 6 Ω, 3 W (Part# RW03-00060).

The Output PLL PC board (A18) may be changed to Revision B. The circuit is modified as follows: L7 is changed from 820 µH to 150 µH (Part# LADO-07150). R70 is changed from 3.2K to 7.5K (Part# RN50-17500).

The YIG Driver PC board (A19) may be replaced by an alternative version (DWG# 120BA08351, Revision A); the parts list and drawings for this circuit are attached.

In some instruments with Option 26, the 10 dB Step Attenuator (normally a 20 GHz attenuator, Part# MPB0-02001) may be replaced by a 26 GHz attenuator (Part# KP90-02603).

The 100 MHz Reference PLL (14) may be replaced by an alternative version (DWG# 120BA06951, Revision A); the parts list and drawings for this circuit are attached.

The Data Entry PC board (A106) may be changed to Revision D. The circuit is modified as follows: R1 is changed to 5.11K (Part# RN55-15110).

The 1 Hz PLL PC board (A15) may be changed to Revision J. The circuit is modified as follows: R57 is changed to 6.19K, nominal (Part# RN50-16190).

# *Design Changes*

The Display Driver PC board (A20) may be changed to Revision B. The circuit is modified as follows: R10 and R13 are changed to zero ohm jumpers (Part# WJIB-05022).

The Pulse Driver PC board (A5) may be changed to Revision E. This change affects the method of assembly only, and does not modify the circuit as it is described in the manual.

The Level PC board (A9) may be changed to Revision B. The circuit is modified as follows:
R41 is changed from 2K to 1K (Part# RN50-11000).
R51 is changed from Rxx to 51.1 ohms, nominal (Part# RN50-00511).
R66 is changed from 162K to 402K (Part# RN50-34020).
R70 is changed from 1K to Rxx.
R71 is changed from from Rxx to 1K (Part# RN50-11000). U31 is changed from UIDO-07524 to UINO-07524.

The Power Supply PC board (A11) may be changed to Revision C. The circuit is modified as follows:
R22 is changed from 3 Ω to a 0 Ω jumper.
R23 is changed from 3 Ω to 6 Ω, 3 W (Part# RW03-00060).
The following capacitors are changed from .022 uF to .01 uF (Part# CC50-03100): C1 through C5, C7, C8, C9, C12, C13, C15 through C18, C22, C25, C26, C27, C30, C32, C38 through C42.
The following capacitors are changed from .022 uF to 220 pF (Part# CC50-03220): C6, C10, C19, C23, C29, and C33.

Bill of Material (by Ref Designator)

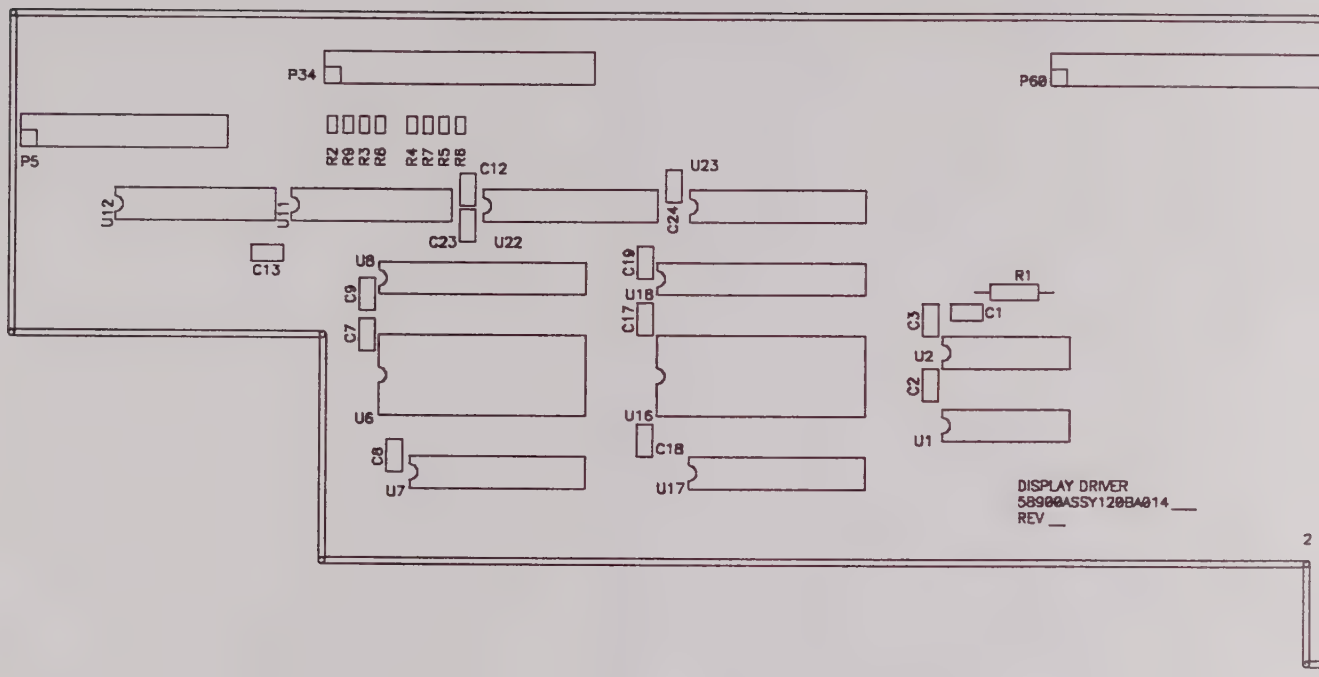
Parts List For: 120BA01411 DISPLAY DRIVER PCA REV: B

| Item | Part Number | Qty | Mfgr | Mfr's Part Number | Description |
|---|---|---|---|---|---|
| 0 | 120BS01411 | 0.000 | | | DISPLAY DRIVER SCH |
| 1 | 120DF01400 | 1.000 | | | DISPLAY DRIVER PCB |
| 2 | HQH1-02200 | 1.000 | THRMLL | THERMALLOY 6073B | TO220 HEATSINK |
| 101 | HBPP-44006 | 1.000 | NYLOK | NS137CR440R6 | 4-40 X 3/8 PAN |
| 102 | HWFN-40400 | 1.000 | | | #4 X 1/4 NYLON WASHER |
| 103 | HNSS-44004 | 1.000 | | | 4-40 HEX NUT |
| 104 | HQWC-01260 | 1.000 | MOT | B52200F006 | TO126 DOME WASHER |
| C 1 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 2 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 3 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 4 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 5 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 6 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 7 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 8 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 9 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 10 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 11 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 12 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 13 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 14 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 15 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 16 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 17 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 18 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 19 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 20 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 21 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 22 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 23 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 24 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 25 | CE16-R7470 | 1.000 | NIC CO | UVX1C471MPA | 470 UF 16V RADIAL LEAD |
| C 26 | CE16-R7470 | 1.000 | NIC CO | UVX1C471MPA | 470 UF 16V RADIAL LEAD |
| C 27 | CC50-05100 | 1.000 | AVX | SR305E105MAA | 1 UF CERAMIC Z5U |
| C 28 | CE25-R6470 | 1.000 | PANSON | ECEA1EU470 | 47 UF 25V RADIAL LEAD |
| C 29 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 30 | CC50-05100 | 1.000 | AVX | SR305E105MAA | 1 UF CERAMIC Z5U |
| L 1 | LR00-08100 | 1.000 | DELEVA | 3443-72 | 1MH INDUCTOR |
| P 1 | JIA1-05295 | 1.000 | MOLEX | 22-11-2052 | 5 PIN LOCKING STRIP PLUG |
| P 2 | JIR1-10260 | 1.000 | MOLEX | 22-12-2104 | 10 PIN LOCKING STRIP PLG |
| P 5 | JIA2-26460 | 1.000 | CIR AS | CA-D26-23B-46 | 26 PIN STRIPLINE PLUG |
| P 9 | JIR1-20034 | 1.000 | BERG/D | 68022-134 | 34 PIN STRPLN PLG RT ANG |
| P 11 | JIR1-20034 | 1.000 | BERG/D | 68022-134 | 34 PIN STRPLN PLG RT ANG |
| P 34 | JIA2-34460 | 1.000 | CIR AS | CA-D34-23B-46 | 34 PIN STRIPLINE PLUG |
| P 60 | JIR1-20060 | 1.000 | BERG/D | 68022-160 DU PON | 60 PIN STRPLN PLG RT ANG |

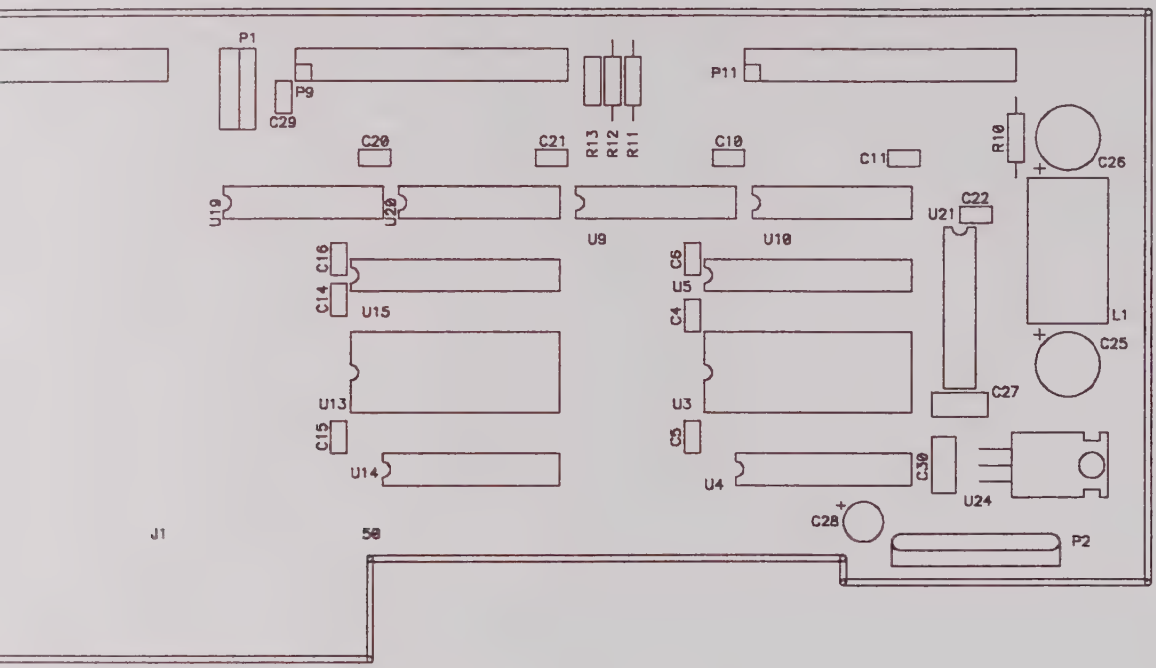
Bill of Material (by Ref Designator)

Parts List For: 120BA01411 DISPLAY DRIVER PCA REV: B

| Item | Part Number | Qty | Mfgr | Mfr's Part Number | Description |
|---|---|---|---|---|---|
| R 1 | RN55-23010 | 1.000 | DALE | RN55C3012F | 30.1 K OHMS 1% MET FILM |
| R 2 | WJIB-02022 | 1.000 | 3M | 923345-02 | .2 INSULATED JUMPER |
| R 3 | WJIB-02022 | 1.000 | 3M | 923345-02 | .2 INSULATED JUMPER |
| R 4 | WJIB-02022 | 1.000 | 3M | 923345-02 | .2 INSULATED JUMPER |
| R 5 | WJIB-02022 | 1.000 | 3M | 923345-02 | .2 INSULATED JUMPER |
| R 6 | WJIB-02022 | 1.000 | 3M | 923345-02 | .2 INSULATED JUMPER |
| R 7 | WJIB-02022 | 1.000 | 3M | 923345-02 | .2 INSULATED JUMPER |
| R 8 | WJIB-02022 | 1.000 | 3M | 923345-02 | .2 INSULATED JUMPER |
| R 9 | WJIB-02022 | 1.000 | 3M | 923345-02 | .2 INSULATED JUMPER |
| R 10 | RN55-00100 | 1.000 | DALE | RN55D10R0F | 10 OHMS 1% MET FILM |
| R 11 | RN55-00150 | 1.000 | AB | RN55C-15R0F | 15 OHMS 1% MET FILM |
| R 12 | RN55-00825 | 1.000 | DALE | RN55C82R5F | 82.5 OHMS 1% MET FILM |
| R 13 | RN55-00100 | 1.000 | DALE | RN55D10R0F | 10 OHMS 1% MET FILM |
| U 1 | UTN0-01322 | 1.000 | TI | MC74HC132E | SN74HC132N 4X SCHMIDT NAN |
| U 2 | UTN0-01971 | 1.000 | TI | SN74LS197N | 74LS197 PRESETTABLE DECA |
| U 3 | UMN0-02128 | 1.000 | SHARP | LH5116-10 | TMM2016 2K X 8 RAM |
| U 4 | UTN0-02442 | 1.000 | TI | SN74HC244N | 74HC244 8X DRIV/RECV |
| U 5 | UTN0-45142 | 1.000 | TI | SN74HC4514NT | 74HC4514 DECODERS/DEMULT |
| U 6 | UMN0-02128 | 1.000 | SHARP | LH5116-10 | TMM2016 2K X 8 RAM |
| U 7 | UTN0-02442 | 1.000 | TI | SN74HC244N | 74HC244 8X DRIV/RECV |
| U 8 | UTN0-45142 | 1.000 | TI | SN74HC4514NT | 74HC4514 DECODERS/DEMULT |
| U 9 | UIN0-00594 | 1.000 | SIG | NE594N | NE594 8X DISP DRIVE |
| U 10 | UIN0-00594 | 1.000 | SIG | NE594N | NE594 8X DISP DRIVE |
| U 11 | UIN0-00594 | 1.000 | SIG | NE594N | NE594 8X DISP DRIVE |
| U 12 | UIN0-00594 | 1.000 | SIG | NE594N | NE594 8X DISP DRIVE |
| U 13 | UMN0-02128 | 1.000 | SHARP | LH5116-10 | TMM2016 2K X 8 RAM |
| U 14 | UTN0-02442 | 1.000 | TI | SN74HC244N | 74HC244 8X DRIV/RECV |
| U 15 | UTN0-45142 | 1.000 | TI | SN74HC4514NT | 74HC4514 DECODERS/DEMULT |
| U 16 | UMN0-02128 | 1.000 | SHARP | LH5116-10 | TMM2016 2K X 8 RAM |
| U 17 | UTN0-02442 | 1.000 | TI | SN74HC244N | 74HC244 8X DRIV/RECV |
| U 18 | UTN0-45142 | 1.000 | TI | SN74HC4514NT | 74HC4514 DECODERS/DEMULT |
| U 19 | UIN0-00594 | 1.000 | SIG | NE594N | NE594 8X DISP DRIVE |
| U 20 | UIN0-00594 | 1.000 | SIG | NE594N | NE594 8X DISP DRIVE |
| U 21 | UIN0-00594 | 1.000 | SIG | NE594N | NE594 8X DISP DRIVE |
| U 22 | UTN0-02442 | 1.000 | TI | SN74HC244N | 74HC244 8X DRIV/RECV |
| U 23 | UTN0-02442 | 1.000 | TI | SN74HC244N | 74HC244 8X DRIV/RECV |
| U 24 | URC0-07805 | 1.000 | MOT | MC7805CT | MC7805CT 1A 5V REG |




**Display Driver (A20)**
**ASSY# 120BA01411 Rev B**
**Sheet 2 of 4**
**7-A20-2**



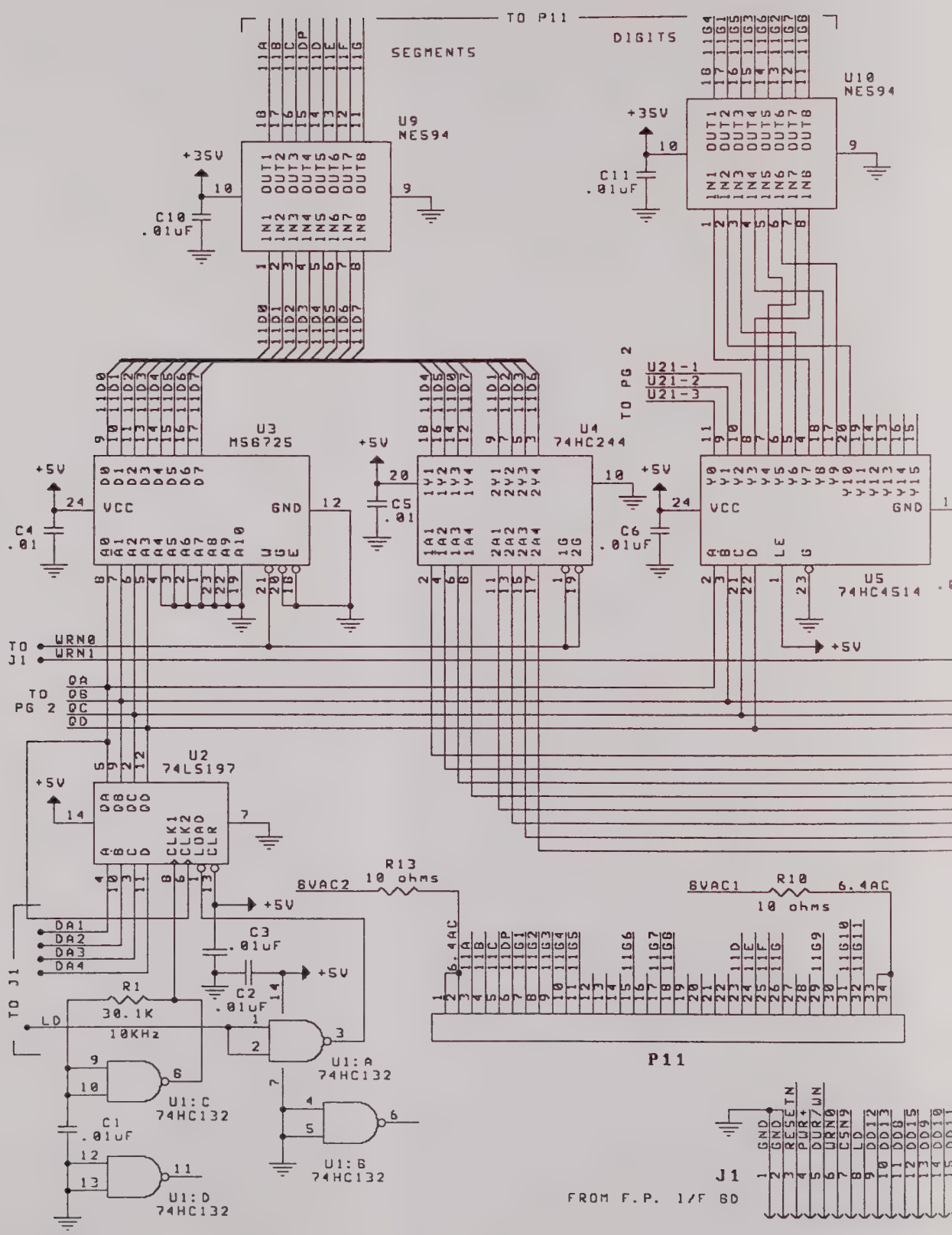

**DISPLAY DRIVER -- PC ASSY A20**

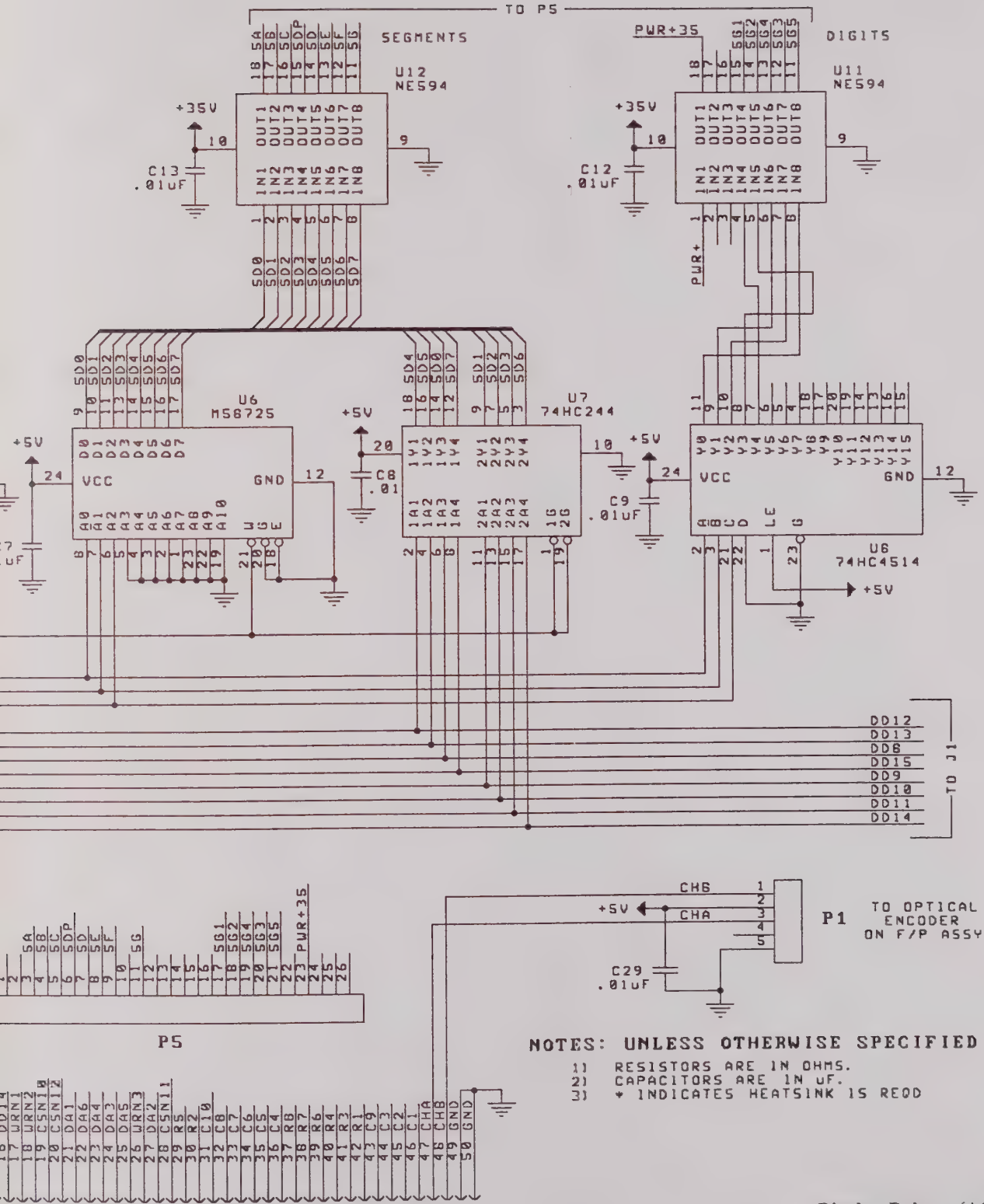
This board holds the necessary circuitry to drive the fluorescent displays and the LEDs on the front panel.

U2 is a counter which is clocked by U1 thereby cycling thru the addresses corresponding to each display digit and its segments. When the computer updates the display or when a setting has been changed, the LD line is activated, and the counter U2 stops counting and outputs the address which is on its A-D inputs, to QA-QD outputs thus addressing the decoders and RAMS when the appropriate chips are selected by the read/write lines. At this time data is available at the input of the latch U4 and can be loaded into the RAM U3. When the data has been updated for all addresses, the LD line becomes inactive and the counter U2 again cycles thru the addresses, selecting data for specific segments to be driven via U9. At the same time decoder U5 decodes the addresses to select each individual digit via U10. This scheme is used to drive all 3 fluorescent displays.

A similar scheme is used for lighting the LEDs on the front panel, the only difference is that they are addressed by rows and columns via U22 and U23 respectively.

U24 regulates +9V to +5V, as required by the front panel alphanumeric displays.

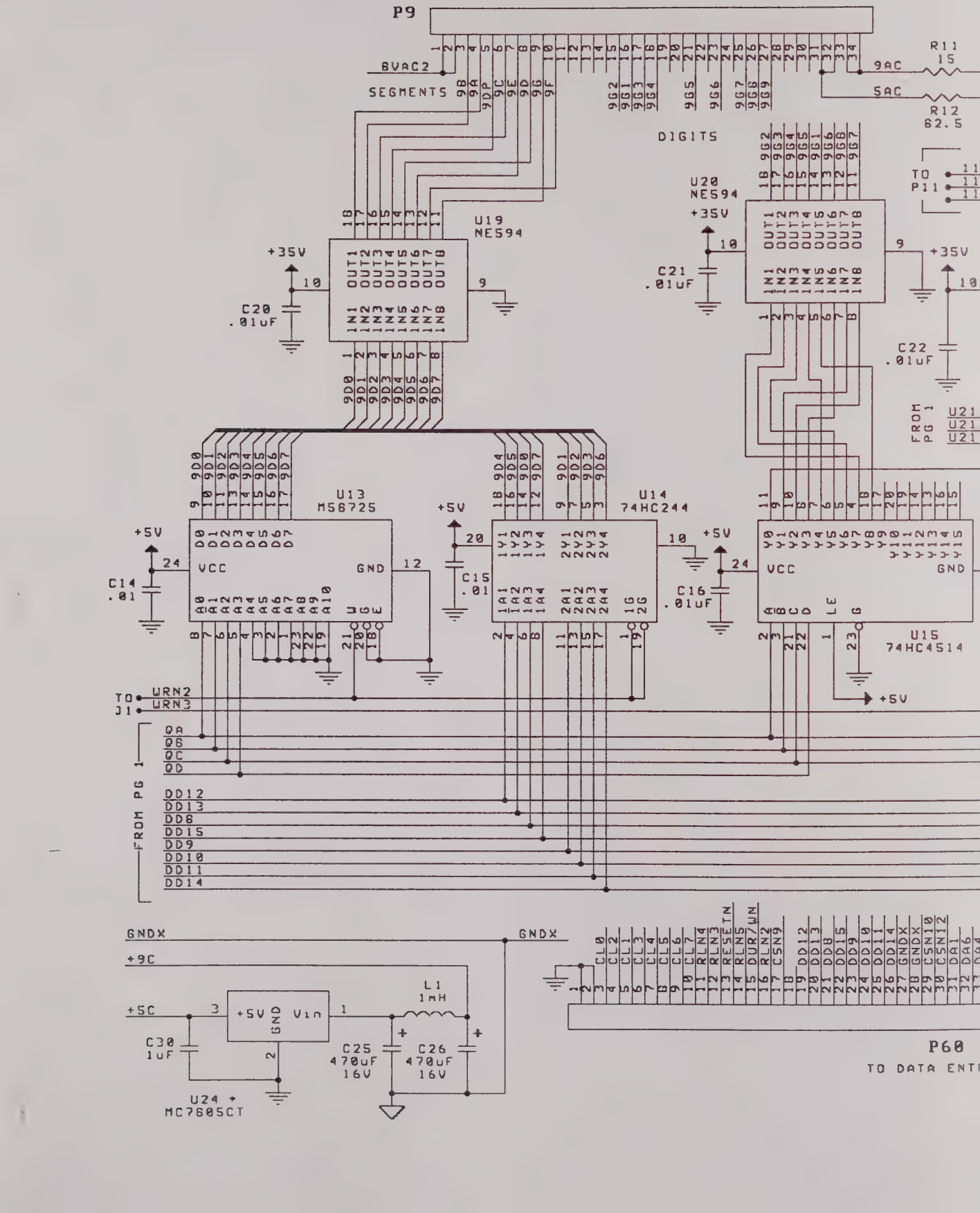

TO P11
SEGMENTS
DIGITS
U9
NE594
U10
NE594
+35V
C10
.01uF
C11
.01uF
U3
M58725
U4
74HC244
U5
74HC4514
U2
74LS197
TO PG 2
U21-1
U21-2
U21-3
+5V
C4
.01
C5
.01
C6
.01uF
VCC
GND
TO J1
WRN0
WRN1
DA
DB
DC
DD
TO PG 2
DA1
DA2
DA3
DA4
R1
30.1K
10KHz
LD
C1
.01uF
C2
.01uF
C3
.01uF
R13
10 ohms
8VAC2
R10
10 ohms
8VAC1
6.4AC
P11
U1:A
74HC132
U1:B
74HC132
U1:C
74HC132
U1:D
74HC132
J1
FROM F.P. I/F BD
GND
RESETN
PWR+
PWR7WN
WRN0
CSN9
LD
DD12
DD13
DD8
DD15
DD9
DD10

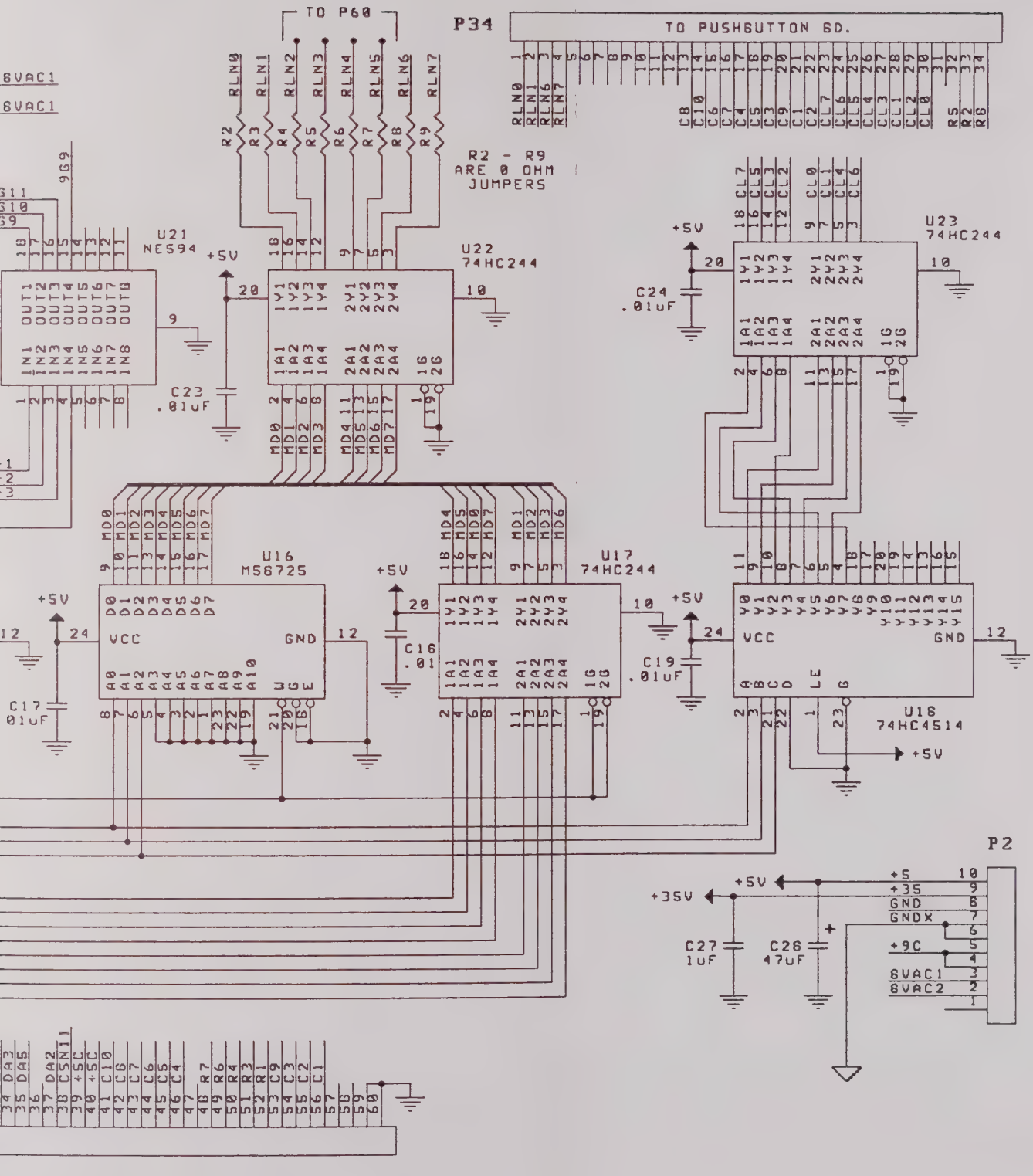



NOTES: UNLESS OTHERWISE SPECIFIED

1) RESISTORS ARE IN OHMS.
2) CAPACITORS ARE IN uF.
3) * INDICATES HEATSINK IS REQD

**Display Driver (A20)**
**ASSY# 120BA01411 Rev B**
**Sheet 3 of 4**
**7-A20-3**


P9
8VAC2
SEGMENTS
9A 9B 9C 9D 9E 9F 9G 9DP
9G1 9G2 9G3 9G4 9G5 9G6 9G7 9G8 9G9
9AC
5AC
R11
1S
R12
62.5
DIGITS
TO P11
U19 NE594
U20 NE594
+35V
C20 .01uF
C21 .01uF
C22 .01uF
OUT1 OUT2 OUT3 OUT4 OUT5 OUT6 OUT7 OUT8
IN1 IN2 IN3 IN4 IN5 IN6 IN7 IN8
9D0 9D1 9D2 9D3 9D4 9D5 9D6 9D7
FROM PG 1
U21
U13 M58725
U14 74HC244
U15 74HC4514
+5V
C14 .01
C15 .01
C16 .01uF
D0 D1 D2 D3 D4 D5 D6 D7
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10
VCC GND W G E
1A1 1A2 1A3 1A4 2A1 2A2 2A3 2A4 1G 2G
1Y1 1Y2 1Y3 1Y4 2Y1 2Y2 2Y3 2Y4
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7 Y8 Y9 Y10 Y11 Y12 Y13 Y14 Y15
A B C D LE G
TO J1
URN2
URN3
QA
QB
QC
QD
FROM PG 1
DD12
DD13
DD8
DD15
DD9
DD10
DD11
DD14
GNDX
+9C
+5C
L1 1mH
C30 1uF
C25 470uF 16V
C26 470uF 16V
U24 * MC7805CT
+5V GND Vin
CL0 CL1 CL2 CL3 CL4 CL5 CL6 CL7 RLN4 RLN3 RESETN RLN5 DUR/WN RLN2 CSN9
DD12 DD13 DD8 DD15 DD9 DD10 DD11 DD14 GNDX CSN10 CSN12 DA1 DA6
P60
TO DATA ENT




**Display Driver (A20)**
**ASSY# 120BA01411 Rev B**
**Sheet 4 of 4**
**7-A20-4**

Bill of Material (by Ref Designator)

Parts List For: 120BA08351 YIG DRIVER PCA; GT9000S REV: A

| Item | Part Number | Qty | Mfgr | Mfr's Part Number | Description |
|---|---|---|---|---|---|
| 0 | 120BS08351 | 0.000 | | | YIG DRIVER SCH; GT9000S |
| 1 | 120CF08300 | 1.000 | | | YIG DRIVER PCB |
| 2 | ETST-06224 | 1.000 | USECO | 1280B-1 | TURRET TERMINAL |
| 3 | WJIB-02022 | 2.000 | 3M | 923345-02 | .2 INSULATED JUMPER |
| C 1 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 2 | CC50-04100 | 1.000 | KEMET | C322C104M5U5CA | .1 UF CERAMIC Z5U |
| C 3 | CC50-00330 | 1.000 | KEMET | C315C330J2G5CA | 33 PF CERAMIC NPO |
| C 4 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 5 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 6 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 7 | CC50-03220 | 1.000 | KEMET | C315C223K5R5CA | .022 UF CERAMIC X7R |
| C 8 | CT25-R6100 | 1.000 | KEMET | T356E106M025AS | 10 UF 25V RADIAL LEAD |
| C 9 | CC50-04100 | 1.000 | KEMET | C322C104M5U5CA | .1 UF CERAMIC Z5U |
| C 10 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 11 | CC50-04100 | 1.000 | KEMET | C322C104M5U5CA | .1 UF CERAMIC Z5U |
| C 12 | CC50-00330 | 1.000 | KEMET | C315C330J2G5CA | 33 PF CERAMIC NPO |
| C 13 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 14 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 15 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 16 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 17 | CC50-03220 | 1.000 | KEMET | C315C223K5R5CA | .022 UF CERAMIC X7R |
| C | CT25-R6100 | 1.000 | KEMET | T356E106M025AS | 10 UF 25V RADIAL LEAD |
| C 19 | CC50-04100 | 1.000 | KEMET | C322C104M5U5CA | .1 UF CERAMIC Z5U |
| C 20 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 21 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 22 | CE25-R6470 | 1.000 | PANSON | ECEA1EU470 | 47 UF 25V RADIAL LEAD |
| C 23 | CE25-R6470 | 1.000 | PANSON | ECEA1EU470 | 47 UF 25V RADIAL LEAD |
| C 24 | CE25-R6470 | 1.000 | PANSON | ECEA1EU470 | 47 UF 25V RADIAL LEAD |
| C 25 | CE25-R6470 | 1.000 | PANSON | ECEA1EU470 | 47 UF 25V RADIAL LEAD |
| C 26 | CE25-R6470 | 1.000 | PANSON | ECEA1EU470 | 47 UF 25V RADIAL LEAD |
| C 27 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 28 | CC50-04100 | 1.000 | KEMET | C322C104M5U5CA | .1 UF CERAMIC Z5U |
| C 29 | CE25-R6470 | 1.000 | PANSON | ECEA1EU470 | 47 UF 25V RADIAL LEAD |
| C 30 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 31 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 32 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 33 | CC50-04100 | 1.000 | KEMET | C322C104M5U5CA | .1 UF CERAMIC Z5U |
| C 34 | CC50-00330 | 1.000 | KEMET | C315C330J2G5CA | 33 PF CERAMIC NPO |
| C 35 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 36 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 37 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 38 | CC50-03220 | 1.000 | KEMET | C315C223K5R5CA | .022 UF CERAMIC X7R |
| C 39 | CT25-R6100 | 1.000 | KEMET | T356E106M025AS | 10 UF 25V RADIAL LEAD |
| C 40 | CC50-04100 | 1.000 | KEMET | C322C104M5U5CA | .1 UF CERAMIC Z5U |
| C 41 | CC50-04100 | 1.000 | KEMET | C322C104M5U5CA | .1 UF CERAMIC Z5U |

rts List For: 120BA08351 YIG DRIVER PCA; GT9000S REV: A

| tem | Part Number | Qty | Mfgr | Mfr's Part Number | Description |
|---|---|---|---|---|---|
| 42 | CC50-00330 | 1.000 | KEMET | C315C330J2G5CA | 33 PF CERAMIC NPO |
| 43 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 44 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 45 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 46 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 47 | CC50-03220 | 1.000 | KEMET | C315C223K5R5CA | .022 UF CERAMIC X7R |
| 48 | CT25-R6100 | 1.000 | KEMET | T356E106M025AS | 10 UF 25V RADIAL LEAD |
| 49 | CC50-04100 | 1.000 | KEMET | C322C104M5U5CA | .1 UF CERAMIC Z5U |
| 50 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 51 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 52 | CE50-R6100 | 1.000 | NIC CO | UVX1H100MAA | 10 UF 50V RADIAL LEAD |
| 53 | CC50-04100 | 1.000 | KEMET | C322C104M5U5CA | .1 UF CERAMIC Z5U |
| 54 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 55 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 56 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 57 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 58 | CC50-02100 | 1.000 | AVX | SR155C122MAT | .001 UF CERAMIC Y5P |
| 59 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 60 | CC50-02100 | 1.000 | AVX | SR155C122MAT | .001 UF CERAMIC Y5P |
| 61 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 62 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 63 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 64 | CC50-01470 | 1.000 | KEMET | C315C471K1G5CA | 470 PF CERAMIC NPO |
| 65 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 66 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 67 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 68 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 69 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 70 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 71 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 72 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 1 | DSA0-04148 | 1.000 | ANY | 1N4148 | 1N4148 G.P. DIODE |
| 2 | DSA0-04148 | 1.000 | ANY | 1N4148 | 1N4148 G.P. DIODE |
| 3 | DSA0-04148 | 1.000 | ANY | 1N4148 | 1N4148 G.P. DIODE |
| 4 | DSA0-04148 | 1.000 | ANY | 1N4148 | 1N4148 G.P. DIODE |
| 1 | QBNS-02222 | 1.000 | ANY | PN2222 | PN2222 .5A 30V NPN |
| 2 | QBNS-02222 | 1.000 | ANY | PN2222 | PN2222 .5A 30V NPN |
| 3 | QBNS-02222 | 1.000 | ANY | PN2222 | PN2222 .5A 30V NPN |
| 4 | QBNS-02222 | 1.000 | ANY | PN2222 | PN2222 .5A 30V NPN |
| 5 | QBNS-02222 | 1.000 | ANY | PN2222 | PN2222 .5A 30V NPN |
| 6 | QBNS-02222 | 1.000 | ANY | PN2222 | PN2222 .5A 30V NPN |
| 7 | QBNS-02222 | 1.000 | ANY | PN2222 | PN2222 .5A 30V NPN |
| 8 | QBNS-02222 | 1.000 | ANY | PN2222 | PN2222 .5A 30V NPN |
| 1 | RAPG-12000 | 1.000 | BOURNS | 3296Z-1-202 | 2K 10% 25T .5W POT. |
| 2 | RAPG-12000 | 1.000 | BOURNS | 3296Z-1-202 | 2K 10% 25T .5W POT. |

Bill of Material (by Ref Designator)

Parts List For: 120BA08351 YIG DRIVER PCA; GT9000S REV: A

| Item | Part Number | Qty | Mfgr | Mfr's Part Number | Description |
|---|---|---|---|---|---|
| R 3 | RN55-24750 | 1.000 | DALE | RN55C4752F | 47.5 K OHMS 1% MET FILM |
| R 4 | RN50-14990 | 1.000 | DALE | RN50C4991F | 4.99 K OHMS 1% NET FILM |
| R 5 | RN55-23920 | 1.000 | DALE | RN55C3922F | 39.2 K OHMS 1% MET FILM |
| R 6 | RN50-11000 | 1.000 | DALE | RNC50H1001F | 1.00 K OHMS 1% MET FILM |
| R 7 | RN50-01000 | 1.000 | DALE | RN50C1000F | 100 OHMS 1% METAL FILM |
| R 8 | RN50-14990 | 1.000 | DALE | RN50C4991F | 4.99 K OHMS 1% NET FILM |
| R 9 | RN55-01000 | 1.000 | DALE | RN55C1000F | 100 OHMS 1% MET FILM |
| R 10 | RN50-14990 | 1.000 | DALE | RN50C4991F | 4.99 K OHMS 1% NET FILM |
| R 11 | RAPG-12000 | 1.000 | BOURNS | 3296Z-1-202 | 2K 10% 25T .5W POT. |
| R 12 | RAPG-12000 | 1.000 | BOURNS | 3296Z-1-202 | 2K 10% 25T .5W POT. |
| R 13 | RAPG-15000 | 1.000 | BOURNS | 3296Z-1-502 | 5K 10% 25T .5W TRIM. POT |
| R 14 | RN50-24750 | 1.000 | DALE | RN50C4752F | 47.5K OHMS 1% MET FILM |
| R 15 | RN50-14990 | 1.000 | DALE | RN50C4991F | 4.99 K OHMS 1% NET FILM |
| R 16 | RN55-23920 | 1.000 | DALE | RN55C3922F | 39.2 K OHMS 1% MET FILM |
| R 17 | RN55-21020 | 1.000 | DALE | RN55C1022F | 10.2 K OHMS 1% MET FILM |
| R 18 | RN50-11000 | 1.000 | DALE | RNC50H1001F | 1.00 K OHMS 1% MET FILM |
| R 19 | RN50-01000 | 1.000 | DALE | RN50C1000F | 100 OHMS 1% METAL FILM |
| R 20 | RN50-14990 | 1.000 | DALE | RN50C4991F | 4.99 K OHMS 1% NET FILM |
| R 21 | RN55-01000 | 1.000 | DALE | RN55C1000F | 100 OHMS 1% MET FILM |
| R 22 | RN50-14990 | 1.000 | DALE | RN50C4991F | 4.99 K OHMS 1% NET FILM |
| R 23 | RAPG-12000 | 1.000 | BOURNS | 3296Z-1-202 | 2K 10% 25T .5W POT. |
| 24 | RAPG-12000 | 1.000 | BOURNS | 3296Z-1-202 | 2K 10% 25T .5W POT. |
| R 25 | RAPG-15000 | 1.000 | BOURNS | 3296Z-1-502 | 5K 10% 25T .5W TRIM. POT |
| R 26 | RN55-22490 | 1.000 | DALE | RN55D2492F | 24.9 K OHMS 1% MET FILM |
| R 27 | RN50-14990 | 1.000 | DALE | RN50C4991F | 4.99 K OHMS 1% NET FILM |
| R 28 | RN55-21500 | 1.000 | DALE | RN55C1502F | 15 K OHMS 1% MET FILM |
| R 29 | RN55-21400 | 1.000 | DALE | RN55C1402F | 14 K OHMS 1% MET FILM |
| R 30 | RN50-11000 | 1.000 | DALE | RNC50H1001F | 1.00 K OHMS 1% MET FILM |
| R 31 | RN50-01000 | 1.000 | DALE | RN50C1000F | 100 OHMS 1% METAL FILM |
| R 32 | RN50-14990 | 1.000 | DALE | RN50C4991F | 4.99 K OHMS 1% NET FILM |
| R 33 | RN55-01000 | 1.000 | DALE | RN55C1000F | 100 OHMS 1% MET FILM |
| R 34 | RN50-14990 | 1.000 | DALE | RN50C4991F | 4.99 K OHMS 1% NET FILM |
| R 35 | RAPG-15000 | 1.000 | BOURNS | 3296Z-1-502 | 5K 10% 25T .5W TRIM. POT |
| R 36 | RAPG-12000 | 1.000 | BOURNS | 3296Z-1-202 | 2K 10% 25T .5W POT. |
| R 37 | RAPG-15000 | 1.000 | BOURNS | 3296Z-1-502 | 5K 10% 25T .5W TRIM. POT |
| R 38 | RN55-26650 | 1.000 | DALE | RN55C6652F | 66.5 K OHMS 1% MET FILM |
| R 39 | RN50-14990 | 1.000 | DALE | RN50C4991F | 4.99 K OHMS 1% NET FILM |
| R 40 | RN55-21690 | 1.000 | DALE | RN55C1692F | 16.9 K OHMS 1% MET FILM |
| R 41 | RN55-22260 | 1.000 | DALE | RN55C2262F | 22.6 K OHMS 1% MET FILM |
| R 42 | RN50-11000 | 1.000 | DALE | RNC50H1001F | 1.00 K OHMS 1% MET FILM |
| R 43 | RN50-01000 | 1.000 | DALE | RN50C1000F | 100 OHMS 1% METAL FILM |
| R 44 | RN50-14990 | 1.000 | DALE | RN50C4991F | 4.99 K OHMS 1% NET FILM |
| R 45 | RN55-01000 | 1.000 | DALE | RN55C1000F | 100 OHMS 1% MET FILM |
| R 46 | RN50-14990 | 1.000 | DALE | RN50C4991F | 4.99 K OHMS 1% NET FILM |
| R 47 | RAPG-21000 | 1.000 | BOURNS | 3296Z-1-103 | 10K 10% 25T .5W TRIM POT |

Bill of Material (by Ref Designator)

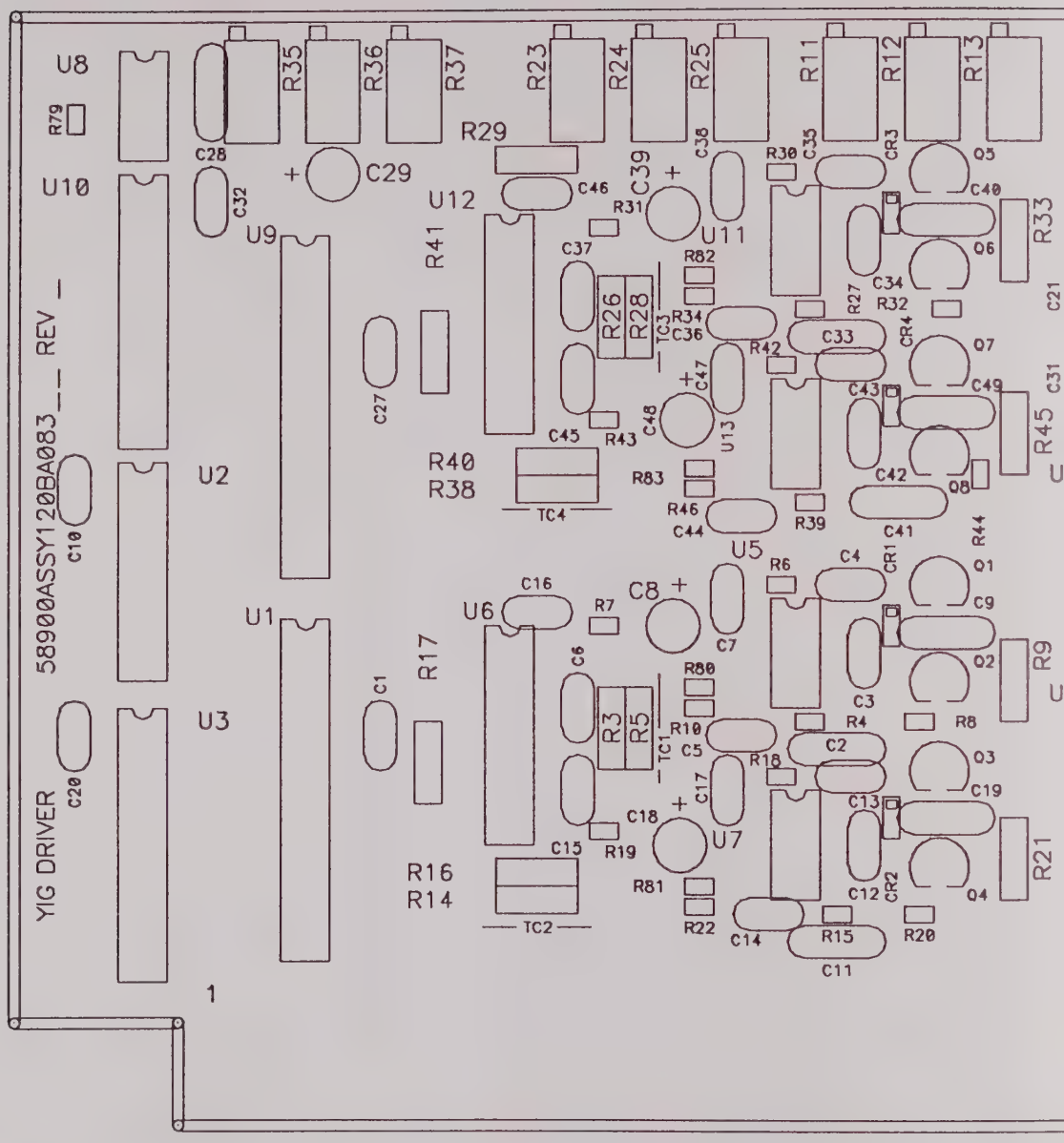
arts List For: 120BA08351 YIG DRIVER PCA; GT9000S REV: A

| em | Part Number | Qty | Mfgr | Mfr's Part Number | Description |
|---|---|---|---|---|---|
| 48 | RAPG-21000 | 1.000 | BOURNS | 3296Z-1-103 | 10K 10% 25T .5W TRIM POT |
| 49 | RAPG-21000 | 1.000 | BOURNS | 3296Z-1-103 | 10K 10% 25T .5W TRIM POT |
| 50 | RAPG-21000 | 1.000 | BOURNS | 3296Z-1-103 | 10K 10% 25T .5W TRIM POT |
| 51 | RN50-21000 | 1.000 | DALE | RN50C1002F | 10.0 K OHMS 1% MET FILM |
| 52 | RN50-41000 | 1.000 | DALE | RN50C1004F | 1.00 M OHMS 1% MET FILM |
| 53 | RN50-14990 | 1.000 | DALE | RN50C4991F | 4.99 K OHMS 1% NET FILM |
| 54 | RN50-14990 | 1.000 | DALE | RN50C4991F | 4.99 K OHMS 1% NET FILM |
| 55 | RN50-41000 | 1.000 | DALE | RN50C1004F | 1.00 M OHMS 1% MET FILM |
| 56 | RN50-21000 | 1.000 | DALE | RN50C1002F | 10.0 K OHMS 1% MET FILM |
| 57 | RN50-41000 | 1.000 | DALE | RN50C1004F | 1.00 M OHMS 1% MET FILM |
| 58 | RN50-41000 | 1.000 | DALE | RN50C1004F | 1.00 M OHMS 1% MET FILM |
| 59 | RN50-14990 | 1.000 | DALE | RN50C4991F | 4.99 K OHMS 1% NET FILM |
| 60 | RN50-14990 | 1.000 | DALE | RN50C4991F | 4.99 K OHMS 1% NET FILM |
| 61 | RN55-32320 | 1.000 | DALE | RN55D2323F | 232 K OHMS 1% MET FILM |
| 62 | RN55-23010 | 1.000 | DALE | RN55C3012F | 30.1 K OHMS 1% MET FILM |
| 63 | RN55-13920 | 1.000 | DALE | RN55C3921F | 3.92 K OHMS 1% MET FILM |
| 64 | RN55-14990 | 1.000 | DALE | RN55C4991F | 4.99 K OHMS 1% MET FILM |
| 65 | RN50-21000 | 1.000 | DALE | RN50C1002F | 10.0 K OHMS 1% MET FILM |
| 66 | RN50-21000 | 1.000 | DALE | RN50C1002F | 10.0 K OHMS 1% MET FILM |
| 67 | RN50-21000 | 1.000 | DALE | RN50C1002F | 10.0 K OHMS 1% MET FILM |
| 68 | RN50-21000 | 1.000 | DALE | RN50C1002F | 10.0 K OHMS 1% MET FILM |
| 69 | RN50-21000 | 1.000 | DALE | RN50C1002F | 10.0 K OHMS 1% MET FILM |
| 70 | RN50-21000 | 1.000 | DALE | RN50C1002F | 10.0 K OHMS 1% MET FILM |
| 71 | RN50-21000 | 1.000 | DALE | RN50C1002F | 10.0 K OHMS 1% MET FILM |
| 72 | RN50-02000 | 1.000 | DALE | RN50C2000F | 200 OHMS 1% METAL FILM |
| 73 | RN50-02000 | 1.000 | DALE | RN50C2000F | 200 OHMS 1% METAL FILM |
| 74 | RN50-02000 | 1.000 | DALE | RN50C2000F | 200 OHMS 1% METAL FILM |
| 75 | RN50-02000 | 1.000 | DALE | RN50C2000F | 200 OHMS 1% METAL FILM |
| 76 | RN50-02000 | 1.000 | DALE | RN50C2000F | 200 OHMS 1% METAL FILM |
| 77 | RN50-02000 | 1.000 | DALE | RN50C2000F | 200 OHMS 1% METAL FILM |
| 78 | RN50-01000 | 1.000 | DALE | RN50C1000F | 100 OHMS 1% METAL FILM |
| 79 | RN50-05620 | 1.000 | DALE | RN50D5620F | 562 OHMS 1% METAL FILM |
| 80 | RN50-31000 | 1.000 | DALE | RN50C1003F | 100 K OHMS 1% MET FILM |
| 81 | RN50-31000 | 1.000 | DALE | RN50C1003F | 100 K OHMS 1% MET FILM |
| 82 | RN50-31000 | 1.000 | DALE | RN50C1003F | 100 K OHMS 1% MET FILM |
| 83 | RN50-31000 | 1.000 | DALE | RN50C1003F | 100 K OHMS 1% MET FILM |
| 1 | 120BA17105 | 1.000 | | | TEMP COMP RES ASSY 750K |
| 2 | 120BA17105 | 1.000 | | | TEMP COMP RES ASSY 750K |
| 3 | 120BA17104 | 1.000 | | | TEMP COMP RES ASSY 475K |
| 4 | 120BA17102 | 1.000 | | | TEMP COMP RES ASSY 402K |
| 1 | UIN0-07547 | 1.000 | MAXIM | AD7547KN | AD7547KN DUAL 12 BIT DAC |
| 2 | UTN0-01382 | 1.000 | TI | 74HC138N | 74HC138 DECODER/DEMULTIP |
| 3 | UTN0-02732 | 1.000 | TI | 74HC273N | 74HC273;OCTAL D-TYPE F-F |
| 4 | ULN0-05053 | 1.000 | MAXIM | DG412DJ | IH5053 QUAD ANALOG SWITC |
| 5 | UON0-00708 | 1.000 | ANALO1 | AD708JN | AD708JN DUAL OP AMP |

Bill of Material (by Ref Designator)

Parts List For: 120BA08351 YIG DRIVER PCA; GT9000S REV: A

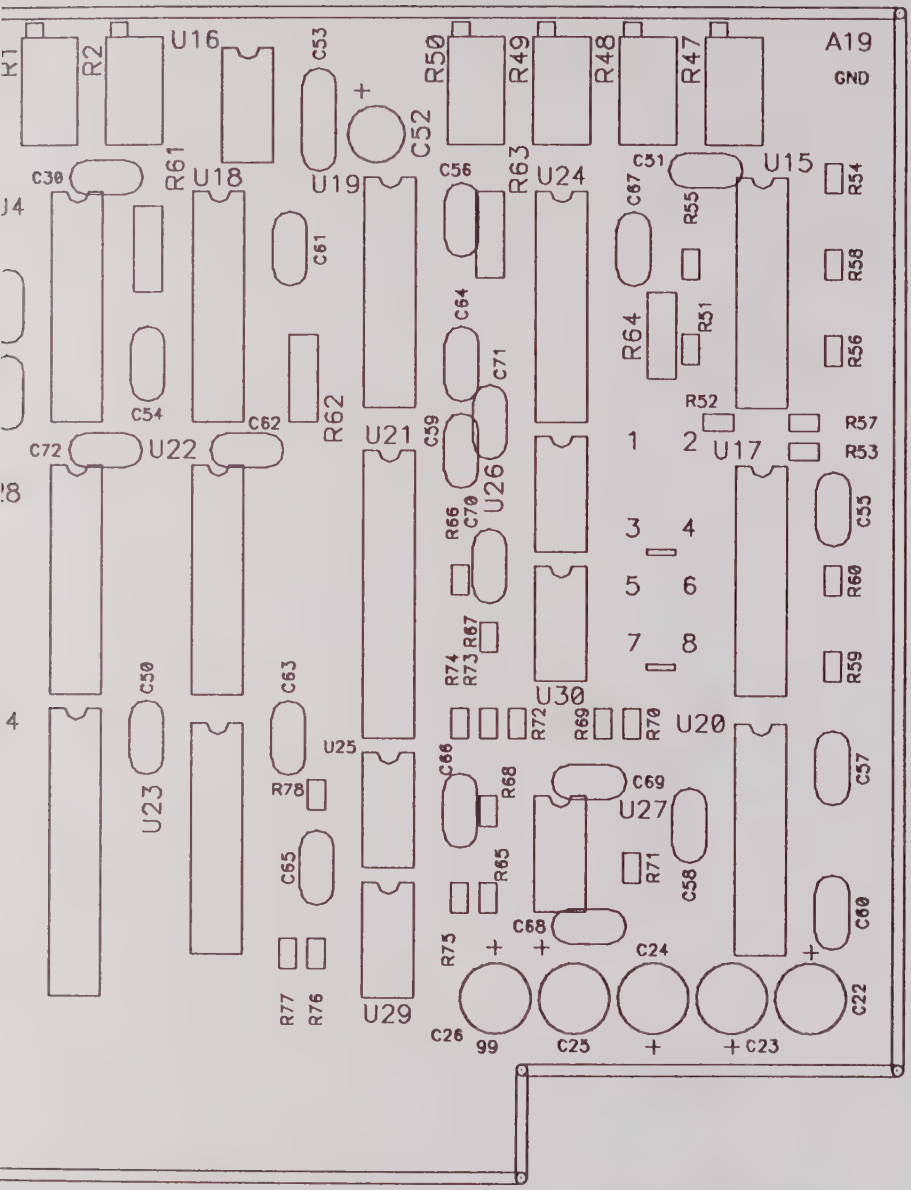
| Item | Part Number | Qty | Mfgr | Mfr's Part Number | Description |
|---|---|---|---|---|---|
| U 6 | ULNO-05043 | 1.000 | MAXIM | IH5043CPE | IH5043CPA DUAL SPDT SW |
| U 7 | UONO-00708 | 1.000 | ANALO1 | AD708JN | AD708JN DUAL OP AMP |
| U 8 | UVNP-00100 | 1.000 | ANALO | AD587JQ | AD587 10V 20PPM REF |
| U 9 | UINO-07547 | 1.000 | MAXIM | AD7547KN | AD7547KN DUAL 12 BIT DAC |
| U 10 | UTNO-02732 | 1.000 | TI | 74HC273N | 74HC273;OCTAL D-TYPE F-F |
| U 11 | UONO-00708 | 1.000 | ANALO1 | AD708JN | AD708JN DUAL OP AMP |
| U 12 | ULNO-05043 | 1.000 | MAXIM | IH5043CPE | IH5043CPA DUAL SPDT SW |
| U 13 | UONO-00708 | 1.000 | ANALO1 | AD708JN | AD708JN DUAL OP AMP |
| U 14 | UTNO-02732 | 1.000 | TI | 74HC273N | 74HC273;OCTAL D-TYPE F-F |
| U 15 | ULNO-02901 | 1.000 | TI | LM2901N | LM2901N QUAD COMPARATOR |
| U 16 | UVNP-00100 | 1.000 | ANALO | AD587JQ | AD587 10V 20PPM REF |
| U 17 | UTNO-00862 | 1.000 | TI | 74HC86N | 74HC86 QUAD 2 INPUT X OR |
| U 18 | UTNO-01232 | 1.000 | ANY | 74HC123 | 74HC123 RETRIG. MULTI |
| U 19 | UTNO-00742 | 1.000 | RCA | SN74HC74D | 74HC74 DUAL D FLIP FLOP |
| U 20 | UTNO-00862 | 1.000 | TI | 74HC86N | 74HC86 QUAD 2 INPUT X OR |
| U 21 | UTNO-02732 | 1.000 | TI | 74HC273N | 74HC273;OCTAL D-TYPE F-F |
| U 22 | UTNO-00322 | 1.000 | TI | 74HC32N | 74HC32 QUAD 2 INPUT OR |
| U 23 | UTNO-00322 | 1.000 | TI | 74HC32N | 74HC32 QUAD 2 INPUT OR |
| U 24 | UTNO-01232 | 1.000 | ANY | 74HC123 | 74HC123 RETRIG. MULTI |
| U 25 | UONO-05532 | 1.000 | SIG | NE5532N | NE5532 DUAL OP AMP |
| U 26 | UONO-05532 | 1.000 | SIG | NE5532N | NE5532 DUAL OP AMP |
| U | UONO-00072 | 1.000 | TI | TL072CP | TL072CP DUAL FET OP AMP |
| U 28 | UTNO-00322 | 1.000 | TI | 74HC32N | 74HC32 QUAD 2 INPUT OR |
| U 29 | UONO-05532 | 1.000 | SIG | NE5532N | NE5532 DUAL OP AMP |
| U 30 | UONO-05532 | 1.000 | SIG | NE5532N | NE5532 DUAL OP AMP |




**YIG DRIVER -- PC ASSY A19**

The YIG Driver PCA consists of 4 YIG driver circuits, one for each of the frequency bands (2-8, 8-20, 20-26 GHz and the Reference oscillator). In addition, this board holds the circuitry which generates the logic for different frequency bands, and for switching filters in RF modules. It also generates logic used during sweep.

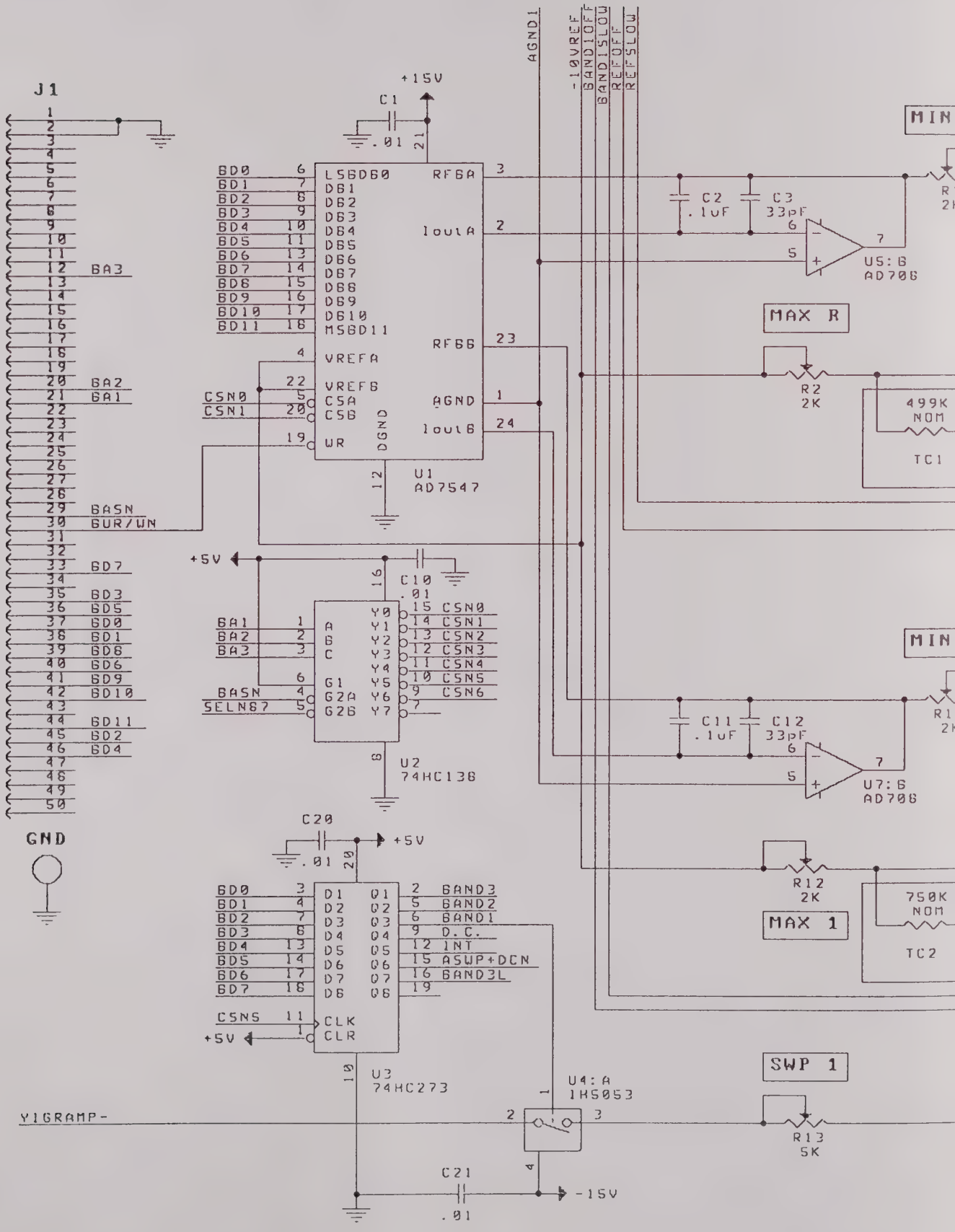
The YIG driver circuit for BAND1 consists of DAC U1 section B whose output is converted to voltage by U7 B. MIN 1 pot (R11) is used for adjusting the voltage to the YIG when at the minimum frequency in band 1. The reference voltage is also summed in at U7-2 thru MAX 1 pot (R12) which is used to adjust the voltage provided to the YIG when at the maximum frequency in band 1. At the output of U7 A there is a filter which can be switched in by U6 B when the Unit is in CW or 'SLOW' mode, ie, when the Unit is not sweeping or changing frequency. This filter is disabled, when the unit is sweeping or changing frequency, allowing the YIG voltage to change rapidly. This switched filter is known as the 'Fast/Slow' circuitry. When analog sweep is activated U4 A is switched allowing a ramp voltage to be summed into the amplifier U7 to sweep the YIG thru the specified band. Q4 is required to turn off the tuning voltage to the YIG when the band is not selected. Q3 provides the drive for the Main tune coil of the YIG.

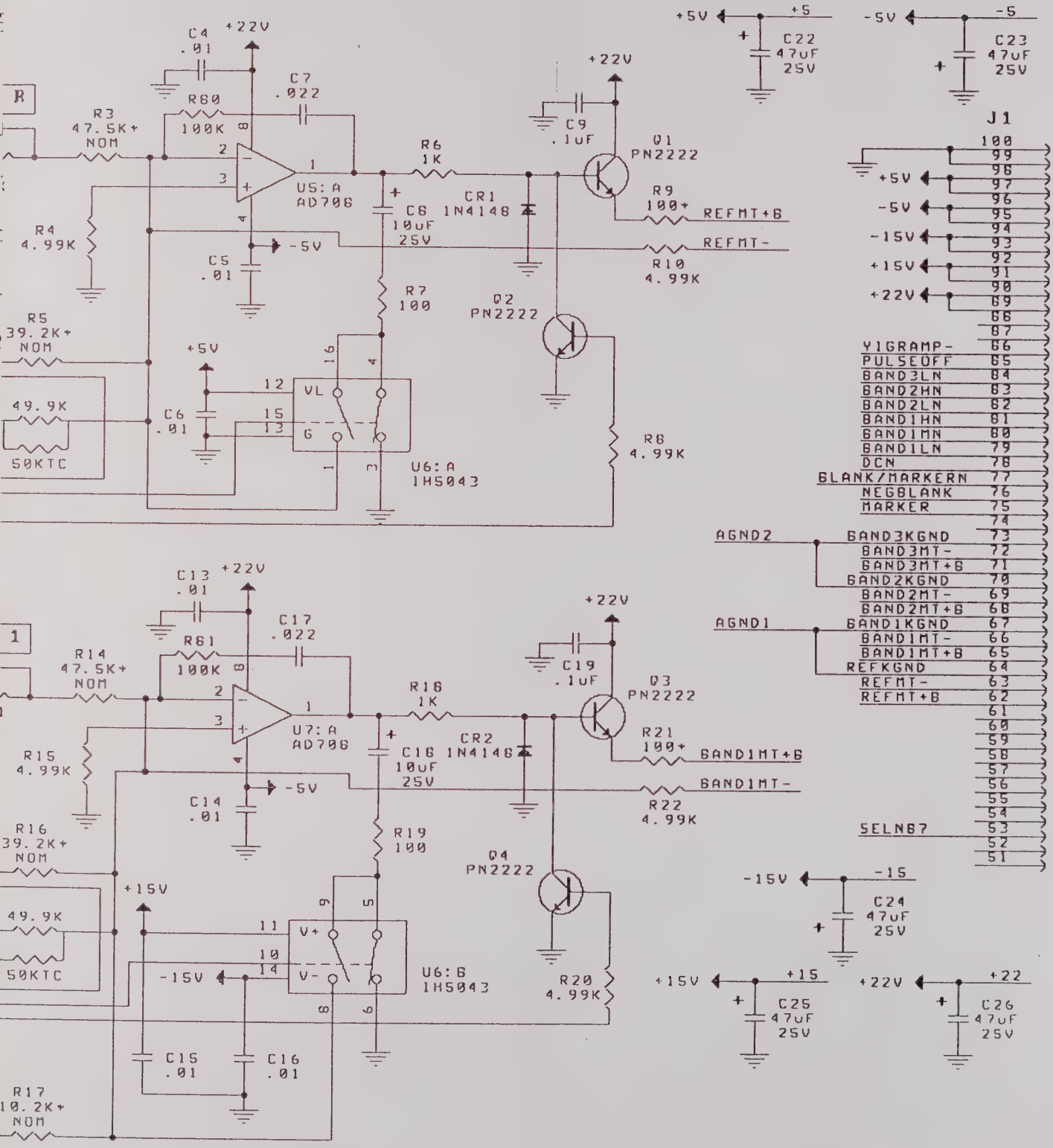



This circuit is repeated for each of the bands. The only difference is that in the reference band there is not a ramp voltage summed in during analog sweep.

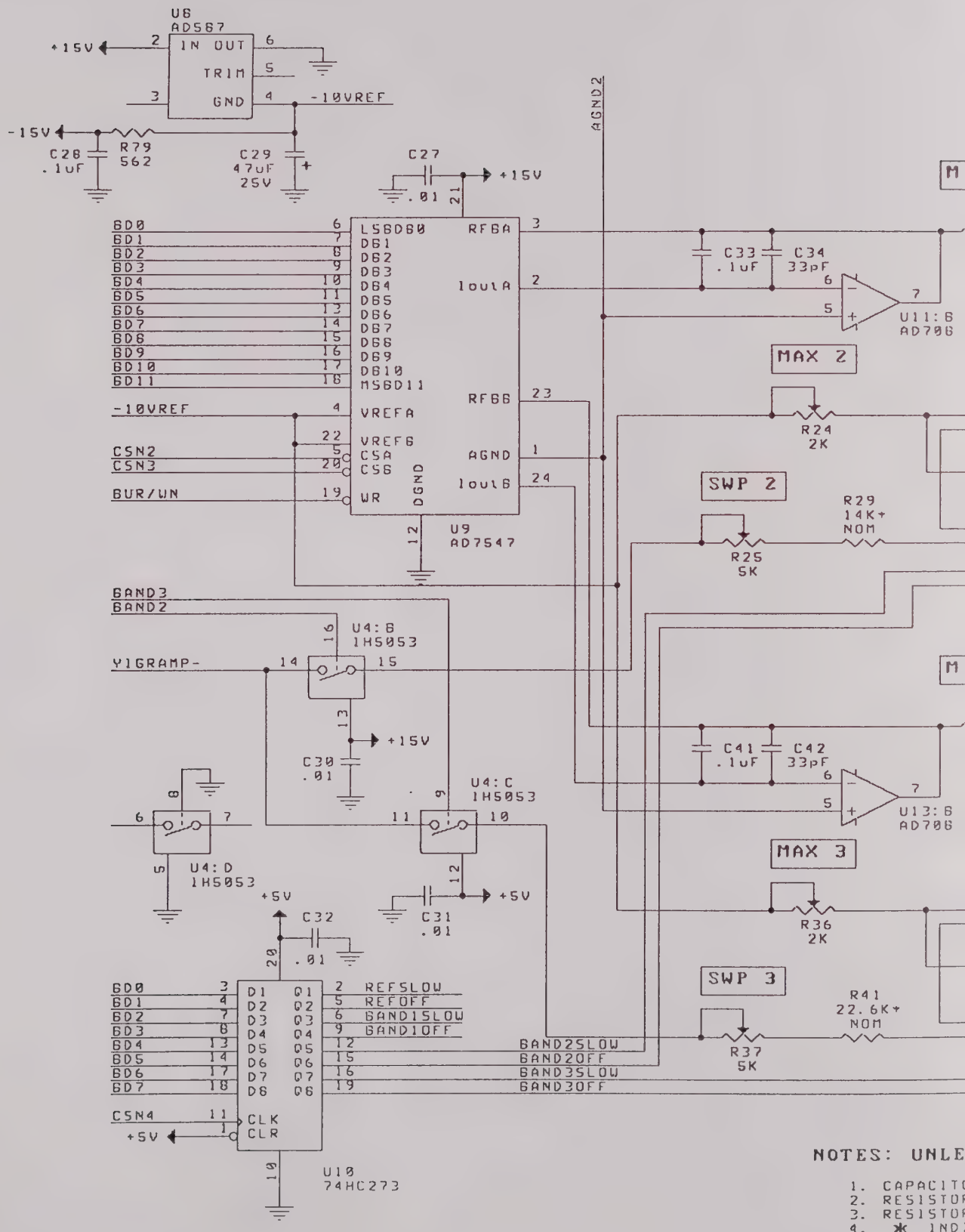
Filter switching logic and sweep logic signals are also generated on A19. When the unit is not in analog sweep U21 is cleared thereby enabling U22 and U23 to propagate the logic latched by U14 from the computer bus. These outputs drive U25 and U26 which drive the filter switches for the output switch module. When the unit is in analog sweep, the computer cannot provide the logic signals at the appropriate times therefore another method is used to detect when to switch the filters. For example, in band 1 this method involves sampling the main tuning voltage and using a comparator U15 C to detect when the main tune voltage reaches a voltage set by the 5.2 pot (R49). This 5.2 reference voltage can be adjusted to insure that the comparator output switches when the frequency is at 5.2 GHz. The output then propagates thru to U21 which is enabled during analog sweep. The remaining logic along with flip flops U18, U19 and U24 work in conjunction to supply the remaining filter logic and blanking signals required during analog sweep.

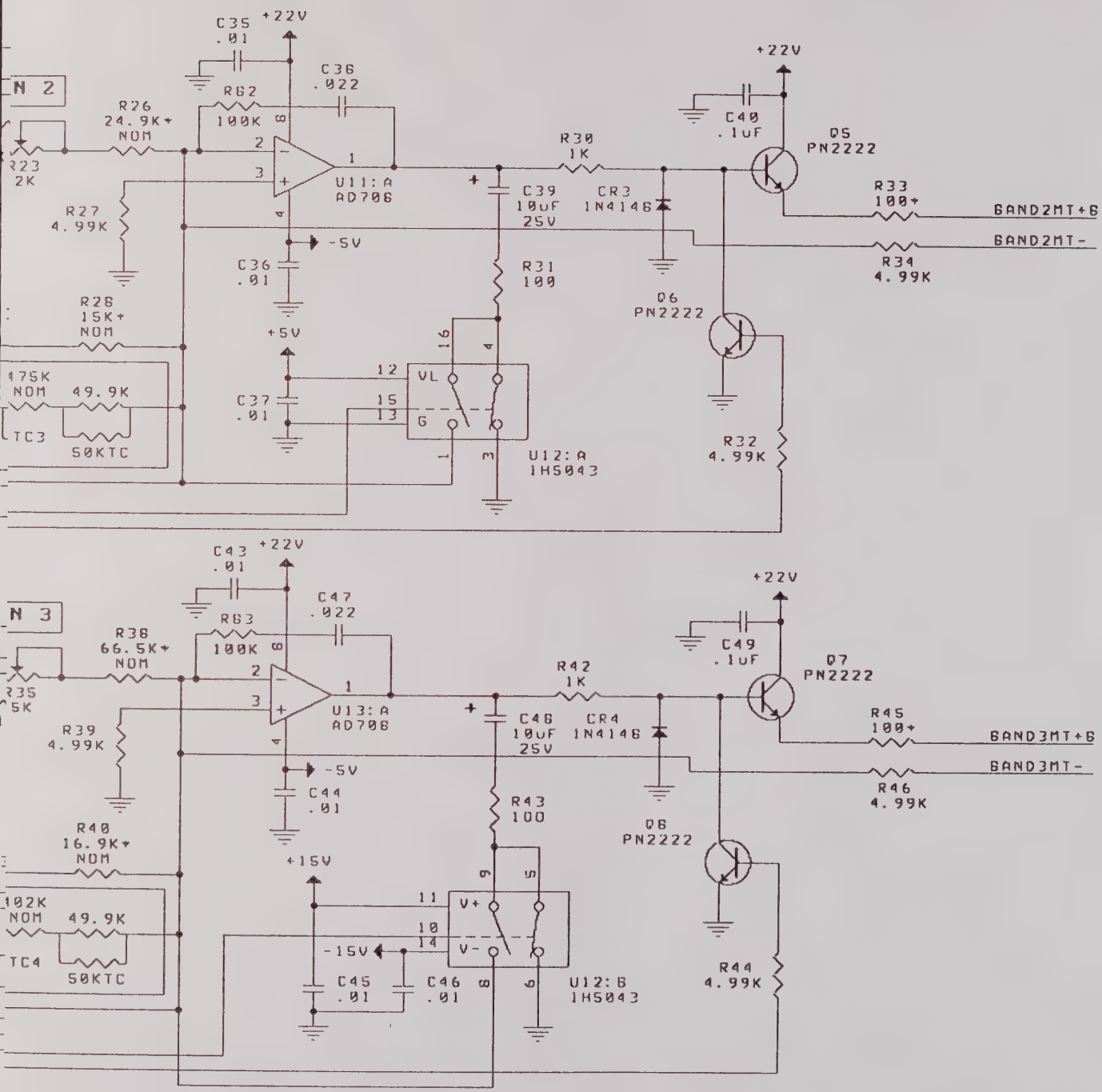
Decoder U2 decodes the chip select lines for circuits on this PC board. U3, U10 and U14 are required for computer bus interface.


J1
GND
+15V
C1
.01
AGND1
-10VREF
BAND1OFF
BAND1SLOW
REFOFF
REFSLOW
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
BD8
BD9
BD10
BD11
LSBDB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DB8
DB9
DB10
MSBD11
VREFA
VREFB
CSA
CSB
WR
DGND
RFBA
IoutA
RFBB
AGND
IoutB
U1
AD7547
CSN0
CSN1
BA3
BA2
BA1
BASN
BUR/WN
C2
.1uF
C3
33pF
U5:B
AD706
MAX R
R2
2K
499K
NOM
TC1
MIN
+5V
C10
.01
A
B
C
G1
G2A
G2B
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
CSN0
CSN1
CSN2
CSN3
CSN4
CSN5
CSN6
SELN87
U2
74HC138
C11
.1uF
C12
33pF
U7:B
AD706
R12
2K
750K
NOM
TC2
MAX 1
C20
.01
+5V
D1
D2
D3
D4
D5
D6
D7
D8
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
BAND3
BAND2
BAND1
D.C.
INT
ASWP+DCN
BAND3L
CSN5
CLK
CLR
+5V
U3
74HC273
U4:A
1HS053
SWP 1
R13
5K
YIGRAMP-
C21
.01
-15V




**YIG Driver (A19)**
**ASSY# 120BA08351 Rev A**
**Sheet 3 of 5**
**7-A19-3**

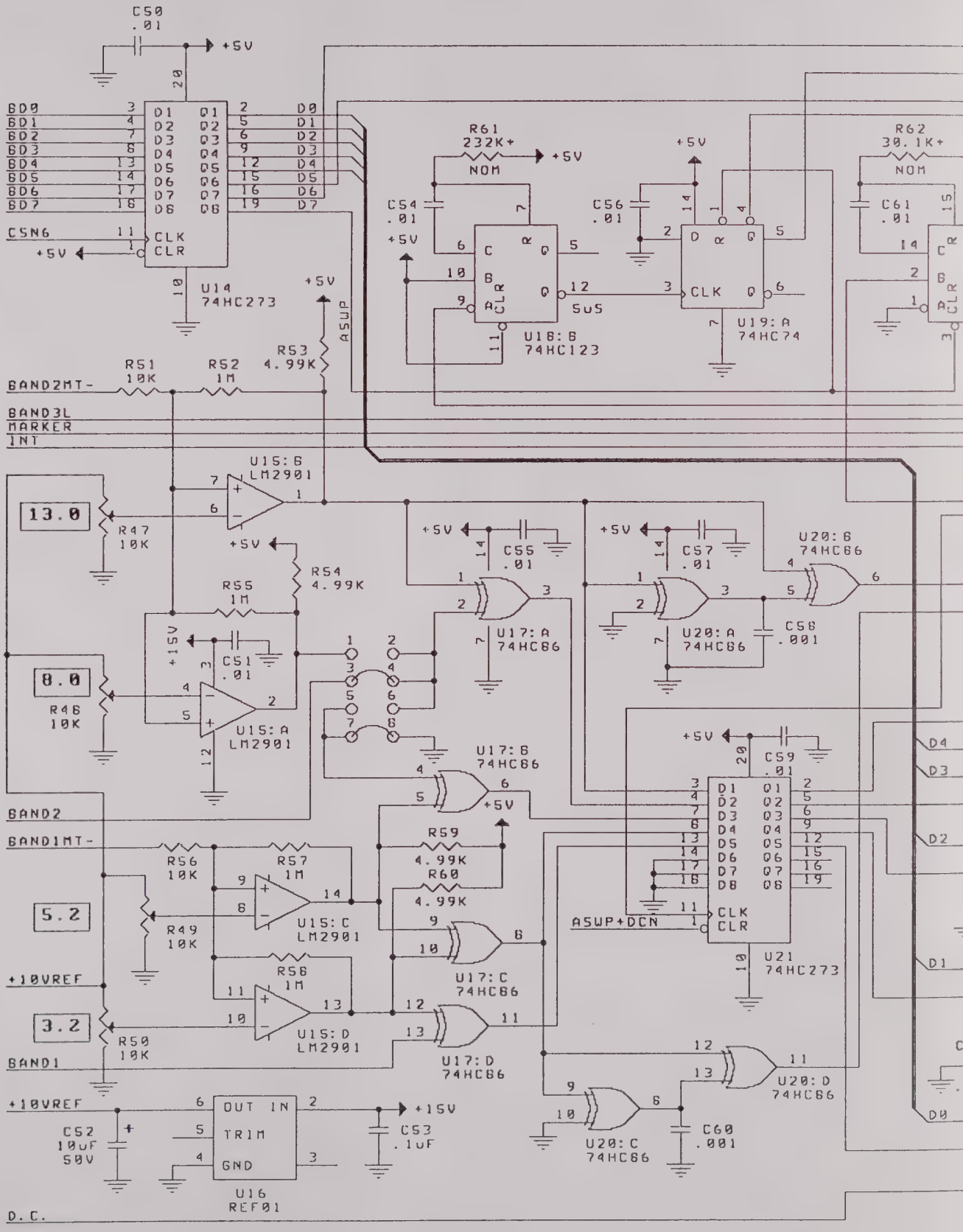

U8
AD587
+15V
IN OUT
TRIM
GND
-10VREF
-15V
C28
.1uF
R79
562
C29
47uF
25V
C27
.01
+15V
AGND2
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
BD8
BD9
BD10
BD11
LSBDB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DB8
DB9
DB10
MSBD11
VREFA
VREFB
CSA
CSB
WR
DGND
RFBA
IoutA
RFBB
AGND
IoutB
U9
AD7547
-10VREF
CSN2
CSN3
BUR/WN
C33
.1uF
C34
33pF
U11:B
AD706
MAX 2
R24
2K
SWP 2
R29
14K+
NOM
R25
5K
BAND3
BAND2
U4:B
1H5053
Y1GRAMP-
C30
.01
+15V
U4:C
1H5053
U4:D
1H5053
C41
.1uF
C42
33pF
U13:B
AD706
MAX 3
R36
2K
SWP 3
R41
22.6K+
NOM
R37
5K
+5V
C32
.01
C31
.01
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
D1
D2
D3
D4
D5
D6
D7
D8
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
REFSLOW
REFOFF
BAND1SLOW
BAND1OFF
BAND2SLOW
BAND2OFF
BAND3SLOW
BAND3OFF
CSN4
CLK
CLR
U10
74HC273
NOTES: UNLE
1. CAPACIT
2. RESISTOR
3. RESISTOR
4. * IND

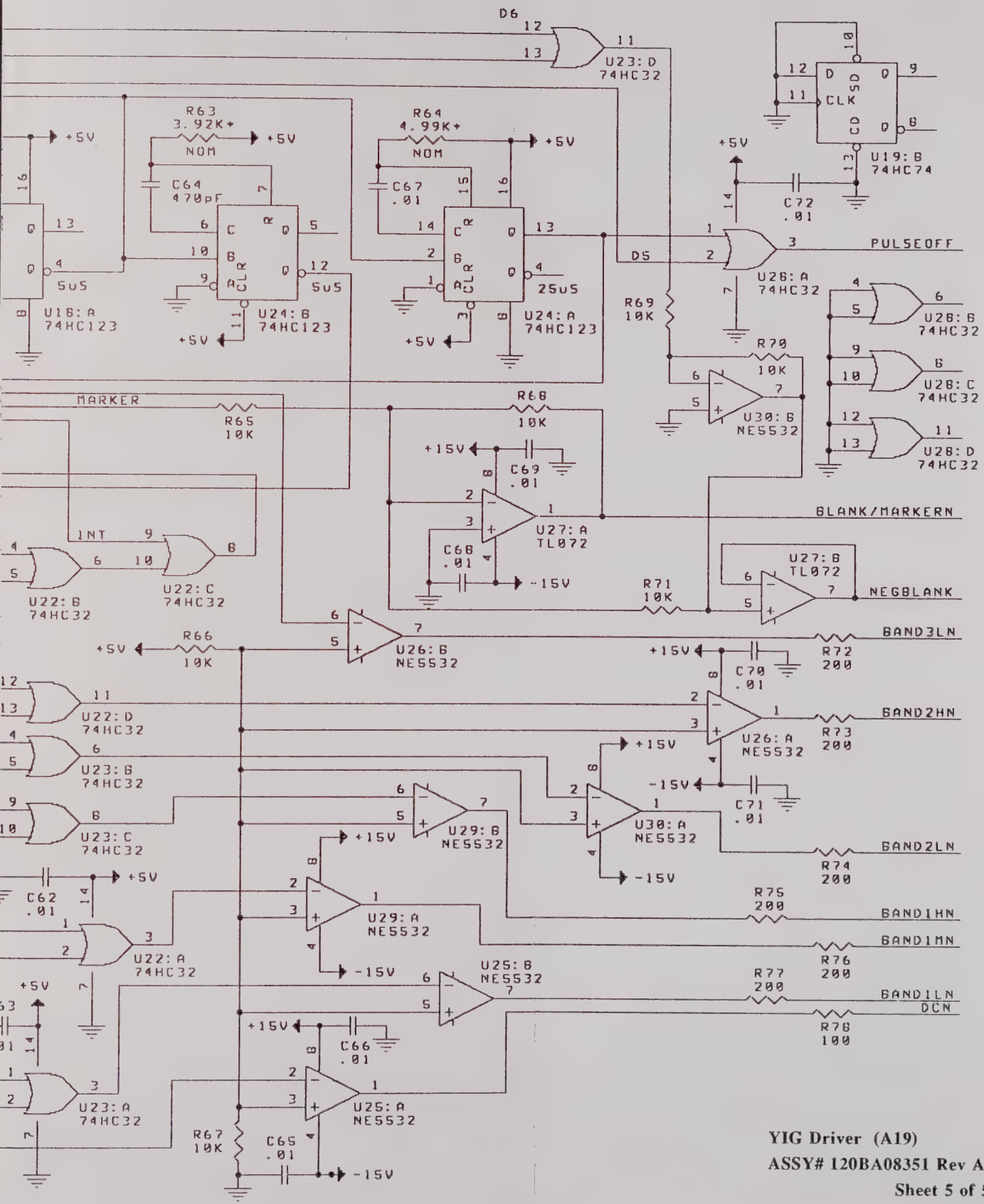



SS OTHERWISE SPECIFIED

R VALUES ARE IN uF
S VALUES ARE IN OHMS
S ARE 1/5W, 1%
CATES 1/4W, 1% RESISTOR

**YIG Driver (A19)**
**ASSY# 120BA08351 Rev A**
**Sheet 4 of 5**
**7-A19-4**


C50 .01
+5V
BD0
BD1
BD2
BD3
BD4
BD5
BD6
BD7
D0
D1
D2
D3
D4
D5
D6
D7
CSN6
CLK
CLR
U14 74HC273
ASWP
R53 4.99K
R51 10K
R52 1M
BAND2MT-
BAND3L
MARKER
INT
R61 232K+
NOM
C54 .01
C56 .01
R62 30.1K+
C61 .01
U18:B 74HC123
5uS
U19:A 74HC74
U15:B LM2901
13.0
R47 10K
C55 .01
C57 .01
U20:B 74HC86
U17:A 74HC86
U20:A 74HC86
C58 .001
R54 4.99K
R55 1M
C51 .01
8.0
R48 10K
U15:A LM2901
U17:B 74HC86
C59 .01
U21 74HC273
BAND2
BAND1MT-
R56 10K
R57 1M
R59 4.99K
R60 4.99K
5.2
R49 10K
U15:C LM2901
U17:C 74HC86
ASWP+DCN
+10VREF
R58 1M
3.2
R50 10K
U15:D LM2901
U17:D 74HC86
U20:D 74HC86
U20:C 74HC86
C60 .001
BAND1
C52 10uF 50V
C53 .1uF
U16 REF01
OUT
IN
TRIM
GND
+15V
D.C.




**YIG Driver (A19)**
**ASSY# 120BA08351 Rev A**
**Sheet 5 of 5**
**7-A19-5**

Bill of Material (by Ref Designator)

Parts List For: 120BA06951 100 MHz PLL PCA REV: A

| Item | Part Number | Qty | Mfgr | Mfr's Part Number | Description |
|---|---|---|---|---|---|
| 1 | 120BS06951 | 0.000 | | | 100 MHz PLL SCH |
| 3 | 120BF06951 | 1.000 | | | 100 MHz PLL PCB |
| 4 | ETST-06224 | 5.000 | USECO | 1280B-1 | TURRET TERMINAL |
| 5 | JJF0-02000 | 1.000 | BERG/D | 89F4578 | TWO CONTACT JUMPER |
| C 1 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 2 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 3 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 4 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 5 | CC50-02100 | 1.000 | AVX | SR155C122MAT | .001 UF CERAMIC Y5P |
| C 6 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 7 | CC50-03470 | 1.000 | KEMET | C320C473K5R5CA | .047 UF CERAMIC X7R |
| C 8 | CE25-R6470 | 1.000 | PANSON | ECEA1EU470 | 47 UF 25V RADIAL LEAD |
| C 9 | CE25-R6470 | 1.000 | PANSON | ECEA1EU470 | 47 UF 25V RADIAL LEAD |
| C 11 | CE25-R6470 | 1.000 | PANSON | ECEA1EU470 | 47 UF 25V RADIAL LEAD |
| C 12 | CE25-R6470 | 1.000 | PANSON | ECEA1EU470 | 47 UF 25V RADIAL LEAD |
| C 13 | CE25-R6470 | 1.000 | PANSON | ECEA1EU470 | 47 UF 25V RADIAL LEAD |
| C 14 | CE25-R6470 | 1.000 | PANSON | ECEA1EU470 | 47 UF 25V RADIAL LEAD |
| C 15 | CC50-04100 | 1.000 | KEMET | C322C104M5U5CA | .1 UF CERAMIC Z5U |
| C 16 | CC50-04100 | 1.000 | KEMET | C322C104M5U5CA | .1 UF CERAMIC Z5U |
| C 17 | CC50-04100 | 1.000 | KEMET | C322C104M5U5CA | .1 UF CERAMIC Z5U |
| C 18 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 19 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 20 | CC50-04100 | 1.000 | KEMET | C322C104M5U5CA | .1 UF CERAMIC Z5U |
| C 21 | CC50-01470 | 1.000 | KEMET | C315C471K1G5CA | 470 PF CERAMIC NPO |
| C 22 | CC50-01470 | 1.000 | KEMET | C315C471K1G5CA | 470 PF CERAMIC NPO |
| C 23 | CC50-04100 | 1.000 | KEMET | C322C104M5U5CA | .1 UF CERAMIC Z5U |
| C 24 | CC50-04100 | 1.000 | KEMET | C322C104M5U5CA | .1 UF CERAMIC Z5U |
| C 25 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 26 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 27 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 29 | CC50-05100 | 1.000 | AVX | SR305E105MAA | 1 UF CERAMIC Z5U |
| C 31 | CC50-05100 | 1.000 | AVX | SR305E105MAA | 1 UF CERAMIC Z5U |
| C 32 | CC50-02100 | 1.000 | AVX | SR155C122MAT | .001 UF CERAMIC Y5P |
| C 33 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 34 | CC50-02100 | 1.000 | AVX | SR155C122MAT | .001 UF CERAMIC Y5P |
| C 35 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 36 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 37 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 38 | CC50-02100 | 1.000 | AVX | SR155C122MAT | .001 UF CERAMIC Y5P |
| C 39 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 40 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 41 | CE25-R6470 | 1.000 | PANSON | ECEA1EU470 | 47 UF 25V RADIAL LEAD |
| C 42 | CC50-02100 | 1.000 | AVX | SR155C122MAT | .001 UF CERAMIC Y5P |
| C 43 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| C 44 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |

arts List For: 120BA06951 100 MHz PLL PCA REV: A

| tem | Part Number | Qty | Mfgr | Mfr's Part Number | Description |
|---|---|---|---|---|---|
| 45 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 46 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 47 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 48 | CC50-01220 | 1.000 | KEMET | C315C221K1G5CA | 220 PF CERAMIC NPO |
| 49 | CC50-01220 | 1.000 | KEMET | C315C221K1G5CA | 220 PF CERAMIC NPO |
| 50 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 51 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 52 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 53 | CC50-04100 | 1.000 | KEMET | C322C104M5U5CA | .1 UF CERAMIC Z5U |
| 54 | CC50-04100 | 1.000 | KEMET | C322C104M5U5CA | .1 UF CERAMIC Z5U |
| 55 | CC50-04100 | 1.000 | KEMET | C322C104M5U5CA | .1 UF CERAMIC Z5U |
| 56 | CC50-04100 | 1.000 | KEMET | C322C104M5U5CA | .1 UF CERAMIC Z5U |
| 57 | CC50-04100 | 1.000 | KEMET | C322C104M5U5CA | .1 UF CERAMIC Z5U |
| 58 | CC50-04100 | 1.000 | KEMET | C322C104M5U5CA | .1 UF CERAMIC Z5U |
| 59 | CC50-04100 | 1.000 | KEMET | C322C104M5U5CA | .1 UF CERAMIC Z5U |
| 60 | CC50-04100 | 1.000 | KEMET | C322C104M5U5CA | .1 UF CERAMIC Z5U |
| 61 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 62 | CC50-04100 | 1.000 | KEMET | C322C104M5U5CA | .1 UF CERAMIC Z5U |
| 63 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| 64 | CC50-04100 | 1.000 | KEMET | C322C104M5U5CA | .1 UF CERAMIC Z5U |
| 65 | CC50-03100 | 1.000 | TDK | RD30HX7R103K | .01 UF CERAMIC X7R |
| R 1 | DSA0-00300 | 1.000 | NATION | FDH300 | FDH300 LOW LEAK DIODE |
| R 2 | DSA0-00300 | 1.000 | NATION | FDH300 | FDH300 LOW LEAK DIODE |
| R 3 | DSA0-04148 | 1.000 | ANY | 1N4148 | 1N4148 G.P. DIODE |
| R 4 | DSA0-04148 | 1.000 | ANY | 1N4148 | 1N4148 G.P. DIODE |
| R 5 | DSA0-04148 | 1.000 | ANY | 1N4148 | 1N4148 G.P. DIODE |
| R 6 | DSA0-04148 | 1.000 | ANY | 1N4148 | 1N4148 G.P. DIODE |
| R 7 | DSA0-02810 | 1.000 | HP | 5082-2800 | 5082-2810 SCHOT. DIODE |
| R 8 | DSA0-02810 | 1.000 | HP | 5082-2800 | 5082-2810 SCHOT. DIODE |
| X 28 | CC50-00100 | 0.000 | KEMET | C315C100J2G5CA | 10 PF CERAMIC NPO |
| X 30 | CC50-00100 | 0.000 | KEMET | C315C100J2G5CA | 10 PF CERAMIC NPO |
| S 1 | ILRR-10125 | 1.000 | HP | HLMP-K101 | RED LED |
| 2 | JRBM-00101 | 1.000 | AMP | 903-373J-51A | SMB M RTANG PC MOUNT |
| 3 | JRBM-00101 | 1.000 | AMP | 903-373J-51A | SMB M RTANG PC MOUNT |
| 4 | JRBM-00101 | 1.000 | AMP | 903-373J-51A | SMB M RTANG PC MOUNT |
| 5 | JRBM-00101 | 1.000 | AMP | 903-373J-51A | SMB M RTANG PC MOUNT |
| 6 | JRBM-00101 | 1.000 | AMP | 903-373J-51A | SMB M RTANG PC MOUNT |
| 7 | JRBM-00101 | 1.000 | AMP | 903-373J-51A | SMB M RTANG PC MOUNT |
| 8 | JRBM-00101 | 1.000 | AMP | 903-373J-51A | SMB M RTANG PC MOUNT |
| 1 | LAD0-06220 | 1.000 | DALE | IMS5-22UH-10% | 22 UH INDUCTOR |
| 2 | LAD0-08120 | 1.000 | DALE | IMS 5 1200 UH 10 | 1200 UH INDUCTOR |
| 3 | LAD0-04680 | 1.000 | DALE | IMS 5.68UH-5% | .68 UH INDUCTOR |
| 1 | J1A1-03230 | 1.000 | DCS | 68000-503 | 3 PIN STRIPLINE PLUG |
| 2 | J1A1-02230 | 1.000 | SAMTEC | TSW-102-07-S-S | 2 PIN STRIPLINE PLUG |
| 3 | J1A1-02230 | 1.000 | SAMTEC | TSW-102-07-S-S | 2 PIN STRIPLINE PLUG |

Bill of Material (by Ref Designator)

Parts List For: 120BA06951 100 MHz PLL PCA REV: A

| Item | Part Number | Qty | Mfgr | Mfr's Part Number | Description |
|---|---|---|---|---|---|
| Q 1 | QBNS-04275 | 1.000 | ANY | PN4275 | PN4275 .1A 15V .6W NPN |
| Q 2 | QBNS-03643 | 1.000 | ANY | PN3643 | PN3643 .5A 30V .6W NPN |
| Q 3 | QBPS-02907 | 1.000 | ANY | PN2907 | PN2907 .5A 40V .6W PNP |
| Q 4 | QBNS-02222 | 1.000 | ANY | PN2222 | PN2222 .5A 30V NPN |
| Q 5 | QBNS-02222 | 1.000 | ANY | PN2222 | PN2222 .5A 30V NPN |
| Q 6 | QBNS-02222 | 1.000 | ANY | PN2222 | PN2222 .5A 30V NPN |
| R 1 | RN50-05620 | 1.000 | DALE | RN50C5620F | 562 OHMS 1% METAL FILM |
| R 2 | RN50-05620 | 1.000 | DALE | RN50C5620F | 562 OHMS 1% METAL FILM |
| R 3 | RN50-05620 | 1.000 | DALE | RN50C5620F | 562 OHMS 1% METAL FILM |
| R 4 | RN50-01000 | 1.000 | DALE | RN50C1000F | 100 OHMS 1% METAL FILM |
| R 5 | RN50-05620 | 1.000 | DALE | RN50C5620F | 562 OHMS 1% METAL FILM |
| R 6 | RN50-05620 | 1.000 | DALE | RN50C5620F | 562 OHMS 1% METAL FILM |
| R 7 | RN50-14750 | 1.000 | DALE | RN50C4751F | 4.75 K OHMS 1% MET FILM |
| R 8 | RN50-04750 | 1.000 | DALE | RN50C4750F | 475 OHMS 1% METAL FILM |
| R 9 | RN55-01000 | 1.000 | DALE | RN55C1000F | 100 OHMS 1% MET FILM |
| R 10 | RN55-01000 | 1.000 | DALE | RN55C1000F | 100 OHMS 1% MET FILM |
| R 11 | RN50-05620 | 1.000 | DALE | RN50C5620F | 562 OHMS 1% METAL FILM |
| R 12 | RN50-24750 | 1.000 | DALE | RN50C4752F | 47.5K OHMS 1% MET FILM |
| R 13 | RN50-24750 | 1.000 | DALE | RN50C4752F | 47.5K OHMS 1% MET FILM |
| R 14 | RN50-05620 | 1.000 | DALE | RN50C5620F | 562 OHMS 1% METAL FILM |
| R 15 | RN50-32740 | 1.000 | DALE | RN50C2734F | 274 K OHMS 1% MET FILM |
| R 16 | RN50-22000 | 1.000 | DALE | RN50C2002F | 20.0 K OHMS 1% MET FILM |
| R 17 | RN50-22000 | 1.000 | DALE | RN50C2002F | 20.0 K OHMS 1% MET FILM |
| R 18 | RN50-34990 | 1.000 | DALE | RN50C4993F | 499 K OHMS 1% MET FILM |
| R 19 | RN50-21000 | 1.000 | DALE | RN50C1002F | 10.0 K OHMS 1% MET FILM |
| R 20 | RN50-31000 | 1.000 | DALE | RN50C1003F | 100 K OHMS 1% MET FILM |
| R 21 | RN50-11000 | 1.000 | DALE | RNC50H1001FS | 1.00 K OHMS 1% MET FILM |
| R 22 | RN55-01000 | 1.000 | DALE | RN55C1000F | 100 OHMS 1% MET FILM |
| R 23 | RN55-01000 | 1.000 | DALE | RN55C1000F | 100 OHMS 1% MET FILM |
| R 24 | RN50-11000 | 1.000 | DALE | RNC50H1001FS | 1.00 K OHMS 1% MET FILM |
| R 25 | RN50-11000 | 1.000 | DALE | RNC50H1001FS | 1.00 K OHMS 1% MET FILM |
| R 26 | RN50-11000 | 1.000 | DALE | RNC50H1001FS | 1.00 K OHMS 1% MET FILM |
| R 27 | RN50-21000 | 1.000 | DALE | RN50C1002F | 10.0 K OHMS 1% MET FILM |
| R 28 | RN50-21000 | 1.000 | DALE | RN50C1002F | 10.0 K OHMS 1% MET FILM |
| R 29 | RN50-31000 | 1.000 | DALE | RN50C1003F | 100 K OHMS 1% MET FILM |
| R 30 | RN50-32740 | 1.000 | DALE | RN50C2734F | 274 K OHMS 1% MET FILM |
| R 31 | RN50-05620 | 1.000 | DALE | RN50C5620F | 562 OHMS 1% METAL FILM |
| R 32 | RN50-05620 | 1.000 | DALE | RN50C5620F | 562 OHMS 1% METAL FILM |
| R 33 | RN50-21000 | 1.000 | DALE | RN50C1002F | 10.0 K OHMS 1% MET FILM |
| R 34 | RN50-05620 | 1.000 | DALE | RN50C5620F | 562 OHMS 1% METAL FILM |
| R 35 | RN50-05620 | 1.000 | DALE | RN50C5620F | 562 OHMS 1% METAL FILM |
| R 36 | RN50-05620 | 1.000 | DALE | RN50C5620F | 562 OHMS 1% METAL FILM |
| R 37 | RN50-11000 | 1.000 | DALE | RNC50H1001FS | 1.00 K OHMS 1% MET FILM |
| R 38 | RN50-11000 | 1.000 | DALE | RNC50H1001FS | 1.00 K OHMS 1% MET FILM |
| R 39 | RN50-11000 | 1.000 | DALE | RNC50H1001FS | 1.00 K OHMS 1% MET FILM |

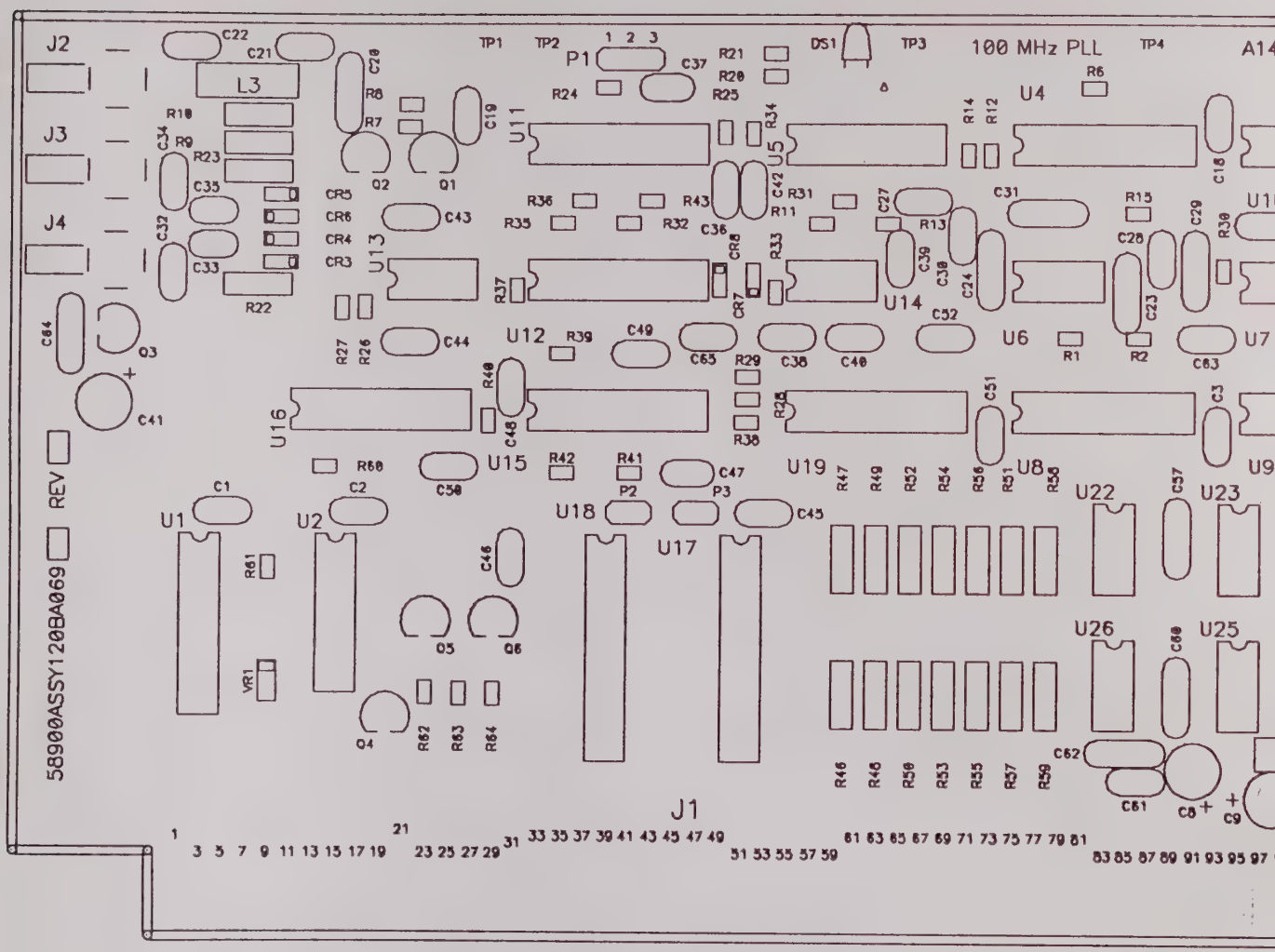
arts List For: 120BA06951 100 MHz PLL PCA REV: A

| tem | Part Number | Qty | Mfgr | Mfr's Part Number | Description |
|---|---|---|---|---|---|
| 40 | RN50-11000 | 1.000 | DALE | RNC50H1001FS | 1.00 K OHMS 1% MET FILM |
| 41 | RN50-11000 | 1.000 | DALE | RNC50H1001FS | 1.00 K OHMS 1% MET FILM |
| 42 | RN50-11000 | 1.000 | DALE | RNC50H1001FS | 1.00 K OHMS 1% MET FILM |
| 43 | RN50-11000 | 1.000 | DALE | RNC50H1001FS | 1.00 K OHMS 1% MET FILM |
| 44 | RN50-11000 | 1.000 | DALE | RNC50H1001FS | 1.00 K OHMS 1% MET FILM |
| 45 | RN50-11000 | 1.000 | DALE | RNC50H1001FS | 1.00 K OHMS 1% MET FILM |
| 46 | RN55-01500 | 1.000 | DALE | RN55C1500D | 150 OHMS 1% MET FILM |
| 47 | RN55-01500 | 1.000 | DALE | RN55C1500D | 150 OHMS 1% MET FILM |
| 48 | RN55-01500 | 1.000 | DALE | RN55C1500D | 150 OHMS 1% MET FILM |
| 49 | RN55-01500 | 1.000 | DALE | RN55C1500D | 150 OHMS 1% MET FILM |
| 50 | RN55-01500 | 1.000 | DALE | RN55C1500D | 150 OHMS 1% MET FILM |
| 51 | RN55-01500 | 1.000 | DALE | RN55C1500D | 150 OHMS 1% MET FILM |
| 52 | RN55-01500 | 1.000 | DALE | RN55C1500D | 150 OHMS 1% MET FILM |
| 53 | RN55-01500 | 1.000 | DALE | RN55C1500D | 150 OHMS 1% MET FILM |
| 54 | RN55-01500 | 1.000 | DALE | RN55C1500D | 150 OHMS 1% MET FILM |
| 55 | RN55-01500 | 1.000 | DALE | RN55C1500D | 150 OHMS 1% MET FILM |
| 56 | RN55-01500 | 1.000 | DALE | RN55C1500D | 150 OHMS 1% MET FILM |
| 57 | RN55-01500 | 1.000 | DALE | RN55C1500D | 150 OHMS 1% MET FILM |
| 58 | RN55-01500 | 1.000 | DALE | RN55C1500D | 150 OHMS 1% MET FILM |
| 59 | RN55-01500 | 1.000 | DALE | RN55C1500D | 150 OHMS 1% MET FILM |
| 60 | RN50-05620 | 1.000 | DALE | RN50C5620F | 562 OHMS 1% METAL FILM |
| 61 | RN50-11000 | 1.000 | DALE | RNC50H1001FS | 1.00 K OHMS 1% MET FILM |
| 62 | RN50-11000 | 1.000 | DALE | RNC50H1001FS | 1.00 K OHMS 1% MET FILM |
| 63 | RN50-11000 | 1.000 | DALE | RNC50H1001FS | 1.00 K OHMS 1% MET FILM |
| 64 | RN50-11000 | 1.000 | DALE | RNC50H1001FS | 1.00 K OHMS 1% MET FILM |
| 1 | UTN0-01382 | 1.000 | TI | 74HC138N | 74HC138 DECODER/DEMULTIP |
| 2 | UTN0-01252 | 1.000 | TI | SN74HC125AN | MC74HC125N QUAD BUFFER |
| 3 | URP0-78150 | 1.000 | MOT | MC78L15ACP | MC78L15 .1A 15V REG |
| 4 | UEN0-10138 | 1.000 | MOT | MC10138P PLASTIC | MC10138P BI-QUINARY CTR |
| 5 | UEN0-12040 | 1.000 | MOT | MC12040P | MC12040P PHASE/FREQ DET |
| 6 | UON0-00072 | 1.000 | TI | TL072CP | TL072CP DUAL FET OP AMP |
| 7 | ULN0-00311 | 1.000 | TI | LM311P | LM311N COMPARATOR |
| 8 | UEN0-10216 | 1.000 | MOT | MC10216PC | MC10216P TRIPLE RCVR |
| 9 | UEN0-10216 | 1.000 | MOT | MC10216PC | MC10216P TRIPLE RCVR |
| 10 | UEN0-10216 | 1.000 | MOT | MC10216PC | MC10216P TRIPLE RCVR |
| 11 | UEN0-10216 | 1.000 | MOT | MC10216PC | MC10216P TRIPLE RCVR |
| 12 | UEN0-10102 | 1.000 | MOT | MC10102P | MC10102P QUAD NOR |
| 13 | ULN0-00311 | 1.000 | TI | LM311P | LM311N COMPARATOR |
| 14 | ULN0-00311 | 1.000 | TI | LM311P | LM311N COMPARATOR |
| 15 | UEN1-10113 | 1.000 | MOT | MC10H113P | MC10H113P QUAD OR GATE |
| 16 | UEN0-10102 | 1.000 | MOT | MC10102P | MC10102P QUAD NOR |
| 17 | UTN0-02732 | 1.000 | TI | 74HC273N | 74HC273;OCTAL D-TYPE F-F |
| 18 | UTN0-02732 | 1.000 | TI | 74HC273N | 74HC273;OCTAL D-TYPE F-F |
| 19 | UEN0-10124 | 1.000 | MOT | MC10124P | MC10124P QUAD TTL TO ECL |
| 20 | UON0-05532 | 1.000 | SIG | NE5532N | NE5532 DUAL OP AMP |

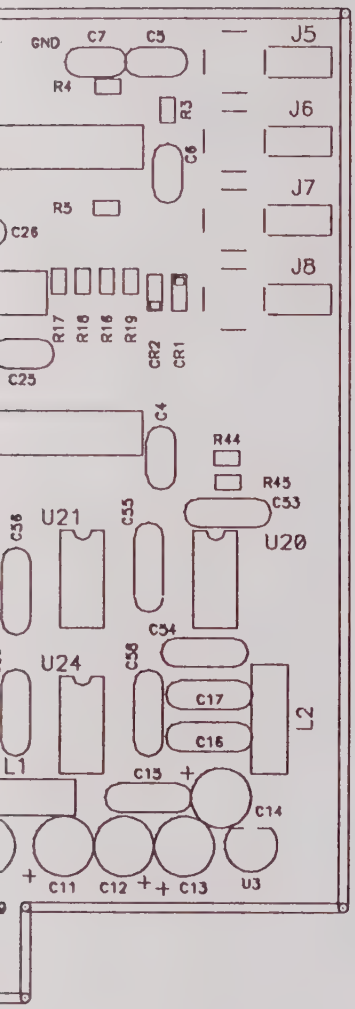
Bill of Material (by Ref Designator)

Parts List For: 120BA06951 100 MHz PLL PCA REV: A

| Item | Part Number | Qty | Mfgr | Mfr's Part Number | Description |
|---|---|---|---|---|---|
| U 21 | UONO-05532 | 1.000 | SIG | NE5532N | NE5532 DUAL OP AMP |
| U 22 | UONO-05532 | 1.000 | SIG | NE5532N | NE5532 DUAL OP AMP |
| U 23 | UONO-05532 | 1.000 | SIG | NE5532N | NE5532 DUAL OP AMP |
| U 24 | UONO-05532 | 1.000 | SIG | NE5532N | NE5532 DUAL OP AMP |
| U 25 | UONO-05532 | 1.000 | SIG | NE5532N | NE5532 DUAL OP AMP |
| U 26 | UONO-05532 | 1.000 | SIG | NE5532N | NE5532 DUAL OP AMP |
| VR 1 | DZAD-04732 | 1.000 | ANY | 1N4732A | IN4732A 4.7 V ZENER |




**100 MHz Ref PLL (A14)**
**ASSY# 120BA06951 Rev A**
**Sheet 2 of 4**
**7-A14-2**



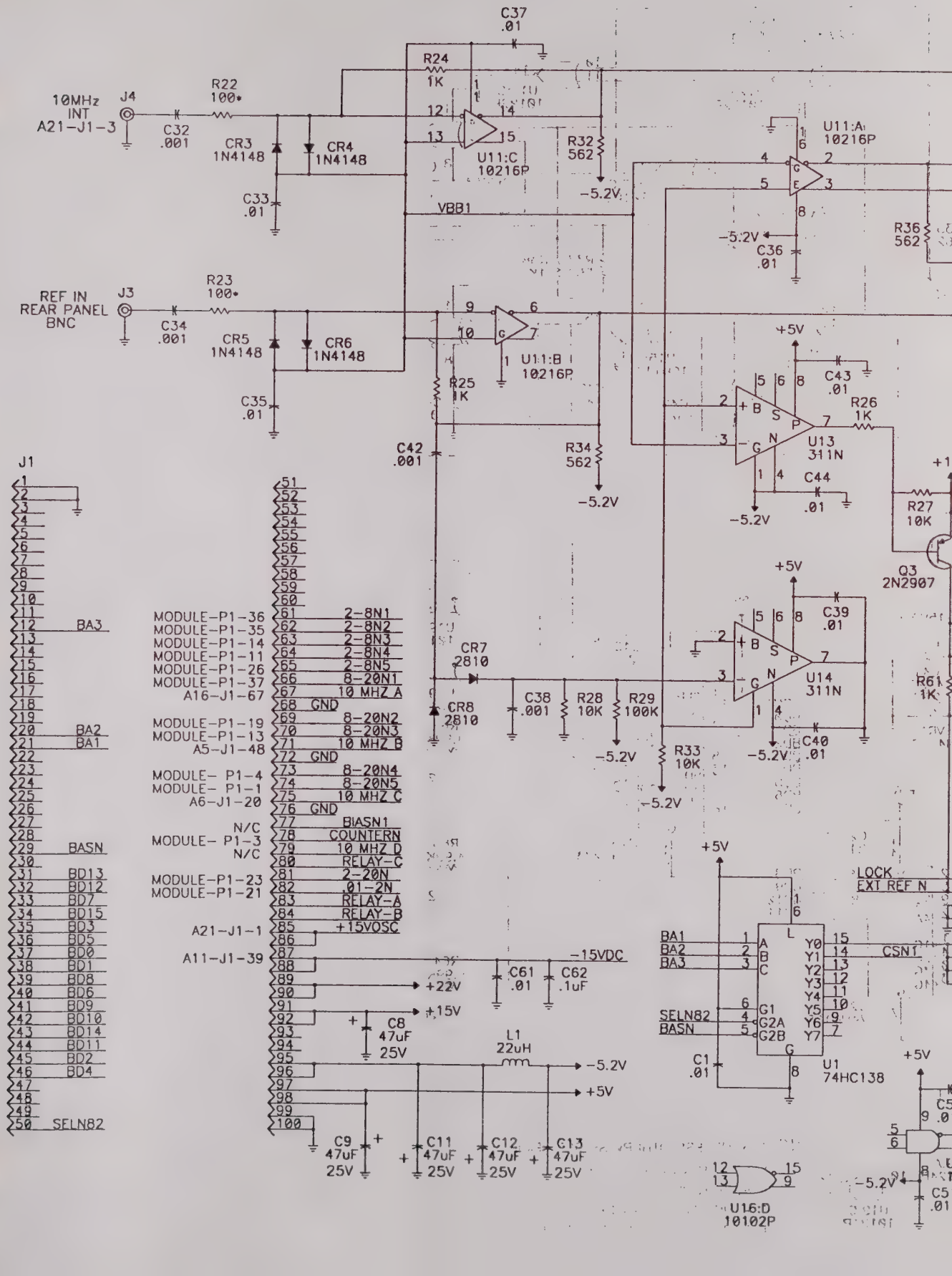

## 100 MHZ REFERENCE PHASE LOCKED LOOP -- PC ASSY A14

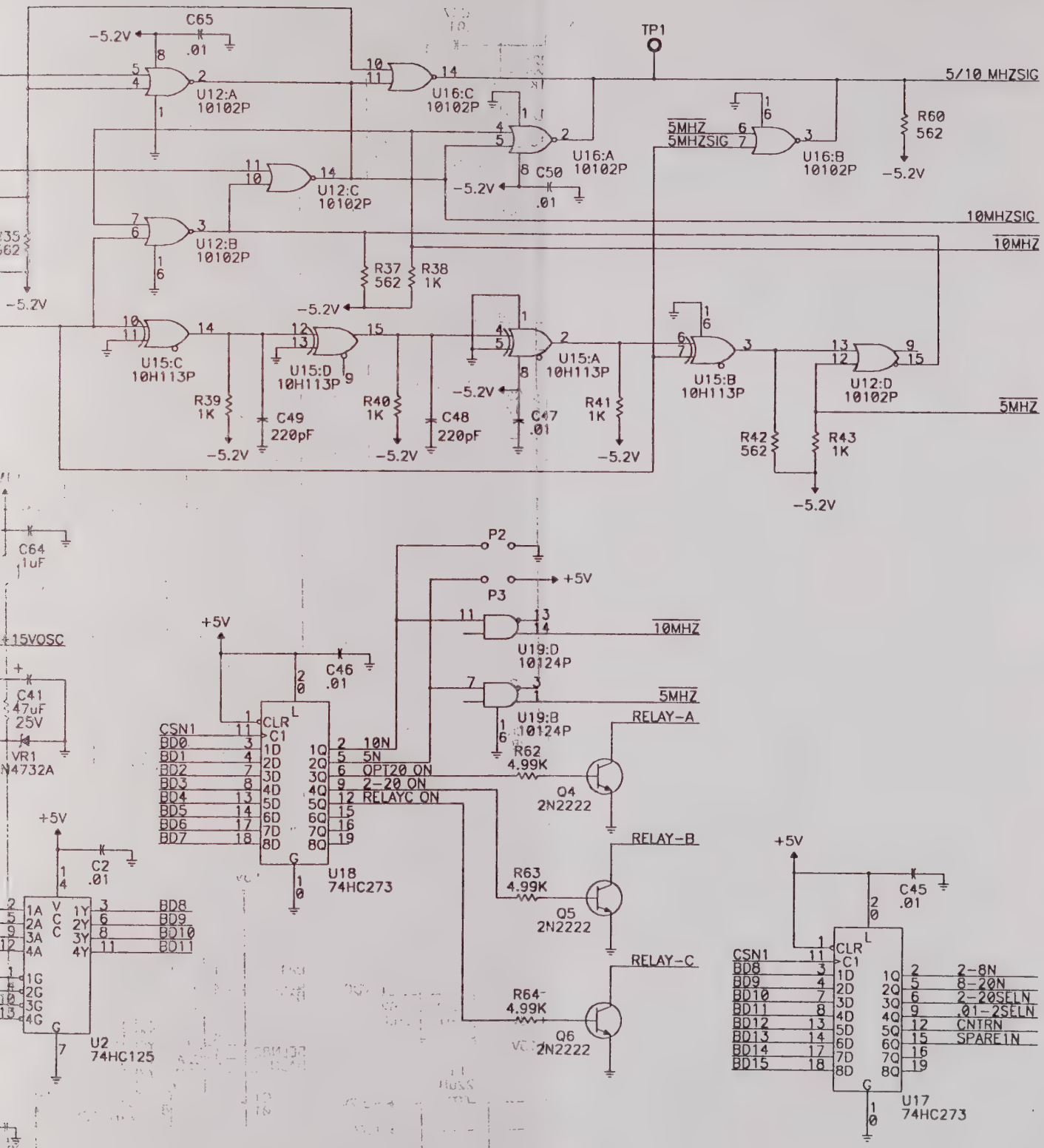
This circuit is used to phase lock the 100 MHz oscillator (A201) to the internal 10 MHz timebase or to an external timebase; in addition to the loop output it produces a lock indicator signal and a set of buffered 10 MHz outputs to be used for references for other loops in the instrument.

The 100 MHz input at J5 is buffered by U10 B before being divided down to 10 MHz by U4. This 10 MHz is then buffered by U8 A, B, C and U9 A, B and C so that it can be used by other circuits in the unit which require a 10 MHz reference. The signal is also applied to the variable input of the phase detector U5-9.

The reference input to the phase detector U5-6 comes from a switching circuit, which selects either an internal or external 10 MHz reference. When no external reference is present at J3 the internal 10 MHz reference at J4, buffered by U11 A, is allowed to propagate through U12 C and on to the phase detector (U5-6). When an external 10 MHz signal is present at J3 it is buffered by U11 A and allowed to propagate through U12 A to the phase detector. The presence of an external 10 MHz reference is detected when a charge is built up on C38 causing the switching circuit (comparator U14) to switch to a high state, in turn causing U13 output to go high which ultimately turns off the supply to the internal 10MHz reference. In addition, the switching circuit enables the external reference path at U12 A and disables the internal reference at U12 C. The selected reference is then available through Q1 and Q2 as the 10 MHz reference output on the rear panel.

The phase comparator U5 compares the 10MHz reference with the output of the divider U4 and determines which signal leads or lags the other. The output pulses at U5-12 and 3 are integrated or filtered by U6 B resulting in a tuning or correction voltage at J6 which will steer the 100 MHz VCXO oscillator in the proper direction (a more positive voltage increases frequency) to acquire and sustain a locked condition. When the loop is phase locked (the reference and variable input frequency and phase are equal) the output pulses of the phase detector will be extremely narrow at a 10 MHz rate. U7, CR1 and CR2 along with other components serve as a window detector which detects the tuning voltage and detects unlocked conditions. When the loop unlocks U7-7 goes low, lighting DS1 and sending the unlock logic level to the computer via U2, a tri-state buffer which serves as the interface to the bus. U1 is a 3 to 8 decoder which is used for decoding chip selects.


10MHz INT A21-J1-3
J4
C32 .001
R22 100•
CR3 1N4148
CR4 1N4148
C33 .01
C37 .01
R24 1K
U11:C 10216P
R32 562
-5.2V
VBB1
U11:A 10216P
R36 562
C36 .01
REF IN REAR PANEL BNC
J3
C34 .001
R23 100•
CR5 1N4148
CR6 1N4148
C35 .01
U11:B 10216P
R25 1K
C42 .001
R34 562
+5V
C43 .01
R26 1K
U13 311N
C44 .01
R27 10K
Q3 2N2907
C39 .01
U14 311N
C40 .01
R61 1K
CR7 2810
CR8 2810
C38 .001
R28 10K
R29 100K
R33 10K
J1
MODULE-P1-36 2-8N1
MODULE-P1-35 2-8N2
MODULE-P1-14 2-8N3
MODULE-P1-11 2-8N4
MODULE-P1-26 2-8N5
MODULE-P1-37 8-20N1
A16-J1-67 10 MHZ A
GND
MODULE-P1-19 8-20N2
MODULE-P1-13 8-20N3
A5-J1-48 10 MHZ B
GND
MODULE- P1-4 8-20N4
MODULE- P1-1 8-20N5
A6-J1-20 10 MHZ C
GND
N/C BIASN1
MODULE- P1-3 COUNTERN
N/C 10 MHZ D
RELAY-C
MODULE-P1-23 2-20N
MODULE-P1-21 .01-2N
RELAY-A
RELAY-B
A21-J1-1 +15VOSC
A11-J1-39 -15VDC
+22V
+15V
C8 47uF 25V
L1 22uH
-5.2V
+5V
C9 47uF 25V
C11 47uF 25V
C12 47uF 25V
C13 47uF 25V
C61 .01
C62 .1uF
BA3
BA2
BA1
BASN
BD13
BD12
BD7
BD15
BD3
BD5
BD0
BD1
BD8
BD6
BD9
BD10
BD14
BD11
BD2
BD4
SELN82
BA1
BA2
BA3
SELN82
BASN
U1 74HC138
C1 .01
LOCK
EXT REF N
CSN1
U16:D 10102P
C5 .01




NOTES: UNLESS OTHERWISE SPECIFIED

1. RESISTORS ARE IN OHMS.
2. RESISTORS ARE 1/5W, 1%.
3. * INDICATES 1/4W RESISTORS.
4. CAPACITOR VALUES ARE IN uF.

**100 MHz Ref PLL (A14)**
**ASSY# 120BA06951 Rev A**
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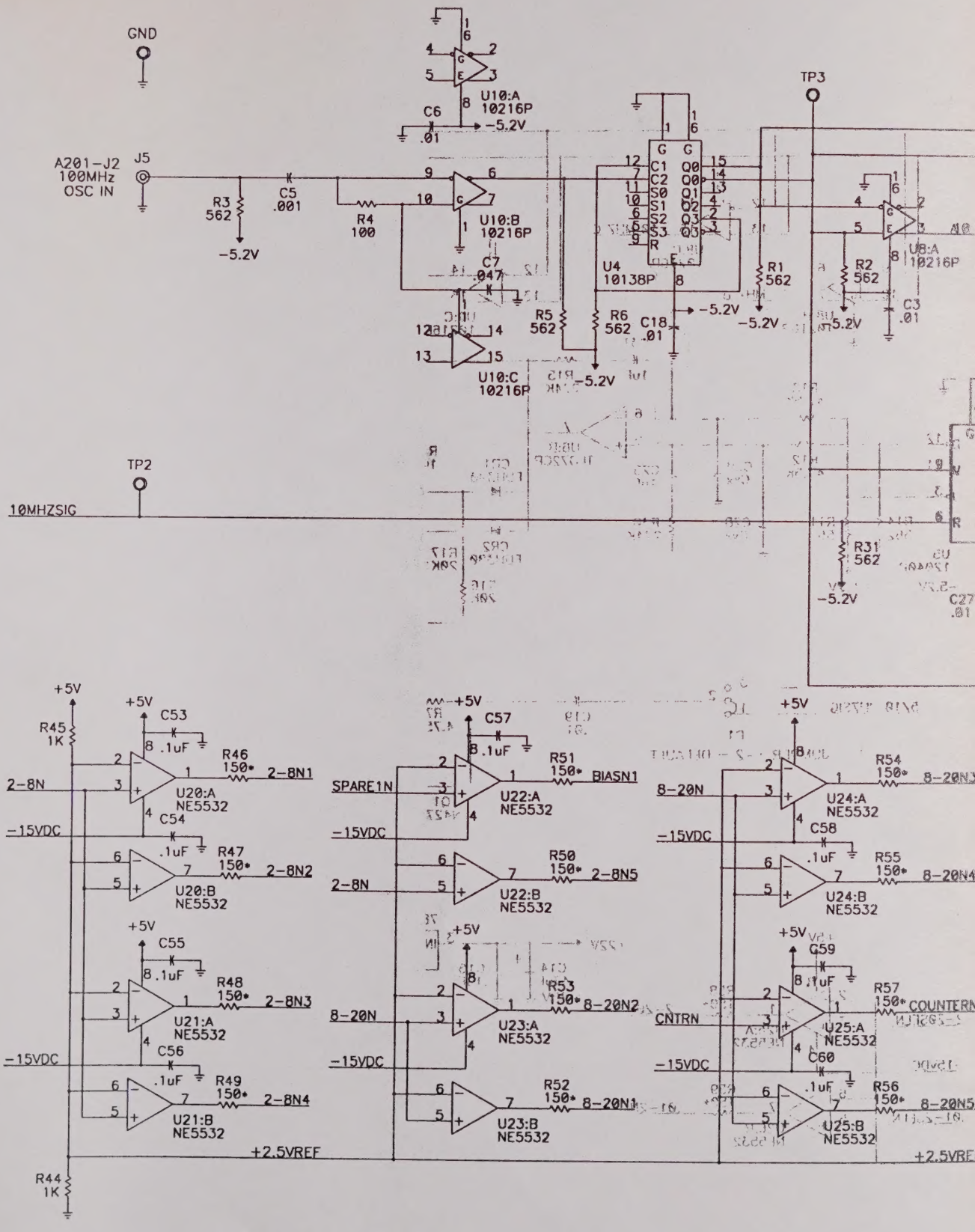
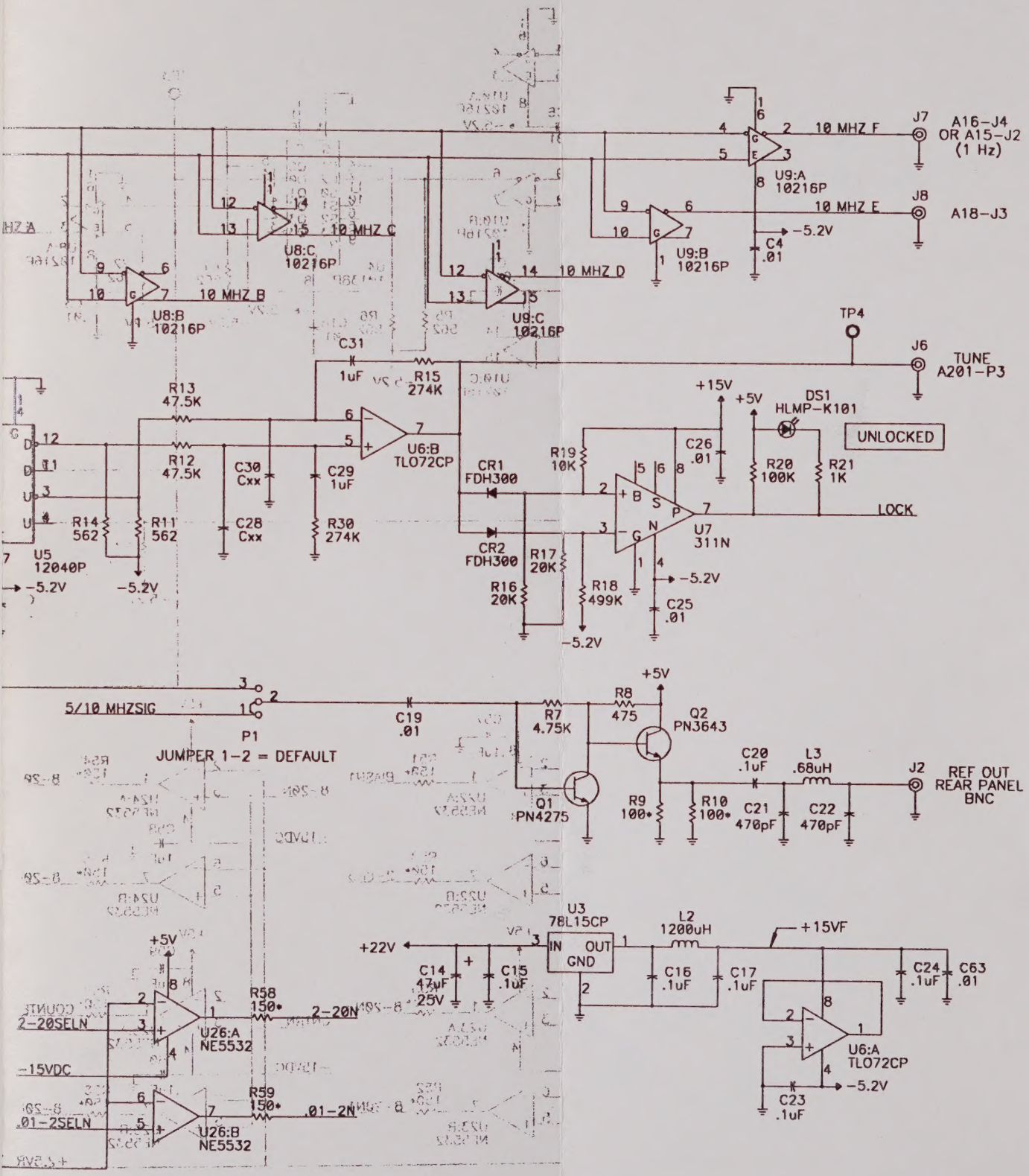
**7-A14-3**


GND
A201-J2
100MHz
OSC IN
J5
R3
562
-5.2V
C5
.001
R4
100
U10:A
10216P
C6
.01
-5.2V
U10:B
10216P
C7
.047
U10:C
10216P
R5
562
R6
562
-5.2V
U4
10138P
C18
.01
-5.2V
TP3
R1
562
-5.2V
R2
562
-5.2V
C3
.01
U8:A
10216P
TP2
10MHZSIG
R31
562
-5.2V
+5V
R45
1K
C53
.1uF
R46
150*
2-8N1
U20:A
NE5532
2-8N
C54
-15VDC
.1uF
R47
150*
2-8N2
U20:B
NE5532
C55
.1uF
R48
150*
2-8N3
U21:A
NE5532
C56
-15VDC
.1uF
R49
150*
2-8N4
U21:B
NE5532
R44
1K
+2.5VREF
C57
.1uF
R51
150*
BIASN1
SPARE1N
U22:A
NE5532
-15VDC
R50
150*
2-8N5
2-8N
U22:B
NE5532
R53
150*
8-20N2
8-20N
U23:A
NE5532
-15VDC
R52
150*
8-20N1
U23:B
NE5532
C59
.1uF
R54
150*
8-20N3
8-20N
U24:A
NE5532
-15VDC
C58
.1uF
R55
150*
8-20N4
U24:B
NE5532
C60
.1uF
R57
150*
COUNTERN
CNTRN
U25:A
NE5532
-15VDC
.1uF
R56
150*
8-20N5
U25:B
NE5532
+2.5VREF

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**ASSY# 120BA06951 Rev A**
**Sheet 4 of 4**
**7-A14-4**

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